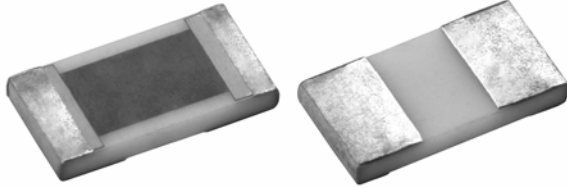


High Power Thin Film Wraparound Chip Resistor



PHP series chip resistors are designed with enlarged backside terminations to reduce the thermal resistance between the topside resistor layer and the solder joint on the end users circuit board.

Actual power handling capability is limited by the end user mounting process. As with any high power chip resistor the ability to remove the generated heat is critical to the overall performance of the device.

FEATURES

- High purity ceramic substrate
- Power rating to 2.5 W
- Resistance range 10 Ω to 30 k Ω
- Resistor tolerance to ± 0.1 %
- TCR to ± 25 ppm/ $^{\circ}$ C
- Flame resistant UL 94 V-0

APPLICATIONS

- Power supplies
- Power switching
- Braking system
- Test and measurement equipment
- Motor deflection circuits

TYPICAL PERFORMANCE

| | ABSOLUTE |
|------|----------|
| TCR | 25 |
| TOL. | 0.1 |

STANDARD ELECTRICAL SPECIFICATIONS

| TEST | SPECIFICATIONS | CONDITIONS |
|--------------------------------|---|---|
| Material | Nichrome | - |
| Resistance Range | 10 Ω to 30 k Ω | - |
| TCR: Absolute | 25 ppm/ $^{\circ}$ C, 50 ppm/ $^{\circ}$ C (standard) and 100 ppm/ $^{\circ}$ C | - 55 $^{\circ}$ C to + 125 $^{\circ}$ C |
| Tolerance: Absolute | 0.1 %, 0.5 %, 1.0 % and 5.0 % | + 25 $^{\circ}$ C |
| Power Rating: Resistor | 1206: 1.0 W, 2512: 2.5 W ⁽¹⁾ | Maximum at + 70 $^{\circ}$ C |
| Stability: Absolute | ΔR 0.1 % | 2000 h at + 70 $^{\circ}$ C |
| Stability: Ratio | Not applicable | - |
| Voltage Coefficient | < 0.1 ppm/V | - |
| Working Voltage | 1206: 100 V, 2512: 200 V | - |
| Operating Temperature Range | - 55 $^{\circ}$ C to + 125 $^{\circ}$ C | - |
| Storage Temperature Range | - 55 $^{\circ}$ C to + 150 $^{\circ}$ C | - |
| Noise | < - 30 dB | - |
| Shelf Life Stability: Absolute | ± 0.01 % | 1 year at + 25 $^{\circ}$ C |

COMPONENT RATINGS

| CASE SIZE | POWER RATING (mW) | WORKING VOLTAGE (V) | RESISTANCE RANGE (Ω) |
|-----------|---------------------|---------------------|-------------------------------|
| 1206 | 1000 ⁽¹⁾ | 100 | 10 to 30K |
| 2512 | 2500 ⁽¹⁾ | 200 | 10 to 30K |

Note

⁽¹⁾ Dependent on component mounting by user

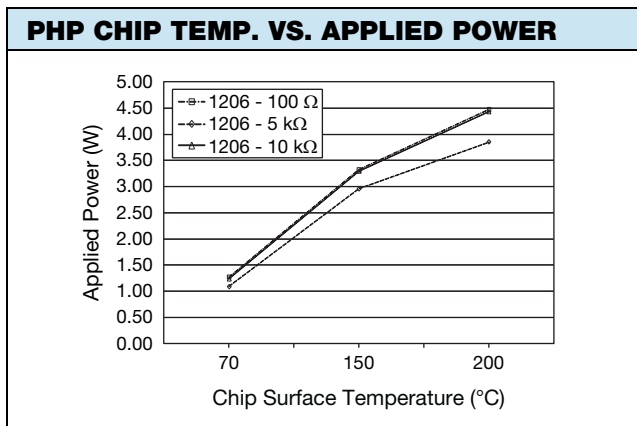
ENVIRONMENTAL TESTS (Vishay Performance vs. MIL-PRF-55342 Requirements)

| ENVIRONMENTAL TEST | LIMITS MIL-PRF-55342 CHARACTERISTIC "E" | TYPICAL VISHAY PERFORMANCE |
|---|---|----------------------------|
| Resistance Temperature Characteristic | ± 25 ppm/ $^{\circ}$ C | ± 15 ppm/ $^{\circ}$ C |
| Maximum Ambient Temperature at Rated Wattage | + 70 $^{\circ}$ C | + 70 $^{\circ}$ C |
| Maximum Ambient Temperature at Power Derating | + 150 $^{\circ}$ C | + 150 $^{\circ}$ C |
| Thermal Shock | ± 0.1 % | ± 0.04 % |
| Low Temperature Operation | ± 0.1 % | ± 0.001 % |
| Short Time Overload | ± 0.1 % | ± 0.003 % |
| High Temperature Exposure | ± 0.1 % | ± 0.030 % |
| Resistance to Soldering Heat | ± 0.2 % | ± 0.007 % |
| Moisture Resistance | ± 0.2 % | ± 0.002 % |
| Life at + 70 $^{\circ}$ C for 2000 h | ± 0.5 % | ± 0.100 % |

| DIMENSIONS in inches | | | | | |
|----------------------|-----------------------|----------------------------|------------------------|------------------------------|---------------------------------|
| | | | | | |
| CASE SIZE | LENGTH | WIDTH W (± 0.005) | THICKNESS MIN./MAX. | TOP PAD D (± 0.005) | BOTTOM PAD E (± 0.005) |
| 1206 | 0.126 \pm 0.008 | 0.063 | 0.015/0.033 | 0.020 + 0.005/- 0.010 | 0.040 |
| 2512 | 0.259 + 0.009/- 0.015 | 0.124 | 0.015/0.033 | 0.02 | 0.050 |

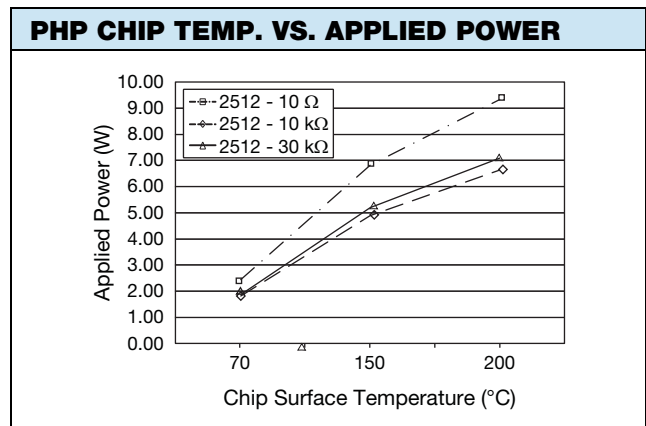
| LAND PATTERN DIMENSIONS in inches | |
|--|--|
| <p>PHP Land Pattern for 1206 Case Size</p> | <p>PHP Land Pattern for 2512 Case Size</p> |

| STANDARD MATERIAL SPECIFICATIONS | |
|----------------------------------|---|
| Resistive Element | Nichrome |
| Substrate Material | Alumina (Al ₂ O ₃) |
| Terminations (Tin/Lead) | Tin/lead solder over nickel barrier |
| Terminations (Lead (Pb)-free) | Tin/silver/copper (Sn96.5Ag3.0Cu0.5) solder over nickel barrier |



Notes

- Chip surface temperature measured using FLIR A40 thermal imaging system with an approximate test card surface temperature of 85 °C.
- Thermal imaging was conducted under ambient conditions resulting in a steady state test card surface temperature of 85 °C over the full range of power levels.
- Thermal imaging and load life testing was conducted mounting one device to 2" x 3" test cards with 2.5 mil copper plating on both surfaces. Thermal vias on 120 mil centers were utilized for heat transfer between surfaces of the test card.



Notes

- Chip surface temperature measured using FLIR A40 thermal imaging system with an approximate test card surface temperature of 85 °C.

| Case Size | 2512 | 2512 | 2512 |
|------------------|------------|-------------|-------------|
| Resistance Value | Up to 10 Ω | Up to 10 kΩ | Up to 30 kΩ |
| Temperature | Power (W) | | |
| 70 | 2.44 | 1.81 | 1.87 |
| 150 | 6.82 | 4.89 | 5.19 |
| 200 | 9.33 | 6.63 | 7.09 |

| GLOBAL PART NUMBER INFORMATION | | | | | | | | | | | | | | | | | | |
|--------------------------------|--------------------|----------------------|---------------------------|---------------------------|--|----------|----------|--------------------|--------------------|--------------------|--------------------|--------------------|---|---|--|----------|--|--|
| P | H | P | 0 | 1 | 2 | 0 | 6 | E | 1 | 0 | 0 | 2 | B | B | T | 1 | | |
| GLOBAL MODEL | SUBSTRATE | CASE SIZE | TCR | | RESISTANCE | | | TOLERANCE | | TERMINATION | | | PACKAGING | | | | | |
| PHP | 0 = Alumina | 1206 2512 | E = ± 25 ppm/°C | H = ± 50 ppm/°C | The first 3 digits are significant figures and the last digit specifies the number of zeros to follow. "R" designates the decimal point. Example: 10R0 = 10 Ω 1000 = 100 Ω 1001 = 1 kΩ | | | B = ± 0.1 % | D = ± 0.5 % | F = ± 1.0 % | G = ± 2.0 % | J = ± 5.0 % | B = Wraparound Sn/Pb solder w/nickel barrier | S = Wraparound lead (Pb)-free solder SAC-305 RoHS compliant - e1 | BS = BULK 100 min., 1 mult WS = WAFFLE 100 min., 1 mult WI = WAFFLE (item single lot day code) 100 min., 1 mult TAPE AND REEL T1 = 1000 min., 1000 mult TF = Full reel TS = 100 min., 1 mult TI = 100 min., 1 mult (item single lot date code) TP = 100 min., 1 mult (package unit single lot date) | | | |



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