ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
NUC140 Data Sheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. NuMicro™ NUC100 Series includes NUC100, NUC120, NUC130 and NUC140 product line.

The NuMicro™ NUC140 Connectivity Line with USB 2.0 full-speed and CAN functions embeds Cortex™-M0 core running up to 50 MHz with 64K/128K-byte embedded flash, 8K/16K-byte embedded SRAM, and 4K-byte loader ROM for the ISP. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI/MICROWIRE, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, PS2, USB 2.0 FS Device, 12-bit ADC, Analog Comparator, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS2	I^2S
NUC100	•	•	•				•	•
NUC120	•	•	•	•			•	•
NUC130	•	•	•		•	•	•	•
NUC140	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Supported Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 NuMicro™ NUC140 Features – Connectivity Line

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep-mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Build-in LDO for wide operating voltage ranges from 2.5V to 5.5V
- Flash EPROM Memory
  - 64K/128K bytes Flash EPROM for program code (128KB only support in Medium Density)
  - 4KB flash for ISP loader
  - Support In-system program (ISP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128KB system, fixed 4KB data flash for 64KB system (Only support 4KB data flash in Low Density)
  - Support 2 wire ICP update through SWD/ICE interface
  - Support fast parallel programming mode by external programmer
- SRAM Memory
  - 8K/16K bytes embedded SRAM (16KB only support in Medium Density)
  - Support PDMA mode
- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals (Only support 1 channel in Low Density)
- Clock Control
  - Flexible selection for different applications
  - Build-in 22.1184 MHz OSC (Trimmed to 1%) for system operation, and low power 10 kHz OSC for watchdog and wakeup sleep operation
  - Support one PLL, up to 50 MHz, for high performance system operation
  - External 4~24 MHz crystal input for USB and precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
- Timer
  - Support 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter

- Independent clock source for each timer
- Provides one-shot, periodic, toggle and auto-reload counting operation modes

- Watch Dog Timer
  - Multiple clock sources
  - 8 selectable time out period from 6ms ~ 3.0sec (depends on clock source)
  - WDT can wake up from power down or sleep mode
  - Interrupt or reset selectable on watchdog time-out
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Support wake up function
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
  - Support Capture interrupt
- UART
  - Up to three UART controllers (Low Density only support 2 UART controllers).
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART0 with 63-byte FIFO is for high speed
  - UART1/2(optional) with 15-byte FIFO for standard device
  - Support IrDA (SIR) and LIN function
  - Support RS-485 9 bit mode and direction control. (Low Density Only)
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode
- SPI
  - Up to four sets of SPI controller
  - Master up to 20 MHz, and Slave up to 10 MHz
  - Support SPI/MICROWIRE master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Support byte suspend mode in 32-bit transmission
  - Support PDMA mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Support multiple address recognition (four slave address with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive
- CAN 2.0
  - CAN 2.0B protocol compatible device
  - Support 11-bit identifier as well as 29-bit identifier
  - Bit rates up to 1Mbits/s
  - NRZ bit Coding/ Encoding
  - Error Detection & Status Report
    - Bit error, Form error, Stuffing error, 15-bit CRC detection, and Acknowledge error Interrupt
    - Each CAN-bus error and Transmission/Receive Done
  - Bit Timing Synchronization
  - Acceptance filter extension
  - Sleep mode wake up
- PS2 Device Controller
  - Host communication inhibit and request to send detection
  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provide 1 interrupt source with 4 interrupt events
  - Support Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 Bytes internal SRAM as USB buffer
  - Provide remote wakeup capability
- EBI (External bus interface) support (Low Density 64-pin Package Only)

- Accessible space: 64KB in 8-bit mode or 128KB in 16-bit mode
- Support 8bit/16bit data width
- Support byte write in 16bit data width mode

- ADC
  - 12-bit SAR ADC with 600K SPS
  - Up to 8-ch single-end input or 4-ch differential input
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by software programming or external input
  - Support PDMA Mode
- Analog Comparator
  - Up to two analog comparator
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up
- One built-in temperature sensor with 1℃ resolution
- Brown-out detector
  - With 4 levels: 4.5V/3.8V/2.7V/2.2V
  - Support Brownout Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0V
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin / 64-pin / 48-pin (100-pin for Medium Density Only)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC140 Products Selection Guide

3.1.1 NuMicro™ NUC140 Medium Density Connectivity Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I^2C	USB	LIN	CAN								
NUC140LD3AN	64 KB	16 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140LE3AN	128 KB	16 KB	Definable	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140RD3AN	64 KB	16 KB	4 KB	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	-	v	LQFP64
NUC140RE3AN	128 KB	16 KB	Definable	4 KB	up to 45	4x32-bit	3	2	2	1	2	1	1	2	4	8x12-bit	v	-	v	LQFP64
NUC140VD2AN	64 KB	8 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	2	1	1	2	8	8x12-bit	v	-	v	LQFP100
NUC140VD3AN	64 KB	16 KB	4 KB	4 KB	up to 76	4x32-bit	3	4	2	1	2	1	1	2	8	8x12-bit	v	-	v	LQFP100
NUC140VE3AN	128 KB	16 KB	Definable	4 KB	up to 76	4x32-bit	3	4	2	1	2	1	1	2	8	8x12-bit	v	-	v	LQFP100

3.1.2 NuMicro™ NUC140 Low Density Connectivity Line Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP ICP	Package
							UART	SPI	I^2C	USB	LIN	CAN								
NUC140LC1BN	32 KB	4 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140LD2BN	64 KB	8 KB	4 KB	4 KB	up to 31	4x32-bit	2	1	2	1	2	1	1	1	4	8x12-bit	v	-	v	LQFP48
NUC140RC1BN	32 KB	4 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64
NUC140RD2BN	64 KB	8 KB	4 KB	4 KB	up to 45	4x32-bit	2	2	2	1	2	1	1	2	4	8x12-bit	v	v	v	LQFP64

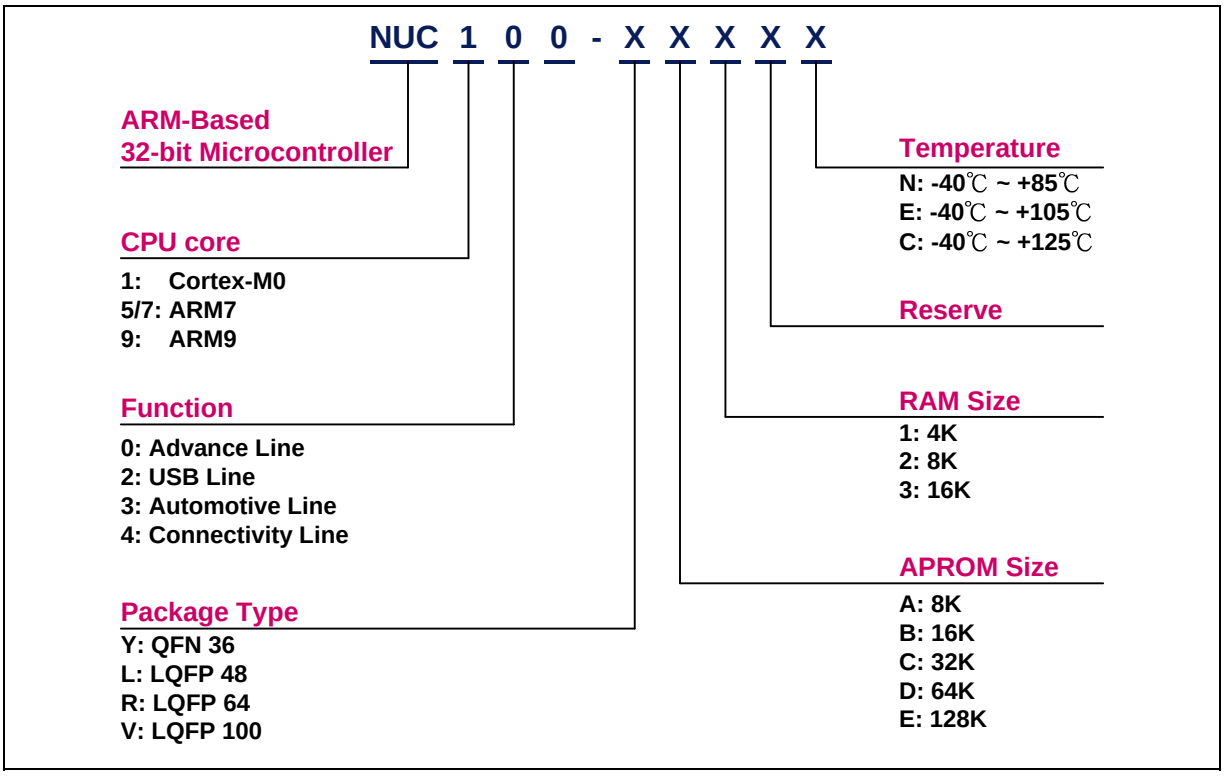


Figure 3-1 NuMicro™ NUC100 Series selection code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC140 Medium Density Pin Diagram

3.2.1.1 NuMicro™ NUC140 LQFP 100 pin

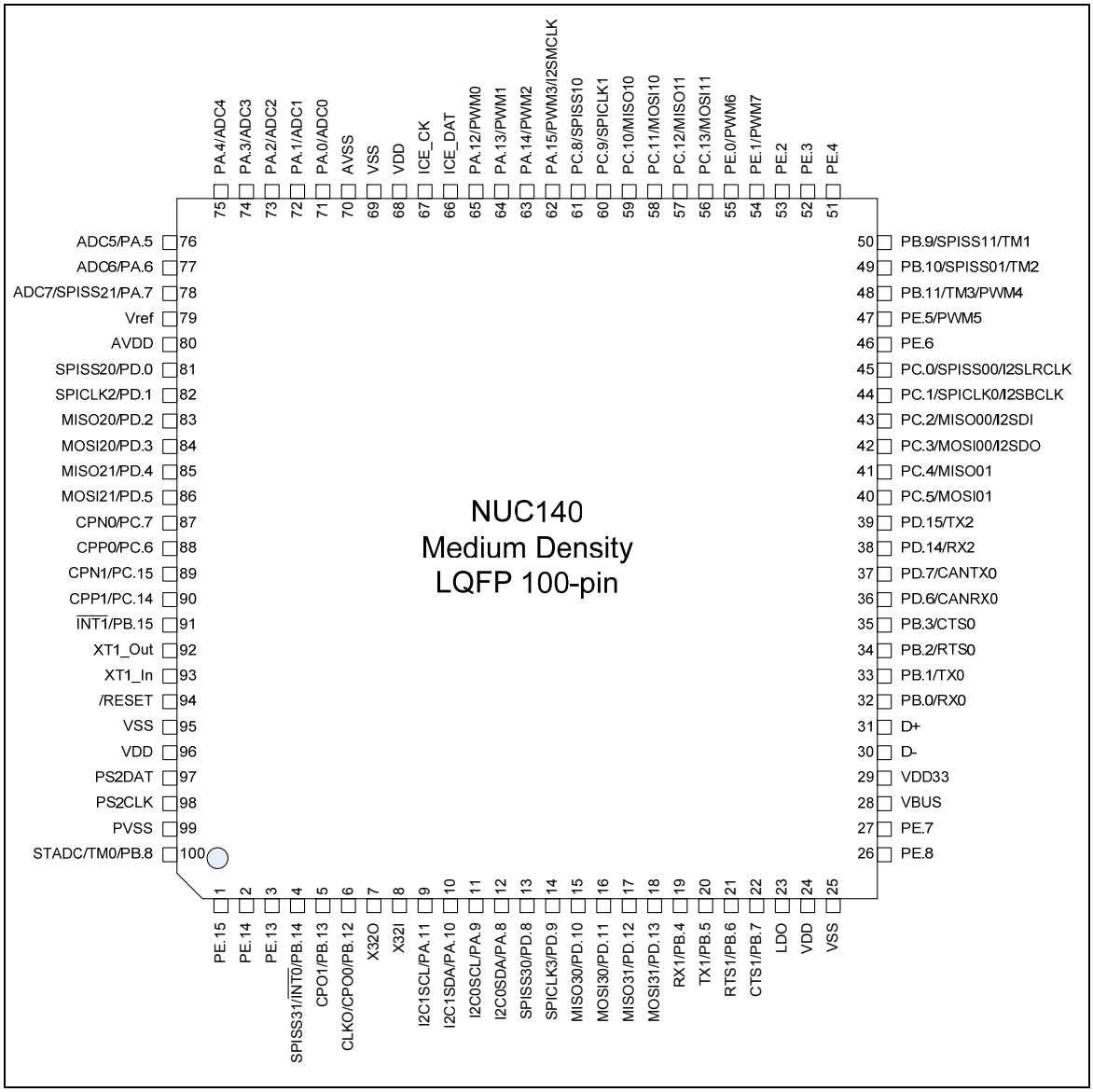


Figure 3-2 NuMicro™ NUC140 Medium Density LQFP 100-pin Pin Diagram

3.2.1.2 NuMicro™ NUC140 LQFP 64 pin

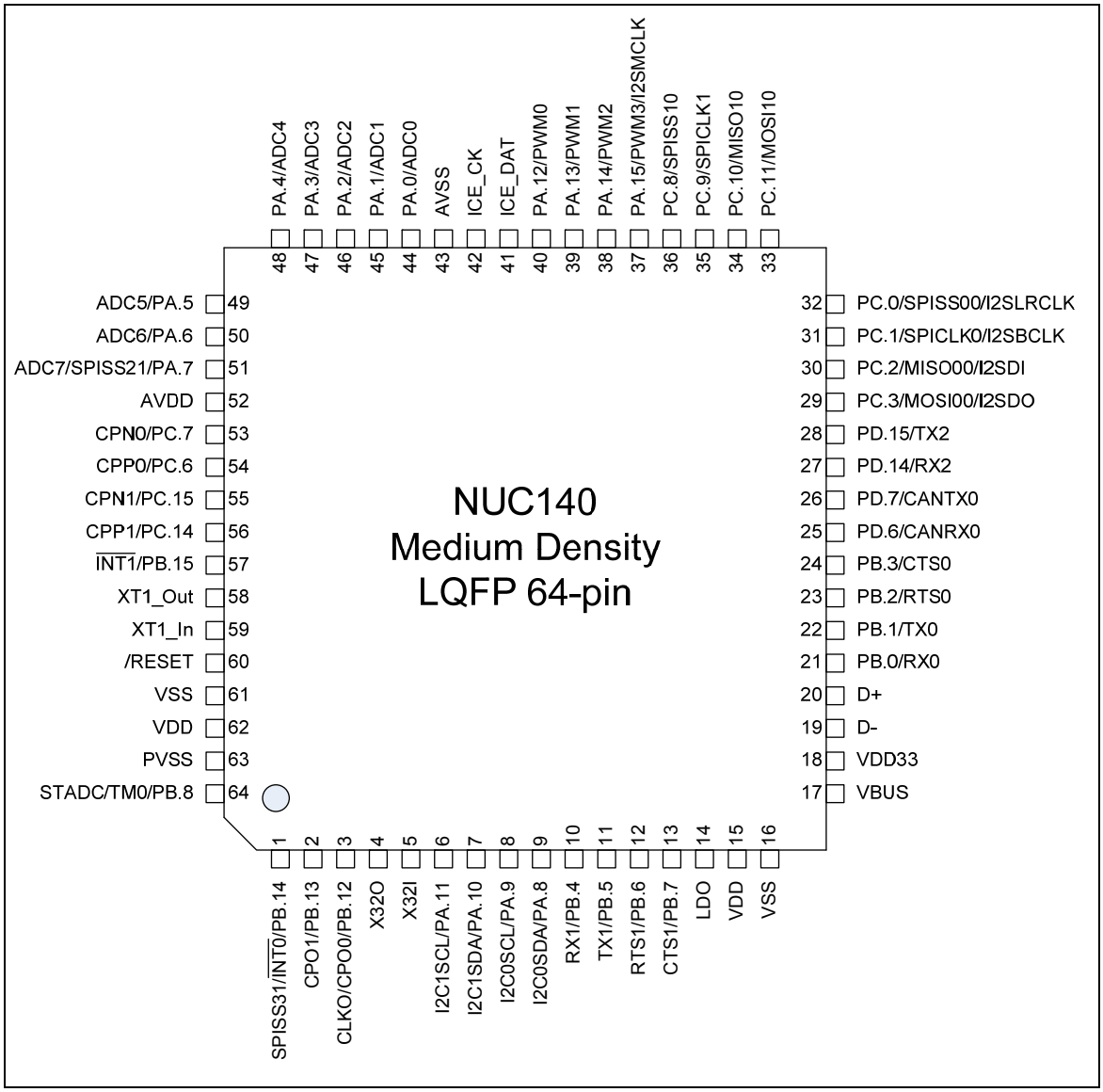


Figure 3-3 NuMicro™ NUC140 Medium Density LQFP 64-pin Pin Diagram

3.2.1.3 NuMicro™ NUC140 LQFP 48 pin

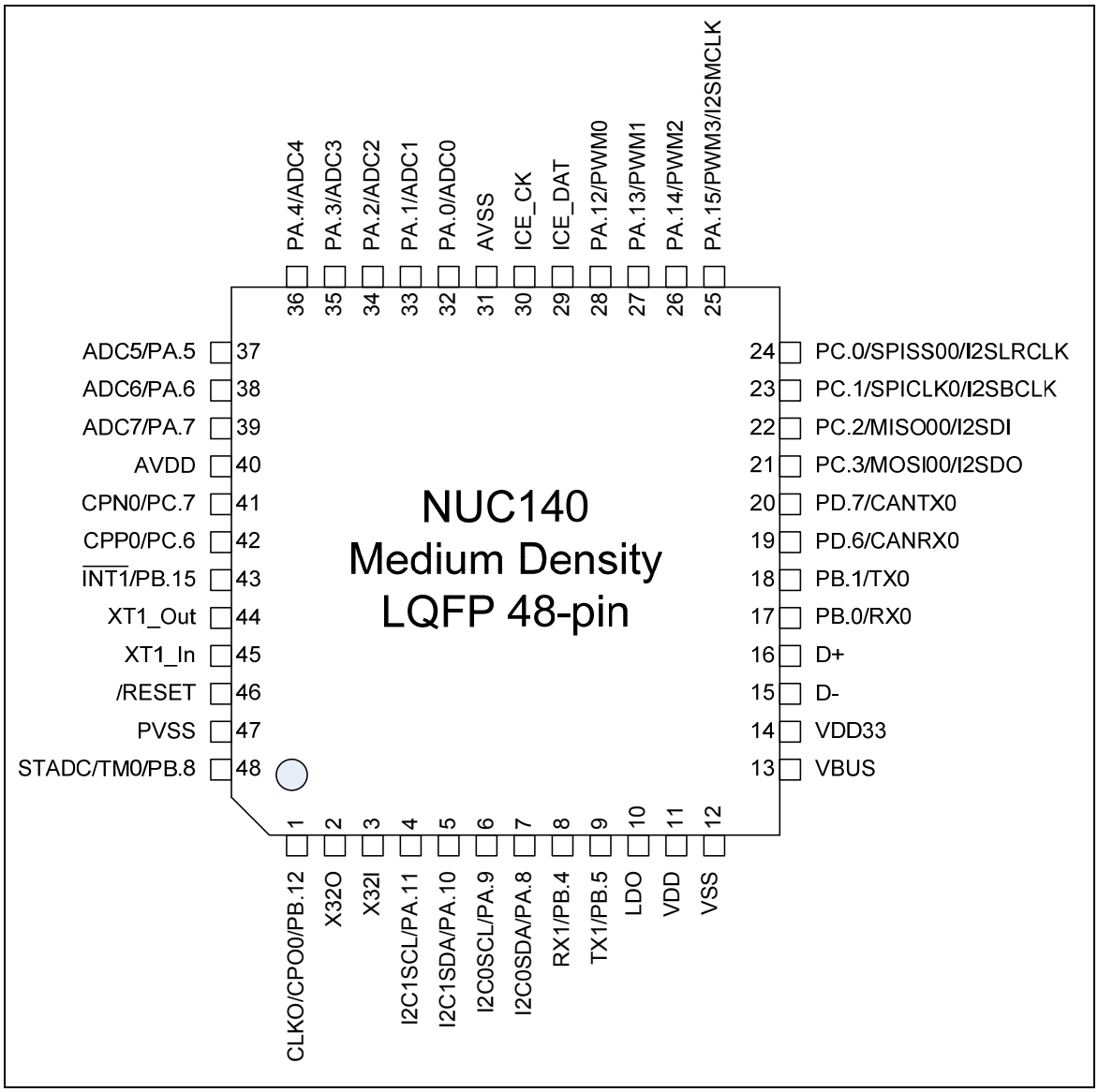


Figure 3-4 NuMicro™ NUC140 Medium Density LQFP 48-pin Pin Diagram

3.2.2 NuMicro™ NUC140 Low Density Pin Diagram

3.2.2.1 NuMicro™ NUC140 LQFP 64 pin

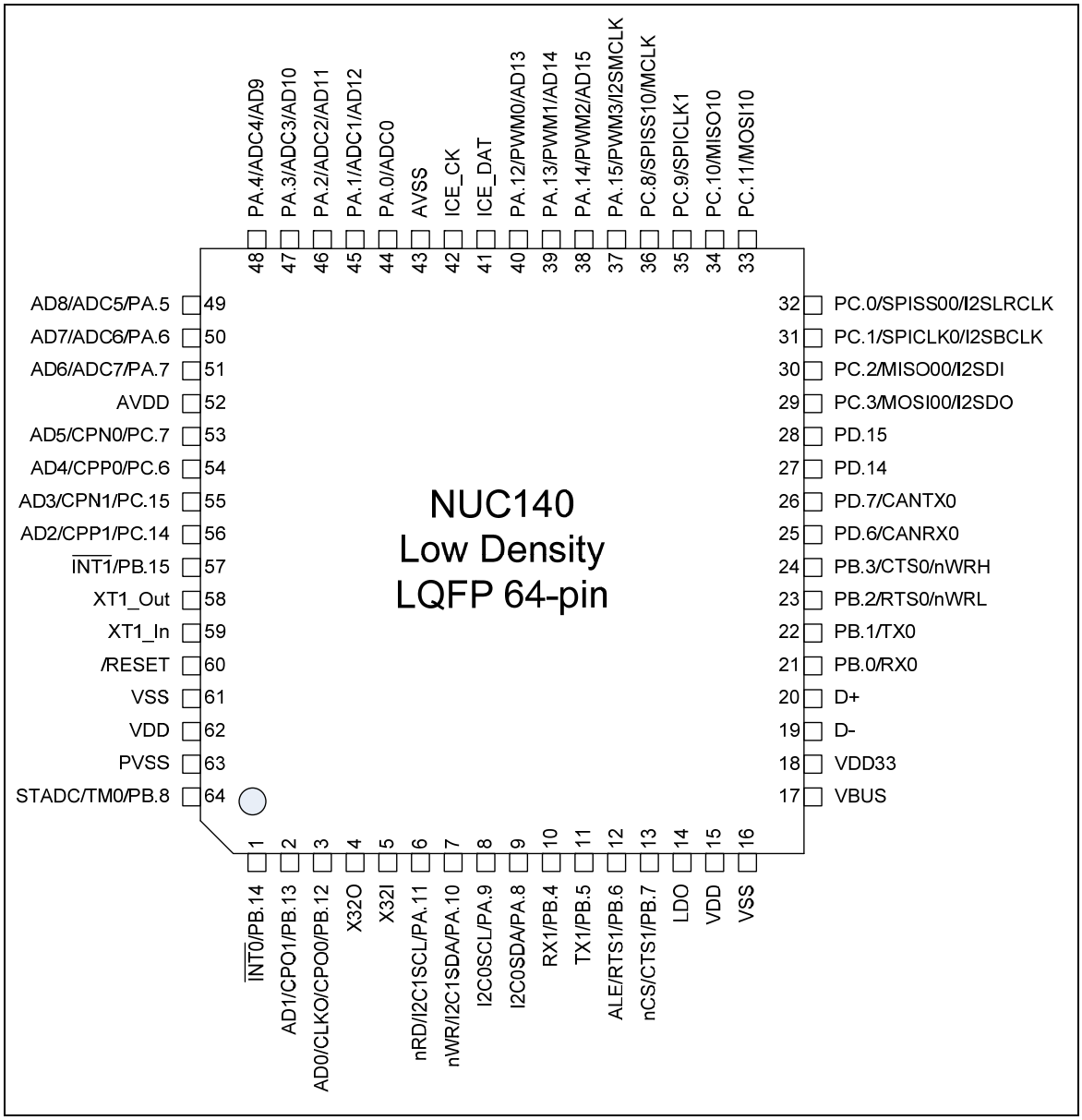


Figure 3-5 NuMicro™ NUC140 Low Density LQFP 64-pin Pin Diagram

3.2.2.2 NuMicro™ NUC140 LQFP 48 pin

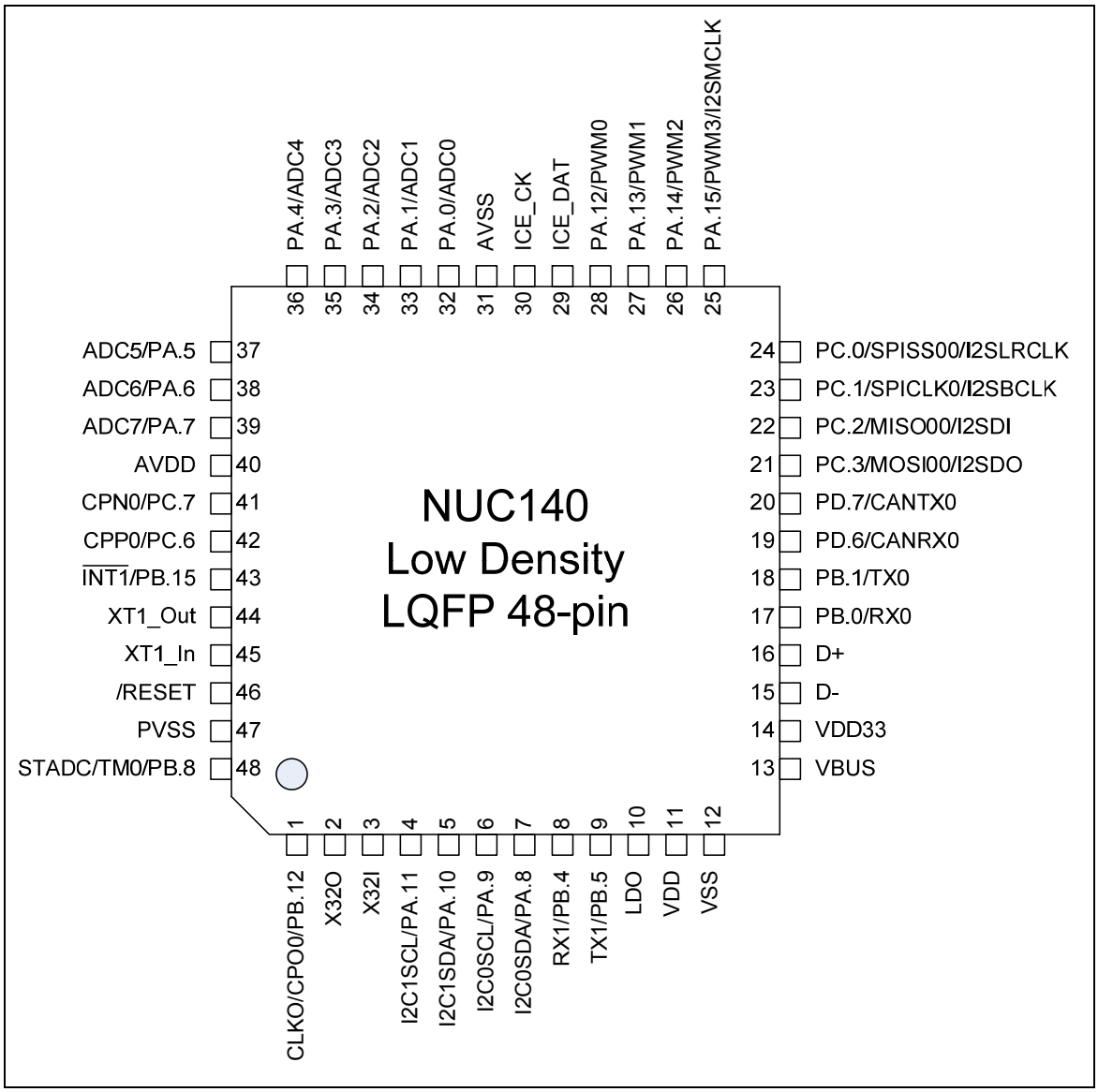


Figure 3-6 NuMicro™ NUC140 Low Density LQFP 48-pin Pin Diagram

3.3 Pin Description

3.3.1 NuMicro™ NUC140 Medium Density Pin Description

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
1			PE.15	**I/O**		General purpose input/output digital pin
2			PE.14	**I/O**		General purpose input/output digital pin
3			PE.13	**I/O**		General purpose input/output digital pin
4	1		PB.14	**I/O**		General purpose input/output digital pin
			/INT0	**I**		/INT0: External interrupt1 input pin
			SPISS31	**I/O**		SPISS31: SPI3 2nd slave select pin
5	2		PB.13	**I/O**		General purpose input/output digital pin
			CPO1	**O**		Comparator1 output pin
6	3	1	PB.12	**I/O**		General purpose input/output digital pin
			CPO0	**O**		Comparator0 output pin
			CLKO	**O**		Frequency Divider output pin
7	4	2	X32O	**O**		External 32.768 kHz crystal output pin
8	5	3	X32I	**I**		External 32.768 kHz crystal input pin
9	6	4	PA.11	**I/O**		General purpose input/output digital pin
			I2C1SCL	**I/O**		I2C1SCL: I^2C1 clock pin
10	7	5	PA.10	**I/O**		General purpose input/output digital pin
			I2C1SDA	**I/O**		I2C1SDA: I^2C1 data input/output pin
11	8	6	PA.9	**I/O**		General purpose input/output digital pin
			I2C0SCL	**I/O**		I2C0SCL: I^2C0 clock pin
12	9	7	PA.8	**I/O**		General purpose input/output digital pin
			I2C0SDA	**I/O**		I2C0SDA: I^2C0 data input/output pin
13			PD.8	**I/O**		General purpose input/output digital pin
			SPISS30	**I/O**		SPISS30: SPI3 slave select pin
14			PD.9	**I/O**		General purpose input/output digital pin
			SPICLK3	**I/O**		SPICLK3: SPI3 serial clock pin
15			PD.10	**I/O**		General purpose input/output digital pin
			MISO30	**I**		MISO30: SPI3 MISO (Master In, Slave Out) pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
16			PD.11	**I/O**		General purpose input/output digital pin
			MOSI30	**O**		MOSI30: SPI3 MOSI (Master Out, Slave In) pin
17			PD.12	**I/O**		General purpose input/output digital pin
			MISO31	**I**		MISO31: SPI3 2nd MISO (Master In, Slave Out) pin
18			PD.13	**I/O**		General purpose input/output digital pin
			MOSI31	**O**		MOSI31: SPI3 2nd MOSI (Master Out, Slave In) pin
19	10	8	PB.4	**I/O**		General purpose input/output digital pin
			RXD1	**I**		RXD1: Data receiver input pin for UART1
20	11	9	PB.5	**I/O**		General purpose input/output digital pin
			TXD1	**O**		TXD1: Data transmitter output pin for UART1
21	12		PB.6	**I/O**		General purpose input/output digital pin
			RTS1			RTS1: Request to Send output pin for UART1
22	13		PB.7	**I/O**		General purpose input/output digital pin
			CTS1			CTS1: Clear to Send input pin for UART1
23	14	10	LDO	**P**		LDO output pin
24	15	11	VDD	**P**		Power supply for I/O ports and LDO source for internal PLL and digital function
25	16	12	VSS	**P**		Ground
26			PE.8	**I/O**		General purpose input/output digital pin
27			PE.7	**I/O**		General purpose input/output digital pin
28	17	13	VBUS	**USB**		POWER SUPPLY: From USB Host or HUB.
29	18	14	VDD33	**USB**		Internal Power Regulator Output 3.3V Decoupling Pin
30	19	15	D-	**USB**		USB Differential Signal D-
31	20	16	D+	**USB**		USB Differential Signal D+
32	21	17	PB.0	**I/O**		General purpose input/output digital pin
			RXD0	**I**		RXD0: Data receiver input pin for UART0
33	22	18	PB.1	**I/O**		General purpose input/output digital pin
			TXD0	**O**		TXD0: Data transmitter output pin for UART0
34	23		PB.2	**I/O**		General purpose input/output digital pin
			RTS0			RTS0: Request to Send output pin for UART0

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
35	24		PB.3	I/O		General purpose input/output digital pin
			CTS0			CTS0: Clear to Send input pin for UART0
36	25	19	PD.6	I/O		General purpose input/output digital pin
			CANRX0	I		CAN Bus0 RX Input
37	26	20	PD.7	I/O		General purpose input/output digital pin
			CANTX0	O		CAN Bus0 TX Output
38	27		PD.14	I/O		General purpose input/output digital pin
			RXD2	I		RXD2: Data receiver input pin for UART2
39	28		PD.15	I/O		General purpose input/output digital pin
			TXD2	O		TXD2: Data transmitter output pin for UART2
40			PC.5	I/O		General purpose input/output digital pin
			MOSI01	O		MOSI01: SPI0 2nd MOSI (Master Out, Slave In) pin
41			PC.4	I/O		General purpose input/output digital pin
			MISO01	I		MISO01: SPI0 2nd MISO (Master In, Slave Out) pin
42	29	21	PC.3	I/O		General purpose input/output digital pin
			MOSI00	O		MOSI00: SPI0 MOSI (Master Out, Slave In) pin
			I2SDO	O		I2SDO: I2S data output
43	30	22	PC.2	I/O		General purpose input/output digital pin
			MISO00	I		MISO00: SPI0 MISO (Master In, Slave Out) pin
			I2SDI	I		I2SDI: I2S data input
44	31	23	PC.1	I/O		General purpose input/output digital pin
			SPICLK0	I/O		SPICLK0: SPI0 serial clock pin
			I2SBCLK	I/O		I2SBCLK: I2S bit clock pin
45	32	24	PC.0	I/O		General purpose input/output digital pin
			SPISS00	I/O		SPISS00: SPI0 slave select pin
			I2SLRCLK	I/O		I2SLRCLK: I2S left right channel clock
46			PE.6	I/O		General purpose input/output digital pin
47			PE.5	I/O		General purpose input/output digital pin
			PWM5	O		PWM5: PWM output

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
48			PB.11	I/O		General purpose input/output digital pin
			TM3	O		TM3: Timer3 external counter input
			PWM4	O		PWM4: PWM output
49			PB.10	I/O		General purpose input/output digital pin
			TM2	O		TM2: Timer2 external counter input
			SPISS01	I/O		SPISS01: SPI0 2nd slave select pin
50			PB.9	I/O		General purpose input/output digital pin
			TM1	O		TM1: Timer1 external counter input
			SPISS11	I/O		SPISS11: SPI1 2nd slave select pin
51			PE.4	I/O		General purpose input/output digital pin
52			PE.3	I/O		General purpose input/output digital pin
53			PE.2	I/O		General purpose input/output digital pin
54			PE.1	I/O		General purpose input/output digital pin
			PWM7	O		PWM7: PWM output
55			PE.0	I/O		General purpose input/output digital pin
			PWM6	O		PWM6: PWM output
56			PC.13	I/O		General purpose input/output digital pin
			MOSI11	O		MOSI11: SPI1 2nd MOSI (Master Out, Slave In) pin
57			PC.12	I/O		General purpose input/output digital pin
			MISO11	I		MISO11: SPI1 2nd MISO (Master In, Slave Out) pin
58	33		PC.11	I/O		General purpose input/output digital pin
			MOSI10	O		MOSI10: SPI1 MOSI (Master Out, Slave In) pin
59	34		PC.10	I/O		General purpose input/output digital pin
			MISO10	I		MISO10: SPI1 MISO (Master In, Slave Out) pin
60	35		PC.9	I/O		General purpose input/output digital pin
			SPICLK1	I/O		SPICLK1: SPI1 serial clock pin
61	36		PC.8	I/O		General purpose input/output digital pin
			SPISS10	I/O		SPISS10: SPI1 slave select pin
62	37	25	PA.15	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			PWM3	O		PWM3: PWM output pin
			I2SMCLK	O		I2SMCLK: I^2S master clock output pin
63	38	26	PA.14	I/O		General purpose input/output digital pin
			PWM2	O		PWM2: PWM output
64	39	27	PA.13	I/O		General purpose input/output digital pin
			PWM1	O		PWM1: PWM output
65	40	28	PA.12	I/O		General purpose input/output digital pin
			PWM0	O		PWM0: PWM output
66	41	29	ICE_DAT	I/O		Serial Wired Debugger Data pin
67	42	30	ICE_CK	I		Serial Wired Debugger Clock pin
68			VDD	P		Power supply for I/O ports and LDO source for internal PLL and digital circuit
69			VSS	P		Ground
70	43	31	AVSS	AP		Ground Pin for analog circuit
71	44	32	PA.0	I/O		General purpose input/output digital pin
			ADC0	AI		ADC0: ADC analog input
72	45	33	PA.1	I/O		General purpose input/output digital pin
			ADC1	AI		ADC1: ADC analog input
73	46	34	PA.2	I/O		General purpose input/output digital pin
			ADC2	AI		ADC2: ADC analog input
74	47	35	PA.3	I/O		General purpose input/output digital pin
			ADC3	AI		ADC3: ADC analog input
75	48	36	PA.4	I/O		General purpose input/output digital pin
			ADC4	AI		ADC4: ADC analog input
76	49	37	PA.5	I/O		General purpose input/output digital pin
			ADC5	AI		ADC5: ADC analog input
77	50	38	PA.6	I/O		General purpose input/output digital pin
			ADC6	AI		ADC6: ADC analog input
78	51	39	PA.7	I/O		General purpose input/output digital pin
			ADC7	AI		ADC7: ADC analog input
			SPISS21	I/O		SPISS21: SPI2 2nd slave select pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
79			Vref	**AP**		Voltage reference input for ADC
80	52	40	AVDD	**AP**		Power supply for internal analog circuit
81			PD.0	**I/O**		General purpose input/output digital pin
			SPISS20	**I/O**		SPISS20: SPI2 slave select pin
82			PD.1	**I/O**		General purpose input/output digital pin
			SPICLK2	**I/O**		SPICLK2: SPI2 serial clock pin
83			PD.2	**I/O**		General purpose input/output digital pin
			MISO20	**I**		MISO20: SPI2 MISO (Master In, Slave Out) pin
84			PD.3	**I/O**		General purpose input/output digital pin
			MOSI20	**O**		MOSI20: SPI2 MOSI (Master Out, Slave In) pin
85			PD.4	**I/O**		General purpose input/output digital pin
			MISO21	**I**		MISO21: SPI2 2nd MISO (Master In, Slave Out) pin
86			PD.5	**I/O**		General purpose input/output digital pin
			MOSI21	**O**		MOSI21: SPI2 2nd MOSI (Master Out, Slave In) pin
87	53	41	PC.7	**I/O**		General purpose input/output digital pin
			CPN0	**I**		CPN0: Comparator0 Negative input pin
88	54	42	PC.6	**I/O**		General purpose input/output digital pin
			CPP0	**I**		CPP0: Comparator0 Positive input pin
89	55		PC.15	**I/O**		General purpose input/output digital pin
			CPN1	**I**		CPN1: Comparator1 Negative input pin
90	56		PC.14	**I/O**		General purpose input/output digital pin
			CPP1	**I**		CPP1: Comparator1 Positive input pin
91	57	43	PB.15	**I/O**		General purpose input/output digital pin
			/INT1	**I**		/INT1: External interrupt0 input pin
92	58	44	XT1_OUT	**O**		External 4~24 MHz crystal output pin
93	59	45	XT1_IN	**I**		External 4~24 MHz crystal input pin
94	60	46	/RESET	**I**		External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
95	61		VSS	**P**		Ground
96	62		VDD	**P**		Power supply for I/O ports and LDO source for internal PLL and digital circuit

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
97			PS2DAT	**I/O**		PS2 Data pin
98			PS2CLK	**I/O**		PS2 clock pin
99	63	47	PVSS	**P**		PLL Ground
100	64	48	PB.8	**I/O**		General purpose input/output digital pin
			STADC	**I**		STADC: ADC external trigger input.
			TM0	**O**		TM0: Timer0 external counter input

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

3.3.2 NuMicro™ NUC140 Low Density Pin Description

Pin No.		Pin Name	Pin Type		Description
LQFP 64	LQFP 48				
1		PB.14	I/O		General purpose input/output digital pin
		/INT0	I		/INT0: External interrupt1 input pin
2		PB.13	I/O		General purpose input/output digital pin
		CPO1	O		Comparator1 output pin
		AD1	I/O		EBI Address/Data bus bit1 (64pin package only)
3	1	PB.12	I/O		General purpose input/output digital pin
		CPO0	O		Comparator0 output pin
		CLKO	O		Frequency Divider output pin
		AD0	I/O		EBI Address/Data bus bit0 (64pin package only)
4	2	X32O	O		External 32.768 kHz crystal output pin
5	3	X32I	I		External 32.768 kHz crystal input pin
6	4	PA.11	I/O		General purpose input/output digital pin
		I2C1SCL	I/O		I2C1SCL: I^2C1 clock pin
		nRD	O		EBI read enable output pin (64pin package only)
7	5	PA.10	I/O		General purpose input/output digital pin
		I2C1SDA	I/O		I2C1SDA: I^2C1 data input/output pin
		nWR	O		EBI write enable output pin (64pin package only)
8	6	PA.9	I/O		General purpose input/output digital pin
		I2C0SCL	I/O		I2C0SCL: I^2C0 clock pin
9	7	PA.8	I/O		General purpose input/output digital pin
		I2C0SDA	I/O		I2C0SDA: I^2C0 data input/output pin
10	8	PB.4	I/O		General purpose input/output digital pin
		RXD1	I		RXD1: Data receiver input pin for UART1
11	9	PB.5	I/O		General purpose input/output digital pin
		TXD1	O		TXD1: Data transmitter output pin for UART1
12		PB.6	I/O		General purpose input/output digital pin
		RTS1			RTS1: Request to Send output pin for UART1
		ALE	O		EBI address latch enable output pin (64pin

Pin No.		Pin Name	Pin Type		Description
LQFP 64	LQFP 48				
					package only)
13		PB.7	I/O		General purpose input/output digital pin
		CTS1			CTS1: Clear to Send input pin for UART1
		nCS	O		EBI chip select enable output pin (64pin package only)
14	10	LDO	P		LDO output pin
15	11	VDD	P		Power supply for I/O ports and LDO source for internal PLL and digital function
16	12	VSS	P		Ground
17	13	VBUS	USB		POWER SUPPLY: From USB Host or HUB.
18	14	VDD33	USB		Internal Power Regulator Output 3.3V Decoupling Pin
19	15	D-	USB		USB Differential Signal D-
20	16	D+	USB		USB Differential Signal D+
21	17	PB.0	I/O		General purpose input/output digital pin
		RXD0	I		RXD0: Data receiver input pin for UART0
22	18	PB.1	I/O		General purpose input/output digital pin
		TXD0	O		TXD0: Data transmitter output pin for UART0
23		PB.2	I/O		General purpose input/output digital pin
		RTS0			RTS0: Request to Send output pin for UART0
		nWRL	O		EBI low byte write enable output pin (64pin package only)
24		PB.3	I/O		General purpose input/output digital pin
		CTS0			CTS0: Clear to Send input pin for UART0
		nWRH	O		EBI high byte write enable output pin (64pin package only)
25	19	PD.6	I/O		General purpose input/output digital pin
		CANRX0	I		CAN Bus0 RX Input
26	20	PD.7	I/O		General purpose input/output digital pin
		CANTX0	O		CAN Bus0 TX Output
27		PD.14	I/O		General purpose input/output digital pin
28		PD.15	I/O		General purpose input/output digital pin

Pin No.		Pin Name	Pin Type		Description
LQFP 64	LQFP 48				
29	21	PC.3	I/O		General purpose input/output digital pin
		MOSI00	O		MOSI00: SPI0 MOSI (Master Out, Slave In) pin
		I2SDO	O		I2SDO: I^2S data output
30	22	PC.2	I/O		General purpose input/output digital pin
		MISO00	I		MISO00: SPI0 MISO (Master In, Slave Out) pin
		I2SDI	I		I2SDI: I^2S data input
31	23	PC.1	I/O		General purpose input/output digital pin
		SPICLK0	I/O		SPICLK0: SPI0 serial clock pin
		I2SBCLK	I/O		I2SBCLK: I^2S bit clock pin
32	24	PC.0	I/O		General purpose input/output digital pin
		SPISS00	I/O		SPISS00: SPI0 slave select pin
		I2SLRCLK	I/O		I2SLRCLK: I^2S left right channel clock
33		PC.11	I/O		General purpose input/output digital pin
		MOSI10	O		MOSI10: SPI1 MOSI (Master Out, Slave In) pin
34		PC.10	I/O		General purpose input/output digital pin
		MISO10	I		MISO10: SPI1 MISO (Master In, Slave Out) pin
35		PC.9	I/O		General purpose input/output digital pin
		SPICLK1	I/O		SPICLK1: SPI1 serial clock pin
36		PC.8	I/O		General purpose input/output digital pin
		SPISS10	I/O		SPISS10: SPI1 slave select pin
		MCLK	O		EBI external clock output pin (64pin package only)
37	25	PA.15	I/O		General purpose input/output digital pin
		PWM3	O		PWM3: PWM output pin
		I2SMCLK	O		I2SMCLK: I^2S master clock output pin
38	26	PA.14	I/O		General purpose input/output digital pin
		PWM2	O		PWM2: PWM output
		AD15	I/O		EBI Address/Data bus bit15 (64pin package only)
39	27	PA.13	I/O		General purpose input/output digital pin
		PWM1	O		PWM1: PWM output
		AD14	I/O		EBI Address/Data bus bit14 (64pin package only)

Pin No.		Pin Name	Pin Type		Description
LQFP 64	LQFP 48				
40	28	PA.12	I/O		General purpose input/output digital pin
		PWM0	O		PWM0: PWM output
		AD13	I/O		EBI Address/Data bus bit13 (64pin package only)
41	29	ICE_DAT	I/O		Serial Wired Debugger Data pin
42	30	ICE_CK	I		Serial Wired Debugger Clock pin
43	31	AVSS	AP		Ground Pin for analog circuit
44	32	PA.0	I/O		General purpose input/output digital pin
		ADC0	AI		ADC0: ADC analog input
45	33	PA.1	I/O		General purpose input/output digital pin
		ADC1	AI		ADC1: ADC analog input
		AD12	I/O		EBI Address/Data bus bit12 (64pin package only)
46	34	PA.2	I/O		General purpose input/output digital pin
		ADC2	AI		ADC2: ADC analog input
		AD11	I/O		EBI Address/Data bus bit11 (64pin package only)
47	35	PA.3	I/O		General purpose input/output digital pin
		ADC3	AI		ADC3: ADC analog input
		AD10	I/O		EBI Address/Data bus bit10 (64pin package only)
48	36	PA.4	I/O		General purpose input/output digital pin
		ADC4	AI		ADC4: ADC analog input
		AD9	I/O		EBI Address/Data bus bit9 (64pin package only)
49	37	PA.5	I/O		General purpose input/output digital pin
		ADC5	AI		ADC5: ADC analog input
		AD8	I/O		EBI Address/Data bus bit8 (64pin package only)
50	38	PA.6	I/O		General purpose input/output digital pin
		ADC6	AI		ADC6: ADC analog input
		AD7	I/O		EBI Address/Data bus bit7 (64pin package only)
51	39	PA.7	I/O		General purpose input/output digital pin
		ADC7	AI		ADC7: ADC analog input
		AD6	I/O		EBI Address/Data bus bit6 (64pin package only)
52	40	AVDD	AP		Power supply for internal analog circuit

Pin No.		Pin Name	Pin Type		Description
LQFP 64	LQFP 48				
53	41	PC.7	**I/O**		General purpose input/output digital pin
		CPN0	**I**		CPN0: Comparator0 Negative input pin
		AD5	**I/O**		EBI Address/Data bus bit5 (64pin package only)
54	42	PC.6	**I/O**		General purpose input/output digital pin
		CPP0	**I**		CPP0: Comparator0 Positive input pin
		AD4	**I/O**		EBI Address/Data bus bit4 (64pin package only)
55		PC.15	**I/O**		General purpose input/output digital pin
		CPN1	**I**		CPN1: Comparator1 Negative input pin
		AD3	**I/O**		EBI Address/Data bus bit3 (64pin package only)
56		PC.14	**I/O**		General purpose input/output digital pin
		CPP1	**I**		CPP1: Comparator1 Positive input pin
		AD2	**I/O**		EBI Address/Data bus bit2 (64pin package only)
57	43	PB.15	**I/O**		General purpose input/output digital pin
		/INT1	**I**		/INT1: External interrupt0 input pin
58	44	XT1_OUT	**O**		External 4~24 MHz crystal output pin
59	45	XT1_IN	**I**		External 4~24 MHz crystal input pin
60	46	/RESET	**I**		External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
61		VSS	**P**		Ground
62		VDD	**P**		Power supply for I/O ports and LDO source for internal PLL and digital circuit
63	47	PVSS	**P**		PLL Ground
64	48	PB.8	**I/O**		General purpose input/output digital pin
		STADC	**I**		STADC: ADC external trigger input.
		TM0	**O**		TM0: Timer0 external counter input

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC140 Medium Density Block Diagram

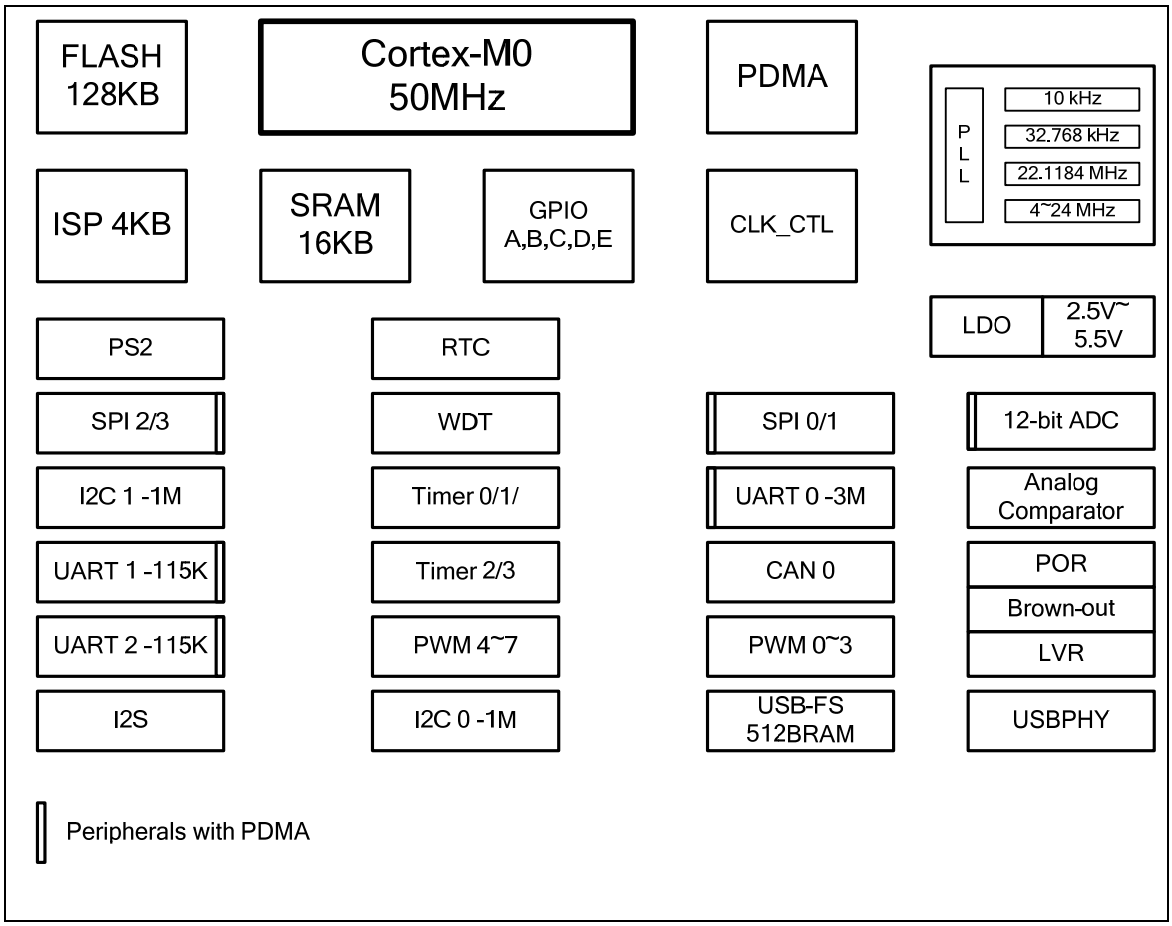


Figure 4-1 NuMicro™ NUC140 Medium Density Block Diagram

4.2 NuMicro™ NUC140 Low Density Block Diagram

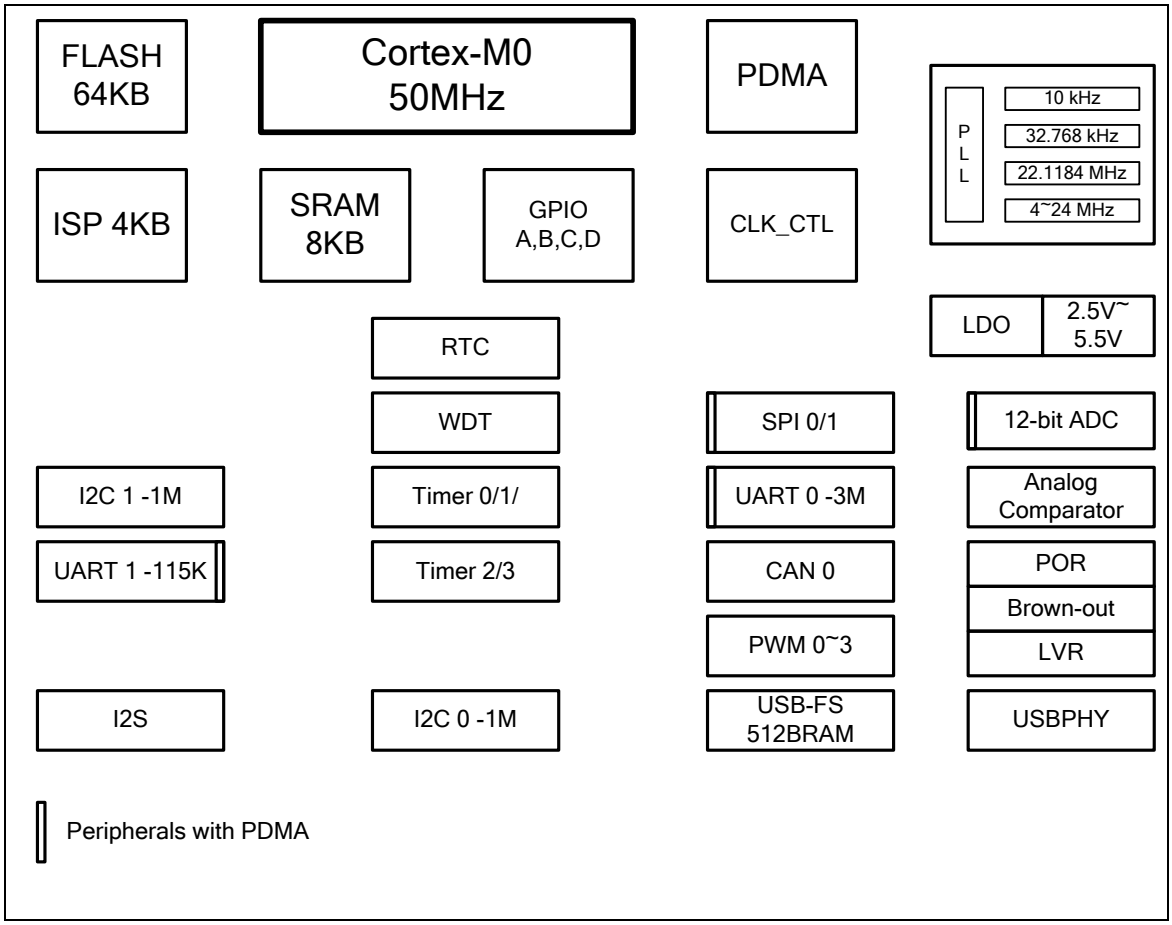


Figure 4-2 NuMicro™ NUC140 Low Density Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 5-1 shows the functional controller of processor.

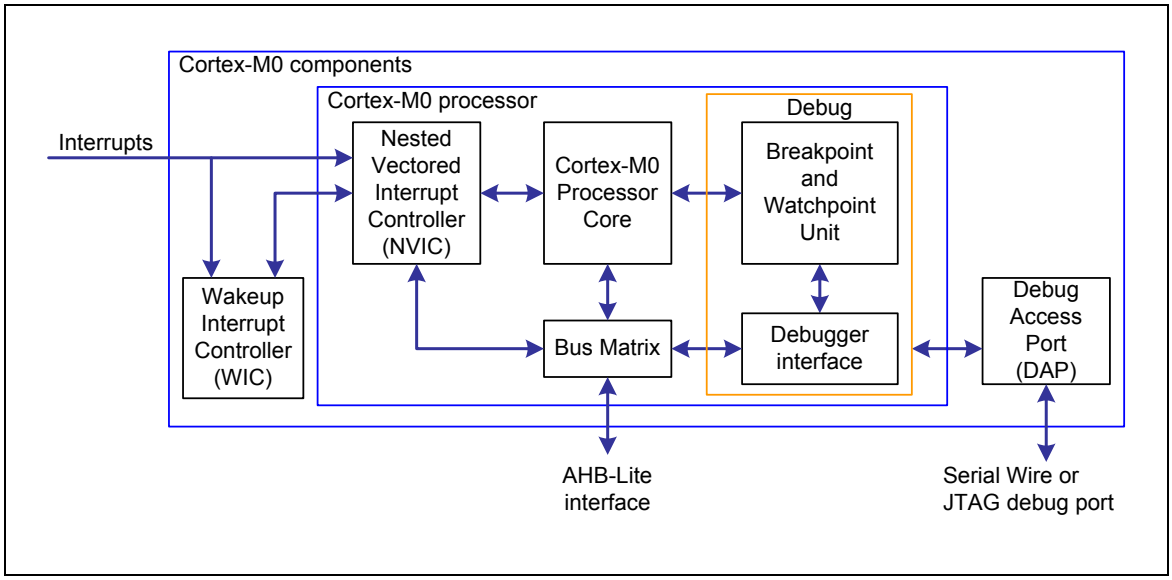


Figure 5-1 Functional Controller Diagram

The implemented device provides:

- A low gate count processor that features:
  - The ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - The system interface supports little-endian data accesses
  - The ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature

- NVIC that features:

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.

- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2 System Manager

5.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)

5.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Brown-Out Detector Reset
- CPU Reset
- System Reset

System Reset and Power-On Reset all reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external crystal circuit and ISPCON.BS bit. System Reset doesn't reset external crystal circuit and ISPCON.BS bit, but Power-On Reset does.

5.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog components operation.
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 2.5V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver. (For NuMicro™ NUC120/NUC140 Only)

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Figure 5-2 shows the power distribution of NuMicro™ NUC120/NUC140 and Figure 5-3 shows the power distribution of NuMicro™ NUC100/ NUC130

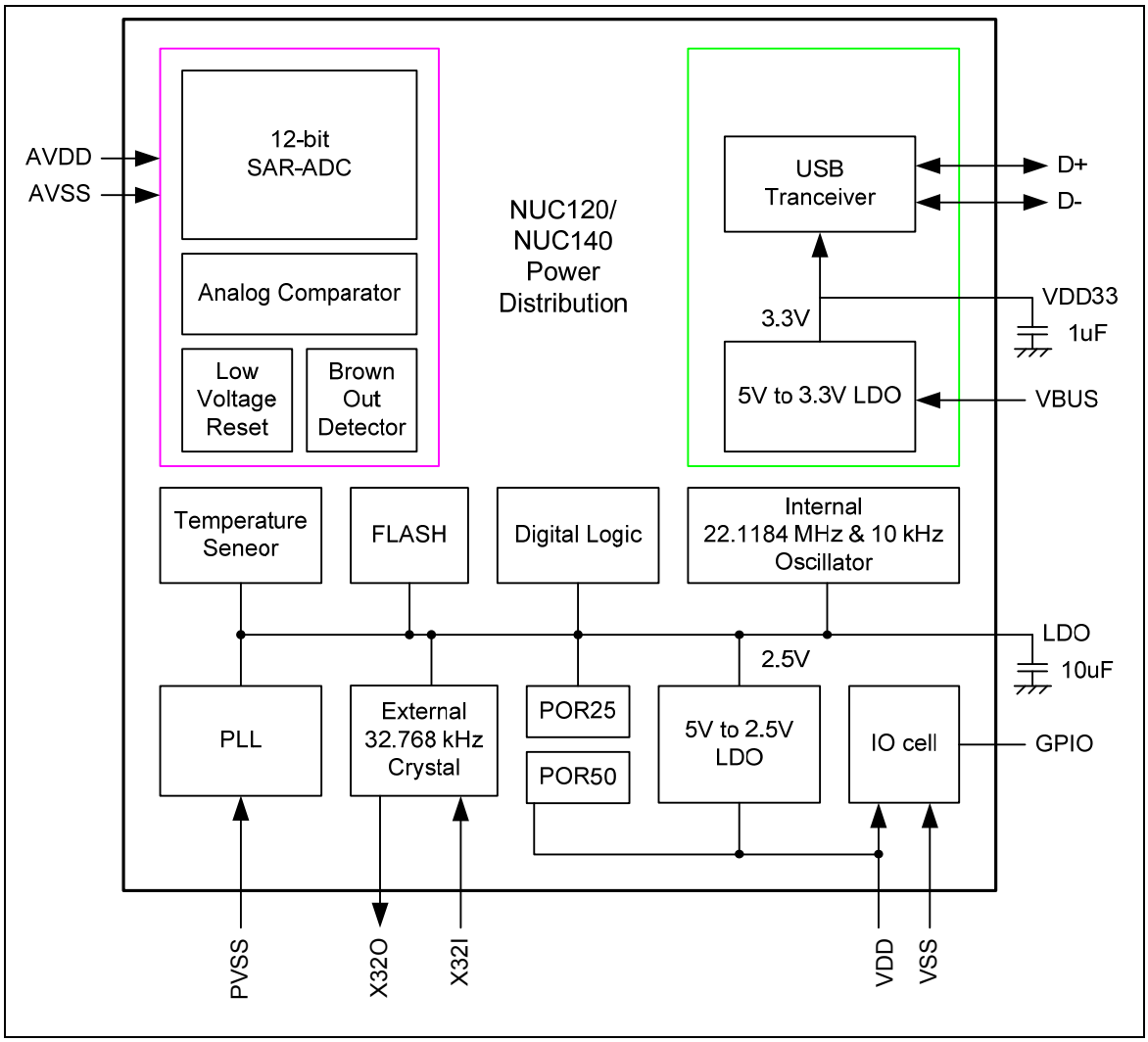


Figure 5-2 NuMicro™ NUC120/NUC140 Power Distribution Diagram

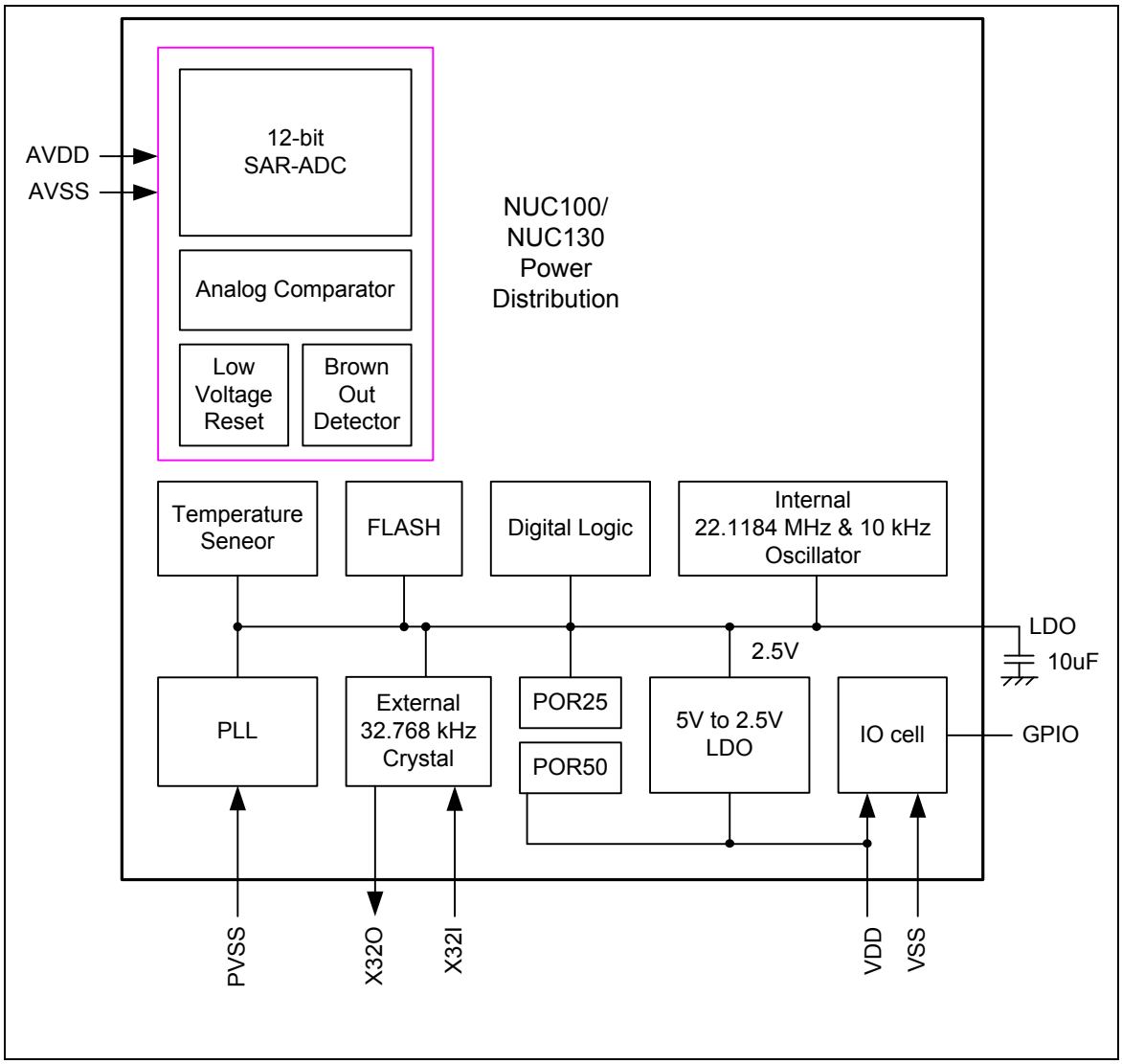


Figure 5-3 NuMicro™ NUC100/ NUC130 Power Distribution Diagram

5.2.4 System Memory Map

NuMicro™ NUC100 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in the following table. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. NuMicro™ NUC100 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash & SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 – 0x6001_FFFF	EXTMEM_BA	External Memory Space (128KB) (Low Density 64-pin Only)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers (Low Density 64-pin Only)
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers

0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400D_0000 – 0x400D_3FFF	ACMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4013_0000 – 0x4013_3FFF	SPI2_BA	SPI2 with master/slave function Control Registers (Medium Density Only)
0x4013_4000 – 0x4013_7FFF	SPI3_BA	SPI3 with master/slave function Control Registers (Medium Density Only)
0x4014_0000 – 0x4014_3FFF	PWMB_BA	PWM4/5/6/7 Control Registers (Medium Density Only)
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_7FFF	UART2_BA	UART2 Control Registers (Medium Density Only)
0x4018_0000 – 0x4018_3FFF	CAN0_BA	CAN0 Bus Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I^2S Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 5-1 Address Space Assignments for On-Chip Controllers

5.2.5 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

5.2.6 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.3 Clock Controller

5.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power-down mode and wait for wake-up interrupt source triggered to leave power-down mode. In the power down mode, the clock controller turns off the external 4~24 MHz crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

5.3.2 Clock Generator

The clock generator consists of 5 clock sources which are listed below:

- One external 32.768 kHz crystal
- One external 4~24 MHz crystal
- One programmable PLL FOUT(PLL source consists of external 4~24 MHz crystal and internal 22.1184 MHz oscillator)
- One internal 22.1184 MHz oscillator
- One internal 10 kHz oscillator

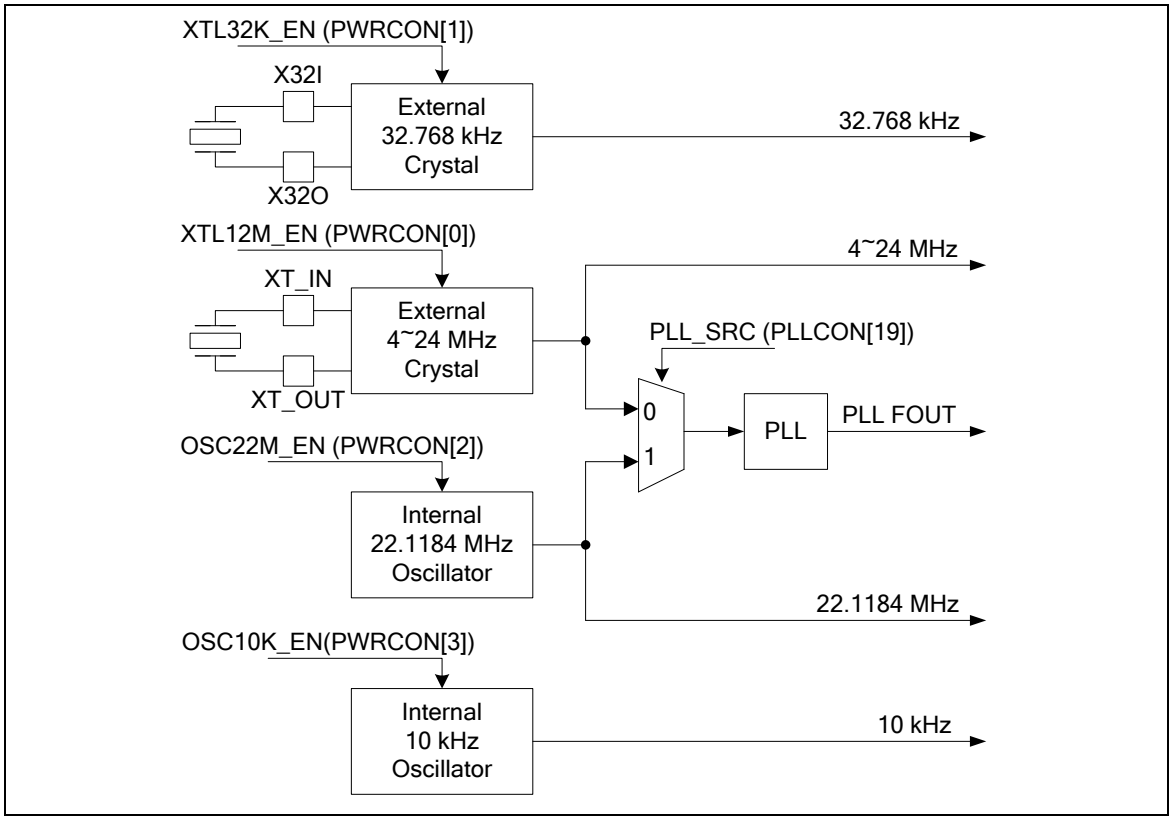


Figure 5-4 Clock generator block diagram

5.3.3 System Clock & SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is showed in Figure 5-5.

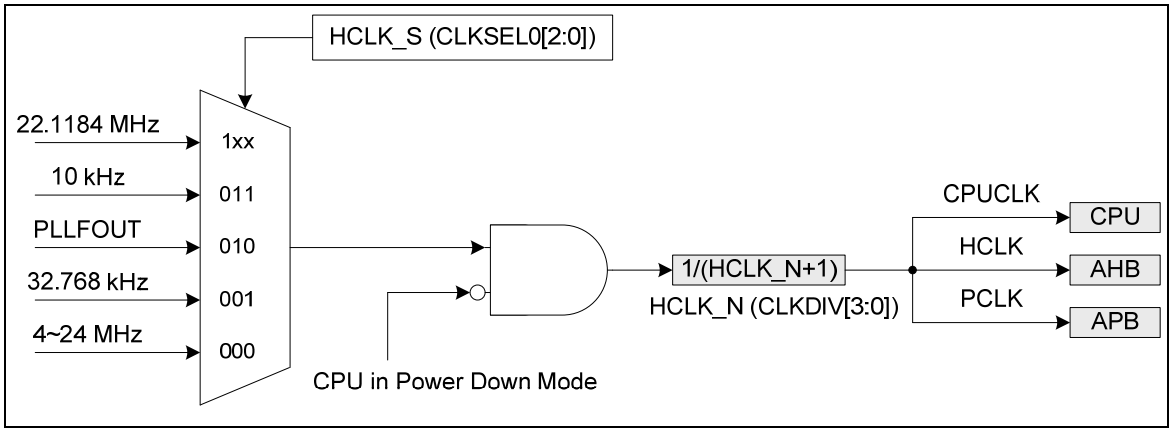


Figure 5-5 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is showed in Figure 5-6.

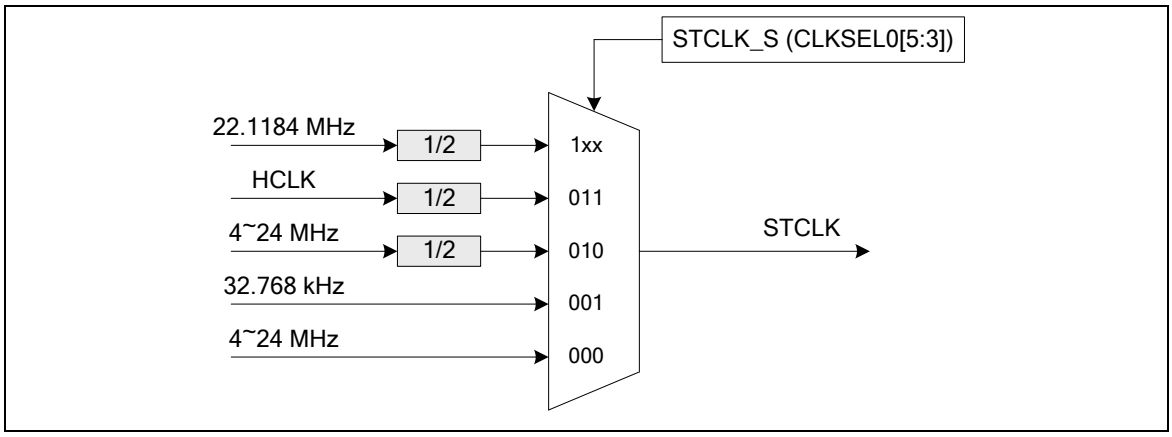


Figure 5-6 SysTick Clock Control Block Diagram

5.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting which depends on the different peripheral. Please refer the CLKSEL1 and CLKSEL2 register description.

5.3.5 Power down mode (Deep Sleep Mode) Clock

When chip enters into power down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in power down mode.

For theses clocks which still keep active list below:

- Clock Generator
  - Internal 10 kHz oscillator clock
  - External 32.768 kHz crystal clock
- Peripherals Clock (When these IP adopt 32.768 kHz or 10 kHz as clock source)

5.3.6 Frequency Divider Output

This device is equipped a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When write 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When write 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

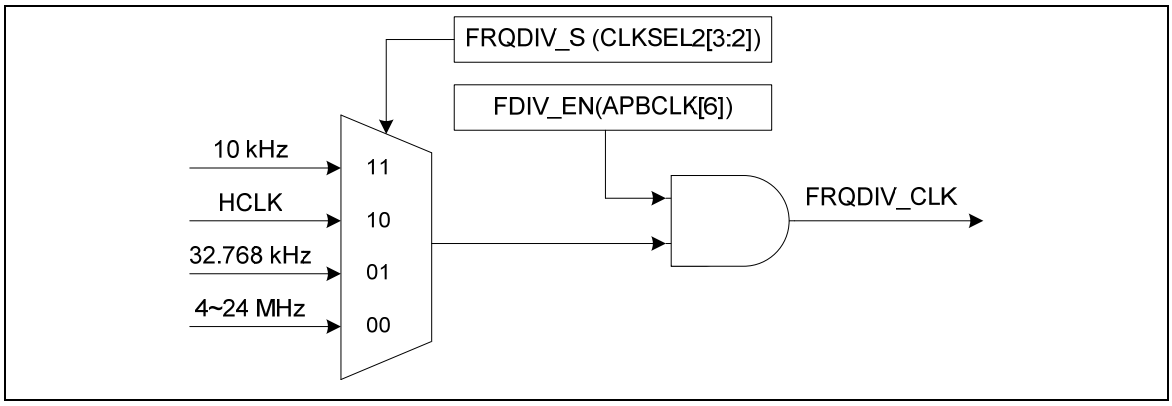


Figure 5-7 Clock Source of Frequency Divider

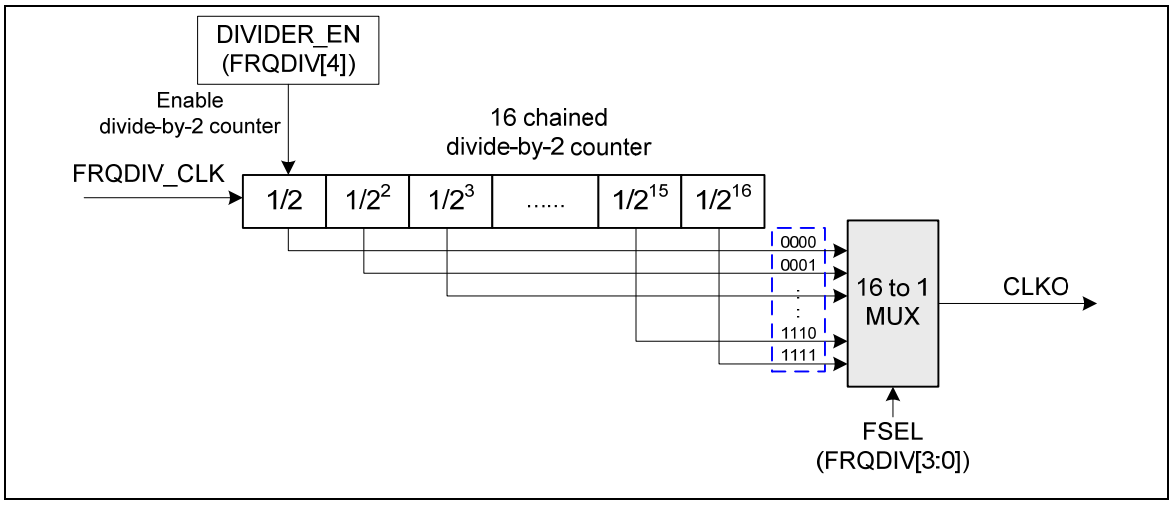


Figure 5-8 Block Diagram of Frequency Divider

5.4 USB Device Controller (USB)

5.4.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. Users need to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (BUFSEGx)”.

This device controller contains 6 configurable endpoints. Each endpoint can be configured as IN, OUT, or SETUP packet type. The function address of the device and endpoint number in each endpoint shall be configured properly in advance for receive or transmit a data packet. The transmit/receive length in each endpoint is defined in maximum payload register (MXPLDx) and the handshakes between Host and Device are handled in it.

There are four different interrupt events in this controller. They are the wake up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also support for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

Reference: Universal Serial Bus Specification Revision 1.1

5.4.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature listing of this USB.

- Compliant with USB 2.0 Full-Speed specification
- Provide 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Support Control/Bulk/Interrupt/Isochronous transfer type
- Support suspend function when no bus activity existing for 3 ms
- Provide 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provide remote wakeup capability

5.5 General Purpose I/O

5.5.1 Overview

NuMicro™ NUC100 Series Medium Density has up to 80 General Purpose I/O pins can be shared with other function pins; it depends on the chip configuration. These 80 pins are arranged in 5 ports named with GPIOA, GPIOB, GPIOC, GPIOD and GPIOE. Each port equips maximum 16 pins. Each one of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

NuMicro™ NUC100 Series Low Density has up to 65 General Purpose I/O pins can be shared with other function pins; it depends on the chip configuration and package. These 65 pins are arranged in 4 ports named with GPIOA, GPIOB, GPIOC and GPIOD with each port equips maximum 16 pins and another port named GPIOE with 1 pins PE.5.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or quasi-bidirectional mode. After reset, the I/O type of all pins stay in quasi-bidirectional mode and port data register GPIOx_DOUT[15:0] resets to 0x0000_FFFF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} is from 5.0V to 2.5V.

5.5.2 Features

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- High driver and high sink IO mode support

5.6 I²C Serial Interface Controller (Master/Slave) (I²C)

5.6.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up 1.0 Mbps.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the Figure 5-9 for more detail I²C BUS Timing.

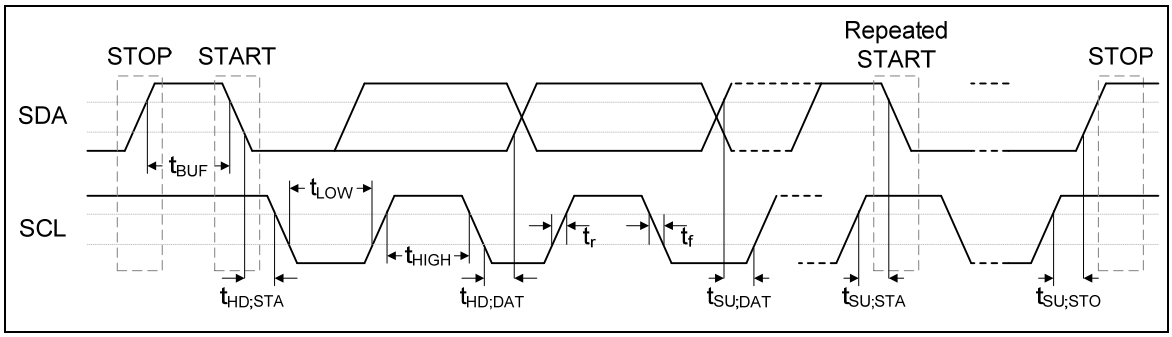


Figure 5-9 I²C Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

5.6.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave up to 1Mbit/s
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- External pull-up are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- I²C-bus controllers support multiple address recognition (Four slave address with mask option)

5.7 PWM Generator and Capture Timer (PWM)

5.7.1 Overview

NuMicro™ NUC100 Medium Density has 2 sets of PWM group supports total 4 sets of PWM Generators which can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable dead-zone generators. NuMicro™ NUC100 Low Density only support 1 set of PWM group supports total 2 sets of PWM Generators which can be configured as 4 independent PWM outputs, PWM0~PWM3, or as 2 complementary PWM pairs, (PWM0, PWM1) and (PWM2, PWM3) with 2 programmable dead-zone generators.

Each PWM Generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as auto-reload mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse high width modulation. The counter control logic changes the output to high level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM 0; and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 3 on each group have the same feature by setting the corresponding control bits in CCR0 and CCR2. For each group, whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

The maximum captured frequency that PWM can capture is confined by the capture interrupt latency. When capture interrupt occurred, software will do at least three steps, they are: Read PIIRx to get interrupt source and Read PWM_CRLx/PWM_CFLx(x=0~3) to get capture value and finally write 1 to clear PIIRx to zero. If interrupt latency will take time T0 to finish, the capture signal mustn't transition during this interval (T0). In this case, the maximum capture frequency will be 1/T0. For example:

HCLK = 50MHz, PWM_CLK = 25MHz, Interrupt latency is 900 ns

So the maximum capture frequency will is 1/900ns ≈ 1000 kHz

5.7.2 Features

5.7.2.1 PWM function features:

- PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16 bits resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- Up to 2 PWM group (PWMA/PWMB) to support 8 PWM channels or 4 PWM paired channels (only 1 PWM group support for Low Density)

5.7.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators
- Support 8 Capture input channels shared with 8 PWM output channels (Low Density only support 4 Capture input channels shared with 4 PWM output channels)
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

5.8 Real Time Clock (RTC)

5.8.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 kHz crystal connected at pins X32I and X32O (reference to pin descriptions) or from an external 32.768 kHz oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). The RTC Time Tick if Wakeup CPU function is enabled (TWKE (TTR[3])=1) and Alarm Match can cause CPU wakeup from sleep or power-down mode.

5.8.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time
- Alarm register (second, minute, hour, day, month, year)
- 12-hour or 24-hour mode is selectable
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message is expressed in BCD code
- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Support RTC Time Tick and Alarm Match interrupt
- Support wake up CPU from sleep or power-down mode

5.9 Serial Peripheral Interface (SPI)

5.9.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. The NuMicro™ NUC100 Medium Density contains up to four sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be configured as a slave device controlled by an off-chip master device. NuMicro™ NUC100 Low Density contains two sets of SPI controller only.

This controller supports a variable serial clock for special application and it also supports 2 bit transfer mode to connect 2 off-chip slave devices at the same time. The SPI controller also supports PDMA function to access the data buffer.

5.9.2 Features

- Up to four sets of SPI controller for NuMicro™ NUC100 Medium Density
- Up to two sets of SPI controller for NuMicro™ NUC100 Low Density
- Support master or slave mode operation
- Support 1-bit or 2-bit transfer mode
- Configurable bit length up to 32 bits of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64 bits for each data transfer
- Provide burst mode operation, transmit/receive can be transferred up to two times word transaction in one transfer
- Support MSB or LSB first transfer
- 2 device/slave select lines in master mode, but 1 device/slave select line in slave mode
- Support byte reorder in data register
- Support byte or word suspend mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode
- Support two channel PDMA request, one for transmitter and another for receiver

5.10 Timer Controller (TMR)

5.10.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current value during operation. Note: event counting function only support in NuMicro™ NUC100 Low Density.

5.10.2 Features

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and auto-reload counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / 25 MHz) * (2^8) * (2^24), if timer clock is 25 MHz
- 24-bit timer value is readable through TDR (Timer Data Register)

5.11 Watchdog Timer (WDT)

5.11.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wakeup CPU from power-down mode. The watchdog timer includes a 18-bit free running counter with programmable time-out intervals. Table 5-2 show the watchdog timeout interval selection and Figure 5-64 shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WDTCR [7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * T_{WDT}) follows the time-out event. User must set WTR (WDTCR [0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid CPU from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR [10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset CPU. This reset will last 63 WDT clocks (T_{RST}) then CPU restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTFR by software to recognize the reset source. WDT also provides wakeup function. When chip is powered down and the Watchdog Timer Wakeup Function Enable bit (WDTR[4]) is set, if the WDT counter has not been cleared after the specific delay time expires, the chip will be waken up from power down state.

WTIS	Timeout Interval Selection T_{TIS}	Interrupt Period T_{INT}	WTR Timeout Interval (WDT_CLK=12 MHz) Min. T_{WTR} ~ Max. T_{WTR}
000	$2^4 * T_{WDT}$	1024 * T_{WDT}	1.33 us ~ 86.67 us
001	$2^6 * T_{WDT}$	1024 * T_{WDT}	5.33 us ~ 90.67 us
010	$2^8 * T_{WDT}$	1024 * T_{WDT}	21.33 us ~ 106.67 us
011	$2^{10} * T_{WDT}$	1024 * T_{WDT}	85.33 us ~ 170.67 us
100	$2^{12} * T_{WDT}$	1024 * T_{WDT}	341.33 us ~ 426.67 us
101	$2^{14} * T_{WDT}$	1024 * T_{WDT}	1.36 ms ~ 1.45 ms
110	$2^{16} * T_{WDT}$	1024 * T_{WDT}	5.46 ms ~ 5.55 ms
111	$2^{18} * T_{WDT}$	1024 * T_{WDT}	21.84 ms ~ 21.93 ms

Table 5-2 Watchdog Timeout Interval Selection

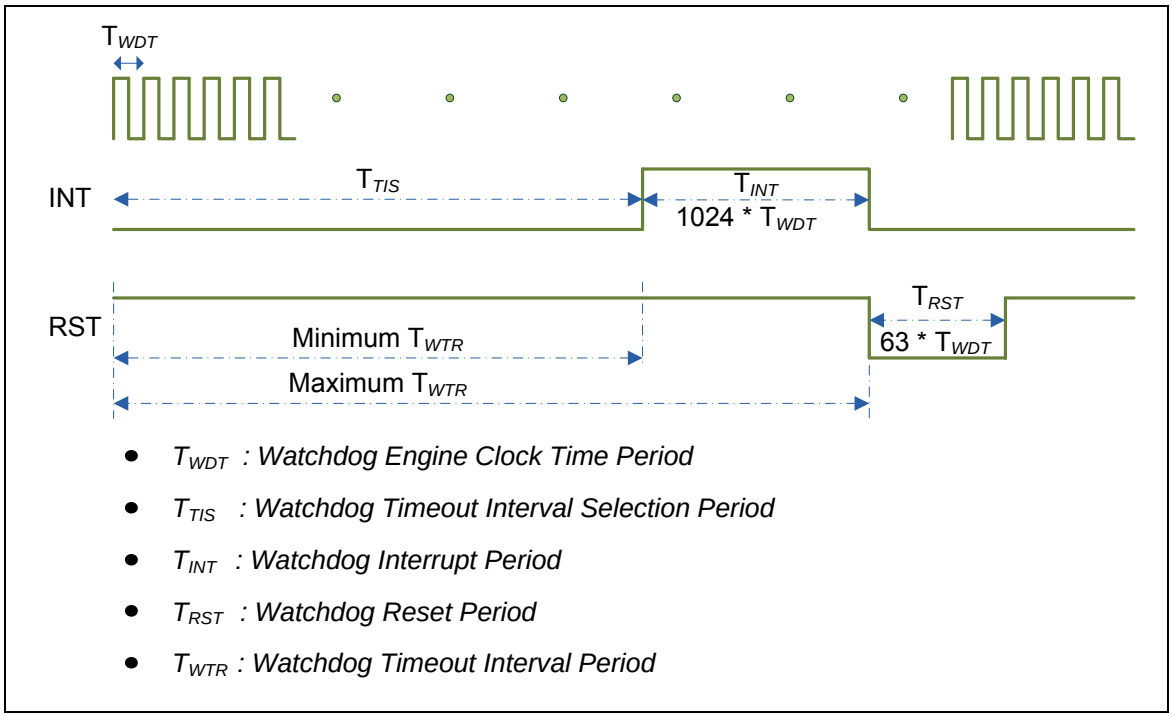


Figure 5-10 Timing of Interrupt and Reset Signal

5.11.2 Features

- 18-bit free running counter to avoid CPU from Watchdog timer reset before the delay time expires.
- Selectable time-out interval (2^4 ~ 2^18) and the time out interval is 86.67 us ~ 21.93 ms (if WDT_CLK = 12 MHz).
- Reset period = (1 / 12 MHz) * 63, if WDT_CLK = 12 MHz.

5.12 UART Interface Controller (UART)

NuMicro™ NUC100 Medium Density provides up to three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UART, besides, only UART0 and UART1 support flow control function. NuMicro™ NUC100 Low Density only supports UART0 and UART1.

5.12.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, LIN master/slave mode function and RS-485 mode functions. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wakeup status interrupt (INT_MODEM), Buffer error interrupt (INT_BUF_ERR) and LIN receiver break field detected interrupt (INT_LIN_RX_BREAK). Interrupts of UART0 and UART2 share the interrupt number 12 (vector number is 28); Interrupt number 13 (vector number is 29) only supports UART1 interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART0 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART1~2 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Table 5-3 lists the equations in the various conditions and Table 5-4 list the UART baud rate setting table.

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5-3 UART Baud Rate Equation

System clock = 22.1184MHz			
Baud rate	Mode0	Mode1	Mode2
921600	x	A=0,B=11	A=22
460800	A=1	A=1,B=15 A=2,B=11	A=46
230400	A=4	A=4,B=15 A=6,B=11	A=94
115200	A=10	A=10,B=15 A=14,B=11	A=190

57600	A=22	A=22,B=15 A=30,B=11	A=382
38400	A=34	A=62,B=8 A=46,B=11 A=34,B=15	A=574
19200	A=70	A=126,B=8 A=94,B=11 A=70,B=15	A=1150
9600	A=142	A=254,B=8 A=190,B=11 A=142,B=15	A=2302
4800	A=286	A=510,B=8 A=382,B=11 A=286,B=15	A=4606

Table 5-4 UART Baud Rate Setting Table

The UART0 and UART1 controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL [1]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the LIN_EN bit in UA_FUN_SEL register. In LIN mode, one start bit and 8-bit data format with 1-bit stop bit are required in accordance with the LIN standard.

For NuMicro™ NUC100 Low Density, another alternate function of UART controllers is RS-485 9 bit mode function, and direction control provided by RTS pin or can program GPIO (PB.2 for RTS0 and PB.6 for RTS1) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

5.12.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 64/16/16 bytes (UART0/UART1/UART2) entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0 and UART1 support)
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTS wake up function (UART0 and UART1 support)
- Support 7 bit receiver buffer time out detection function
- UART0/UART1 can be served by the DMA controller
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Support IrDA SIR function mode
  - Support for 3/16 bit duration for normal mode
- Support LIN function mode
  - Support LIN master/slave mode
  - Support programmable break generation function for transmitter
  - Support break detect function for receiver
- Support RS-485 function mode. (Low Density only)
  - Support RS-485 9bit mode
  - Support hardware or software direct enable control provided by RTS pin

5.13 Controller Area Network (CAN)

5.13.1 Overview

The Controller Area Network (CAN) is a serial communications protocol which is multi-master and it efficiently supports distributed real-time control with very high level of security. Its domain of application range from high speed networks to low cost multiplex wiring. In automotive electronics, engine control units, sensors, anti-skid-systems, etc. are connected using CAN with bit-rates up to 1Mbit/s.

In CAN systems, a node does not make use of any information about the system configuration (station addresses). Any Nodes can be added to the CAN network without requiring any change in the software or hardware of any node. The information on the bus is sent in fixed format message of different but limited length. When the bus is free, any connected unit may start to transmit a new message. The content of message is named by IDENTIFIER. The IDENTIFIER does not indicate the destination of the message, but describes the meaning of the data, so that all nodes in the network are able to decide by Message Filtering whether the data is to be acted upon by them or not. Within a CAN network it is guaranteed that a message is simultaneously accepted either by all nodes or by no node.

5.13.2 Features

- CAN 2.0B protocol compatibility
- Multi-master node
- Support 11-bit identifier as well as 29-bit identifier
- Bit rates up to 1Mbits/s
- NRZ bit coding
- Error detection: bit error, stuff error, form error, 15-bit CRC detection, and acknowledge error
- Listen only mode (no acknowledge, no active error flags)
- Acceptance filter extension (4-byte code, 4-byte mask)
- Error interrupt for each CAN-bus error
- Extended receive buffer (8-byte FIFO)
- Wakeup function

5.14 PS2 Device Controller (PS2D)

5.14.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/W can select 1 to 16 bytes for a continuous transmission.

5.14.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

5.15 I²S Controller (I²S)

5.15.1 Overview

The I²S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word deep FIFO for read path and write path respectively and is capable of handling 8 ~ 32 bit word sizes. DMA controller handles the data movement between FIFO and memory.

5.15.2 Features

- I²S can operate as either master or slave
- Capable of handling 8, 16, 24 and 32 bit word sizes
- Mono and stereo audio data supported
- I²S and MSB justified data format supported
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive
- Generates interrupt requests when buffer levels cross a programmable boundary
- Two DMA requests, one for transmit and one for receive

5.16 Analog-to-Digital Converter (ADC)

5.16.1 Overview

NuMicro™ NUC100 Series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. There are two kinds of scan mode: continuous mode and single cycle mode. The A/D converters can be started by software and external STADC pin.

5.16.2 Features

- Analog input voltage range: 0~Vref (Max to 5.0V)
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or 4 differential analog input channels
- Maximum ADC clock frequency is 16MHz
- Up to 600K SPS conversion rate
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion
- An A/D conversion can be started by
  - Software write 1 to ADST bit
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting
- Channel 7 supports 3 input sources: external analog voltage, internal fixed bandgap voltage, and internal temperature sensor output
- Support Self-calibration to minimize conversion error

5.17 Analog Comparator (CMP)

5.17.1 Overview

NuMicro™ NUC100 Series contains two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause an interrupt when the comparator output value changes.

Note that the analog input port pins must be configured as input type before Analog Comparator function is enabled.

5.17.2 Features

- Analog input voltage range: 0~5.0V
- Hysteresis function supported
- Two analog comparators with optional internal reference voltage input at negative end
- One comparator interrupt requested by either comparator

5.18 PDMA Controller (PDMA)

5.18.1 Overview

NuMicro™ NUC100 Medium Density contains a peripheral direct memory access (PDMA) controller that transfers data to and from memory or transfer data to and from APB devices. The PDMA has nine channels of DMA (Peripheral-to-Memory or Memory-to-Peripheral or Memory-to-Memory). For each PDMA channel (PDMA CH0~CH8), there is one word buffer as transfer buffer between the Peripherals APB devices and Memory.

Software can stop the PDMA operation by disable PDMA [PDMACEN]. The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The PDMA controller can increase source or destination address or fixed them as well.

Notice: NuMicro™ NUC100 Low Density only has 1 PDMA channel (channel 0).

5.18.2 Features

- Up to nine DMA channels. Each channel can support a unidirectional transfer (Low Density only has 1 PDMA channel)
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Support source and destination address increased mode or fixed mode
- Hardware channel priority. DMA channel has the highest priority and channel has the lowest priority

5.19 External Bus Interface (EBI)

5.19.1 Overview

The NuMicro™ NUC100 Low Density LQFP-64 package equips an external bus interface (EBI) for external device used.

To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. And, address latch enable (ALE) signal supported differentiate the address and data cycle.

5.19.2 Features

External Bus Interface has the following functions:

- External devices with max. 64K-byte size (8 bit data width)/128K-byte (16 bit data width) supported
- Variable external bus base clock (MCLK) supported
- 8 bit or 16 bit data width supported
- Variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD) supported
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R)

6 FLASH MEMORY CONTROLLER (FMC)

6.1 Overview

NuMicro™ NUC100 Series equips with 128/64/32K bytes on chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on, Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro™ NUC100 Series also provides additional DATA Flash for user, to store some application dependent data before chip power off. For 128K bytes APROM device, the data flash is shared with original 128K program memory and its start address is configurable and defined by user application request in Config1. For 64K/32K bytes APROM device, the data flash is fixed at 4K.

6.2 Features

- Run up to 50 MHz with zero wait state for continuous address read access
- 128/64/32KB application program memory (APROM) (Low Density only support up to 64KB size)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Configurable or fixed 4KB data flash with 512 bytes page erase unit
- Programmable data flash start address for 128K APROM device
- In System Program (ISP) to update on chip Flash EPROM

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

7.2.1 NuMicro™ NUC100/NUC120/NUC130/NUC140 Medium Density DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50MHz	I_{DD1}		54		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD2}		31		mA	V_{DD} = 5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{DD3}		51		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD4}		28		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 12MHz	I_{DD5}		22		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD6}		14		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{DD7}		20		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD8}		12		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 4MHz	I_{DD9}		15		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD10}		11		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{DD11}		13		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD12}		9		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 50MHz	I_{IDLE1}		38		mA	V_{DD}= 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE2}		15		mA	V_{DD}=5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{IDLE3}		35		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Idle Mode @ 12MHz	I_{IDLE5}		13		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE6}		5.5		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{IDLE7}		12		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{IDLE8}		4		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Idle Mode @ 4MHz	I_{IDLE9}		8.5		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE10}		3.5		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{IDLE11}		7		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE12}		2.5		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		23		μA	V_{DD} = 5.5V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		18		μA	V_{DD} = 3.3V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		28		μA	V_{DD} = 5.5V, RTC run , No load @ Disable BOV function
	I_{PWD4}		22		μA	V_{DD} = 3.3V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IL2}				V	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IH2}		$0.2V_{DD}$		V	
Hysteresis voltage of PA~PE (Schmitt input)	V_{HY}		$0.2V_{DD}$		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V

Note:

1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

7.2.2 NuMicro™ NUC100/NUC120/NUC130/NUC140 Low Density DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	2.5	+10%	V	V_{DD} > 2.7V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50MHz	I_{DD1}		46		mA	V_{DD} = 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD2}		30		mA	V_{DD} = 5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{DD3}		44		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{DD4}		28		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 12MHz	I_{DD5}		19		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD6}		13		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{DD7}		17		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD8}		11.5		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Normal Run Mode @ 4MHz	I_{DD9}		13.5		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD10}		10		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{DD11}		12		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD12}		8		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 50MHz	I_{IDLE1}		30		mA	V_{DD}= 5.5V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE2}		13		mA	V_{DD}=5.5V@50MHz, disable all IP and enable PLL, XTAL=12MHz
	I_{IDLE3}		28		mA	V_{DD} = 3V@50MHz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE4}		12		mA	V_{DD} = 3V@50MHz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Idle Mode @ 12MHz	I_{IDLE5}		11		mA	V_{DD} = 5.5V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE6}		5		mA	V_{DD} = 5.5V@12MHz, disable all IP and disable PLL, XTAL=12MHz
	I_{IDLE7}		10		mA	V_{DD} = 3V@12MHz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE8}		4		mA	V_{DD} = 3V@12MHz, disable all IP and disable PLL, XTAL=12MHz

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Idle Mode @ 4MHz	I_{IDLE9}		7		mA	V_{DD} = 5V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE10}		3.5		mA	V_{DD} = 5V@4MHz, disable all IP and disable PLL, XTAL=4MHz
	I_{IDLE11}		6		mA	V_{DD} = 3V@4MHz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE12}		2.5		mA	V_{DD} = 3V@4MHz, disable all IP and disable PLL, XTAL=4MHz
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		17		μA	V_{DD} = 5.5V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		14.5		μA	V_{DD} = 3.3V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		20		μA	V_{DD} = 5.5V, RTC run , No load @ Disable BOV function
	I_{PWD4}		17		μA	V_{DD} = 3.3V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IL2}	-0.5	-	0.2V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE (Schmitt input)	V_{IH2}	0.4V_{DD}	-	V_{DD} +0.5	V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	v	
Input High Voltage X32I[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V

Note:

1. /RESET pin is a Schmitt trigger input.

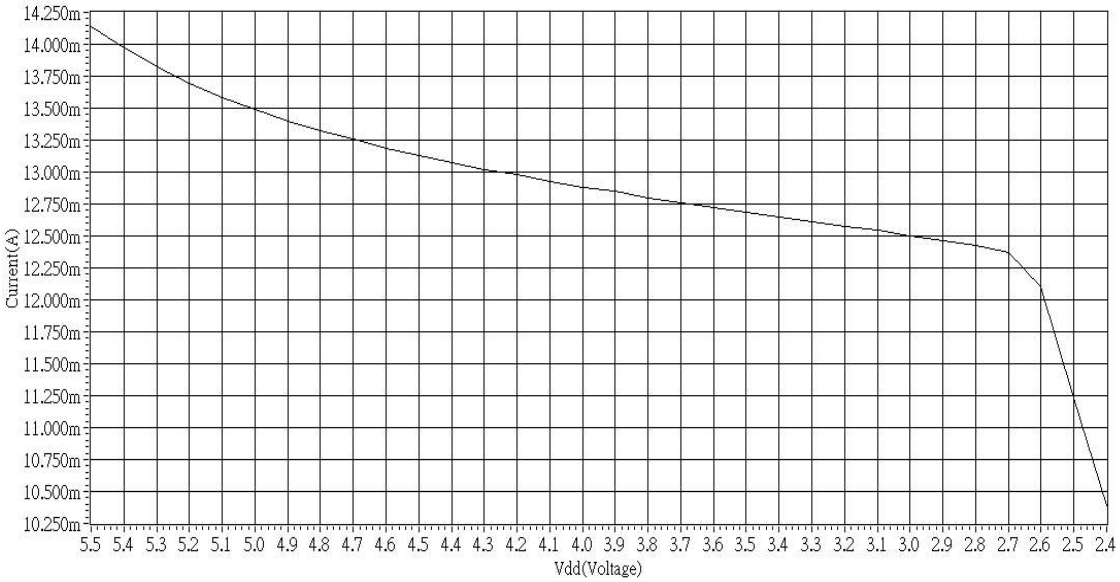
2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

7.2.3 Operating Current Curve (Test condition: run NOP)

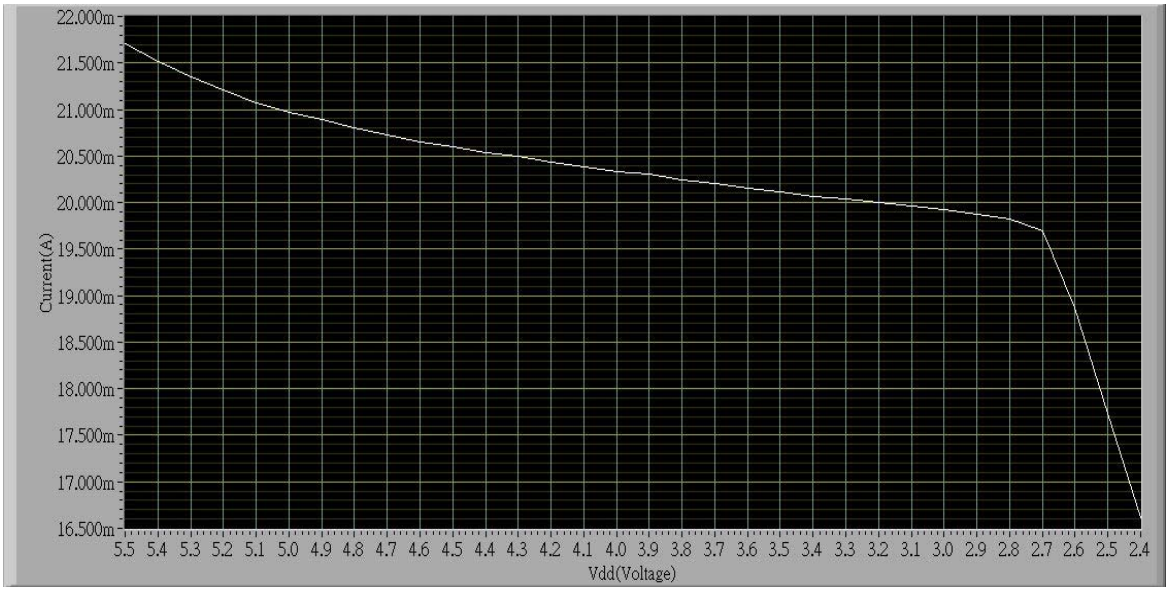
1. XTAL clock = 12 MHz, PLL disable, all-IP disable:

Unit: mA



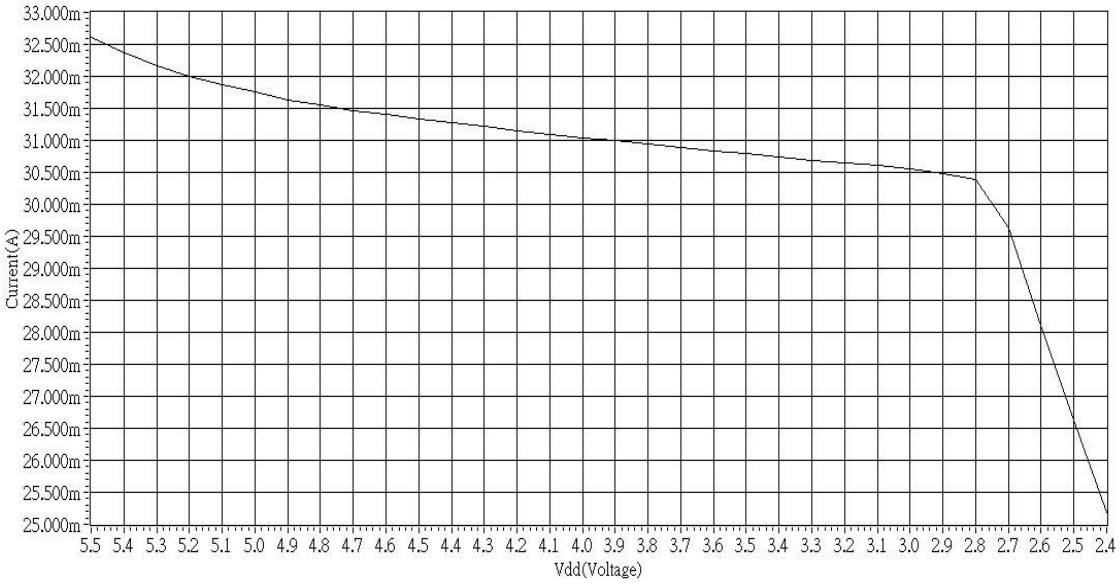
2. XTAL clock = 12 MHz, PLL disable, all-IP enable

Unit: mA



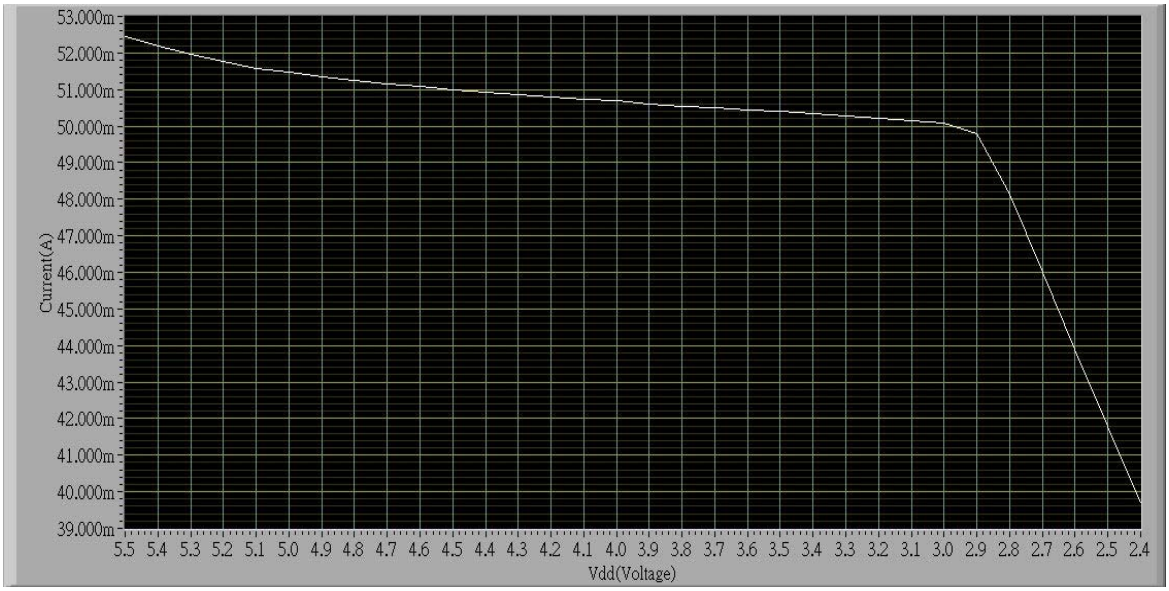
3. XTAL clock = 12 MHz, PLL enable, all-IP disable

Unit: mA



4. XTAL clock = 12 MHz, PLL enable, all-IP enable

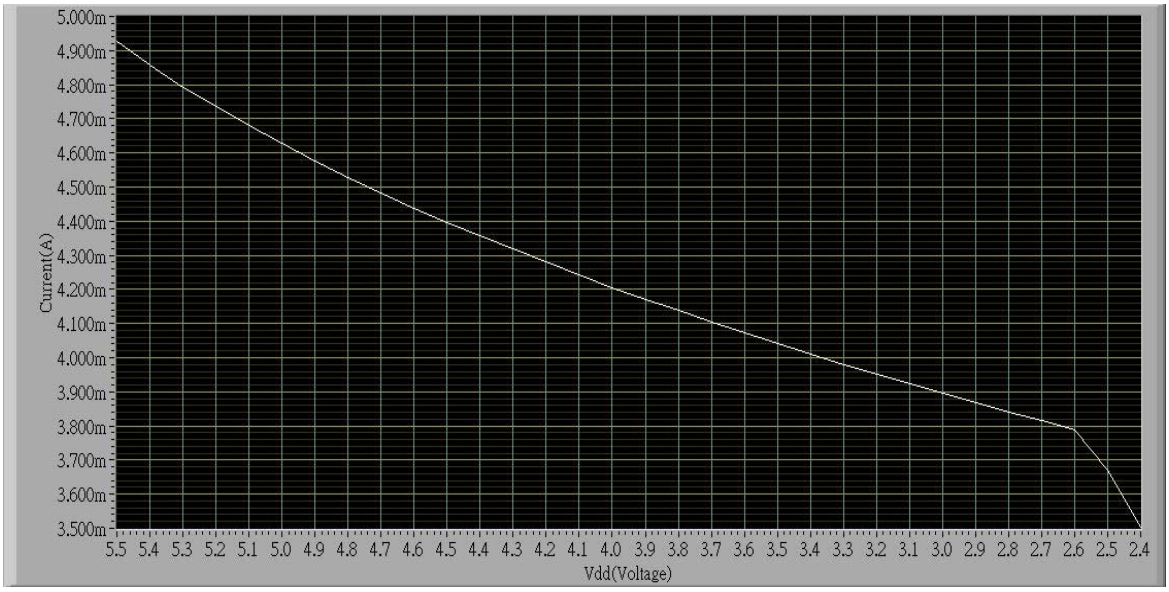
Unit: mA



7.2.4 Idle Current Curve

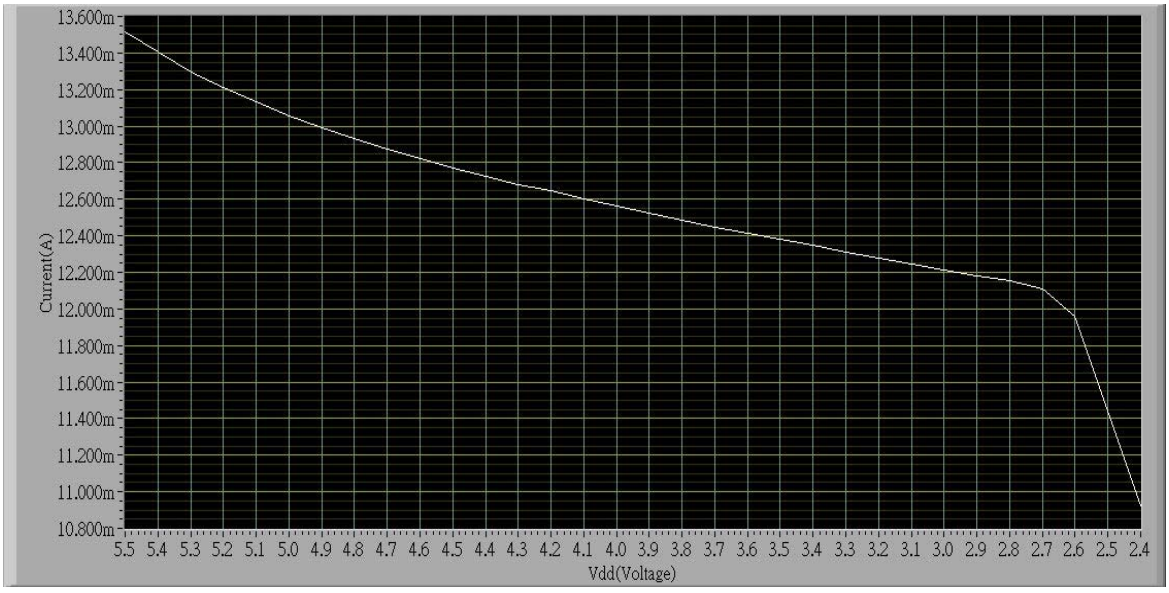
1. XTAL clock = 12 MHz, PLL disable, all-IP disable

Unit: mA



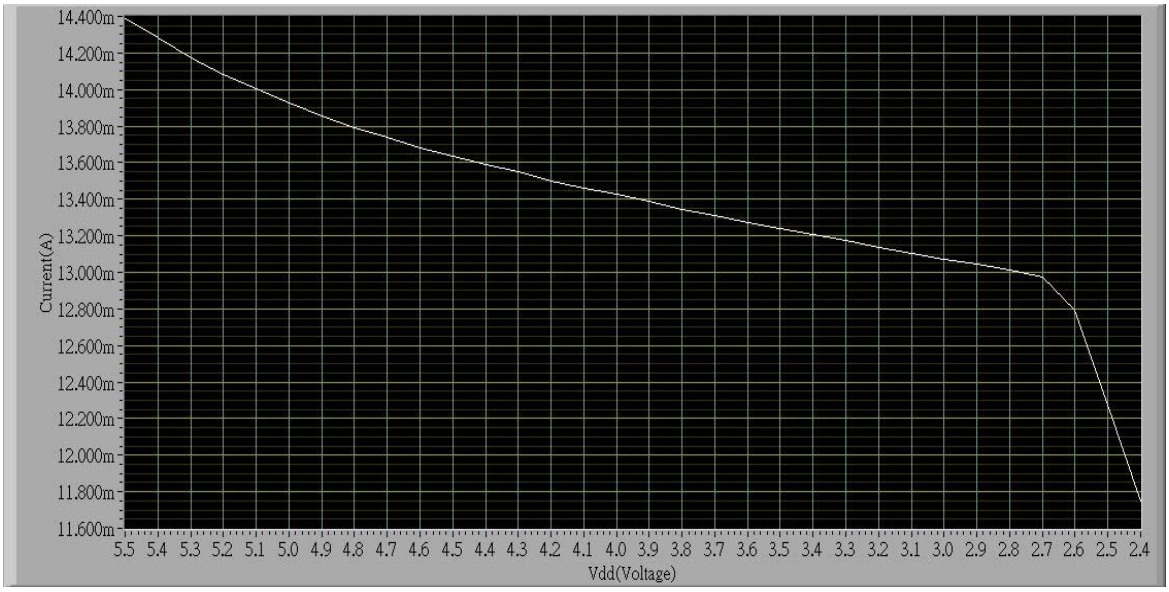
2. XTAL clock = 12 MHz, PLL disable, all-IP enable

Unit: mA



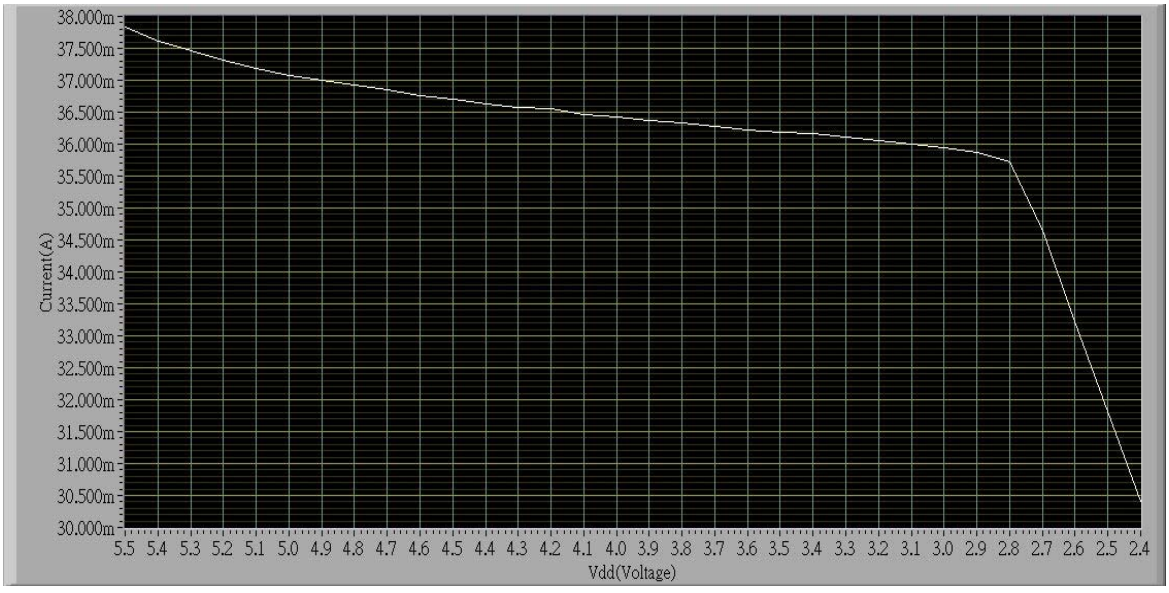
3. XTAL clock = 12 MHz, PLL enable, all-IP disable

Unit: mA



4. XTAL clock = 12 MHz, PLL enable, all-IP enable

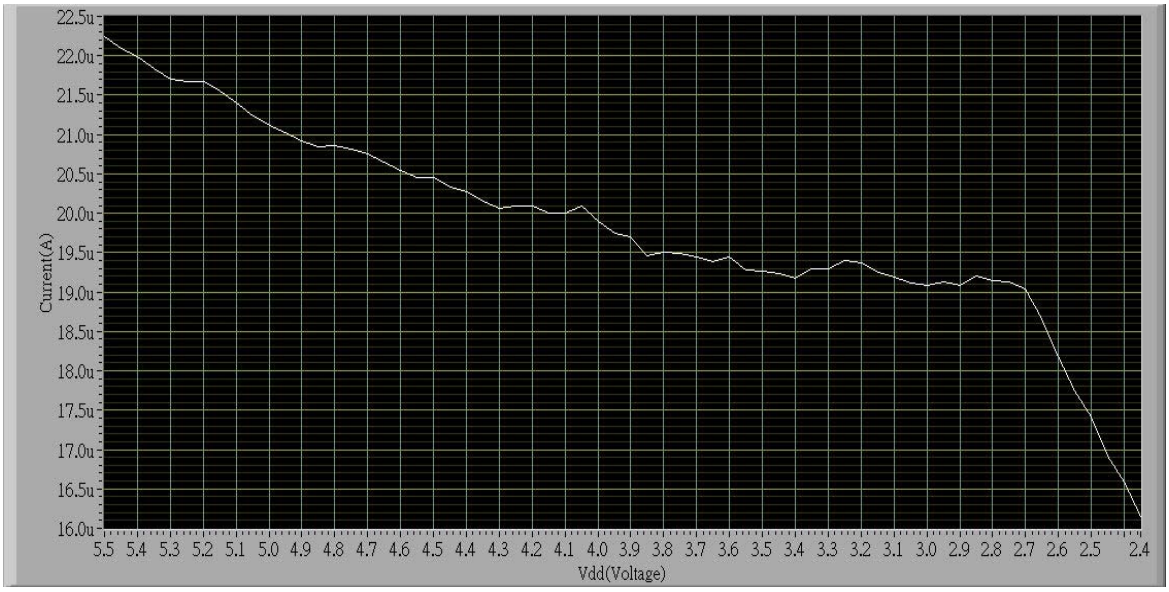
Unit: mA



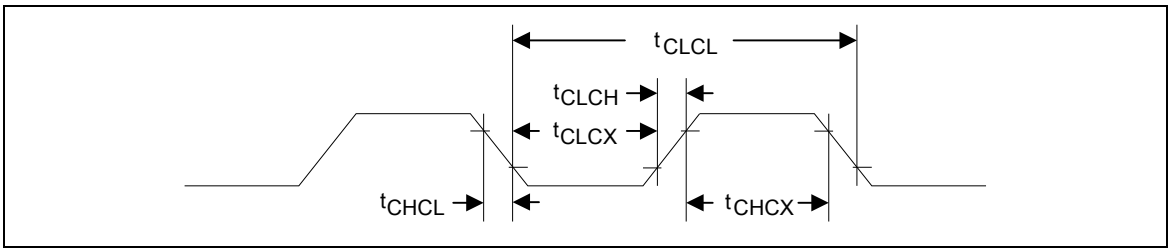
7.2.5 Power Down Current Curve

XTAL clock = 12 MHz, PLL Disable

Unit: mA



7.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

7.3.1 External 4~24MHz Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	5	5.5	V

7.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

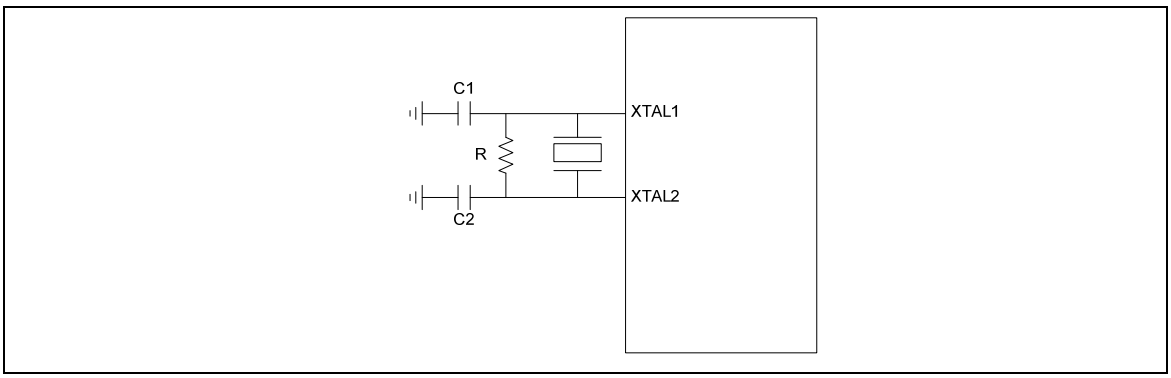


Figure 7-1 Typical Crystal Application Circuit

7.3.2 External 32.768 kHz Crystal

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	-	5.5	V

7.3.3 Internal 22.1184 MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5V	-1	-	+1	%
	-40 C~+85 C; VDD=2.5V~5.5V	-3	-	+3	%
Operation Current	V_{DD} =5V	-	500	-	uA

7.3.4 Internal 10 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 C; V_{DD} =5V	-30	-	+30	%
	-40 C~+85 C; V_{DD}=2.5V~5.5V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 Specification of 12-bit SARADC

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	±3	-	LSB
INL	Integral nonlinearity error	-	±4	-	LSB
EO	Offset error	-	±1	10	LSB
EG	Gain error (Transfer gain)	-	1	1.005	-
-	Monotonic	Guaranteed			
FADC	ADC clock frequency	-	-	20	MHz
TCAL	Calibration time	-	127	-	Clock
TS	Sample time	-	7	-	Clock
TADC	Conversion time	-	13	-	Clock
FS	Sample rate	-	-	600	K SPS
VLDO	Supply voltage	-	2.5	-	V
VADD		3	-	5.5	V
IDD	Supply current (Avg.)	-	0.5	-	mA
IDDA		-	1.5	-	mA
VREF	Reference voltage	-	VDDA	-	V
IREFP	Reference current (Avg.)	-	1	-	mA
VIN	Reference voltage	0	-	VREF	V
CIN	Capacitance	-	5	-	pF

7.4.2 Specification of LDO & Power management

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V_{DD} input voltage
Output Voltage	-10%	2.5	+10%	V	V_{DD} > 2.7V
Temperature	-40	25	85	℃	
Quiescent Current (PD=0)	-	100	-	uA	
Quiescent Current (PD=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1	-	uF	Resr=1ohm
Cload	-	250	-	pF	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V
	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Specification of Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.4.6 Specification of Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]		2.5	-	5.5	V
Temperature		-40	-	125	℃
Current consumption		6.4	-	10.5	uA
Gain		-1.95	-2	-2.05	mV/℃
Offset	Temp=0 ℃	688	708	730	mV

Note: Internal operation voltage comes form LDO.

7.4.7 Specification of Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
VDD	-	2.4	3	5.5	V
VDD current	20uA@VDD=3V	-	20	40	uA
Input offset voltage	-	-	5	15	mV
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2V & VDIFF=0.1V	-	200	-	ns
Comparison voltage	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis	10	20	-	mV
Hysteresis	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V	-	±10	-	mV
Wake up time	@CINP=1.3V CINN=1.2V	-	-	2	us

7.4.8 Specification of USB PHY

7.4.8.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.8.2 USB Full-Speed Driver Electrical Characteristics

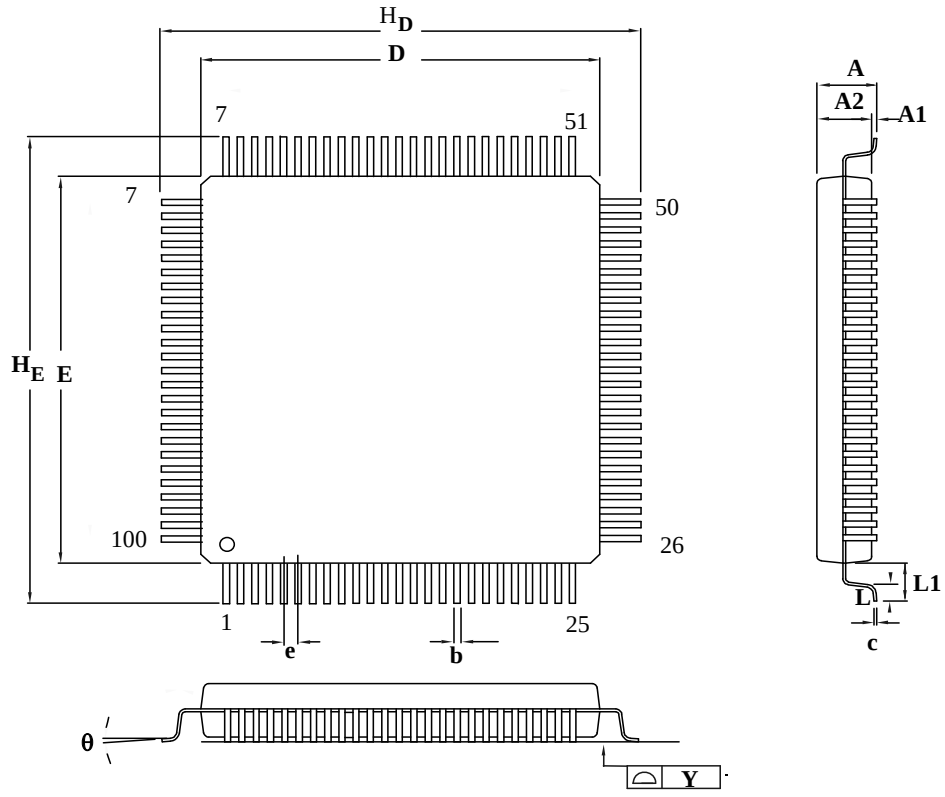
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4		20	ns
T_{FF}	Fall Time	C_L=50p	4		20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90		111.11	%

7.4.8.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

8 PACKAGE DIMENSIONS

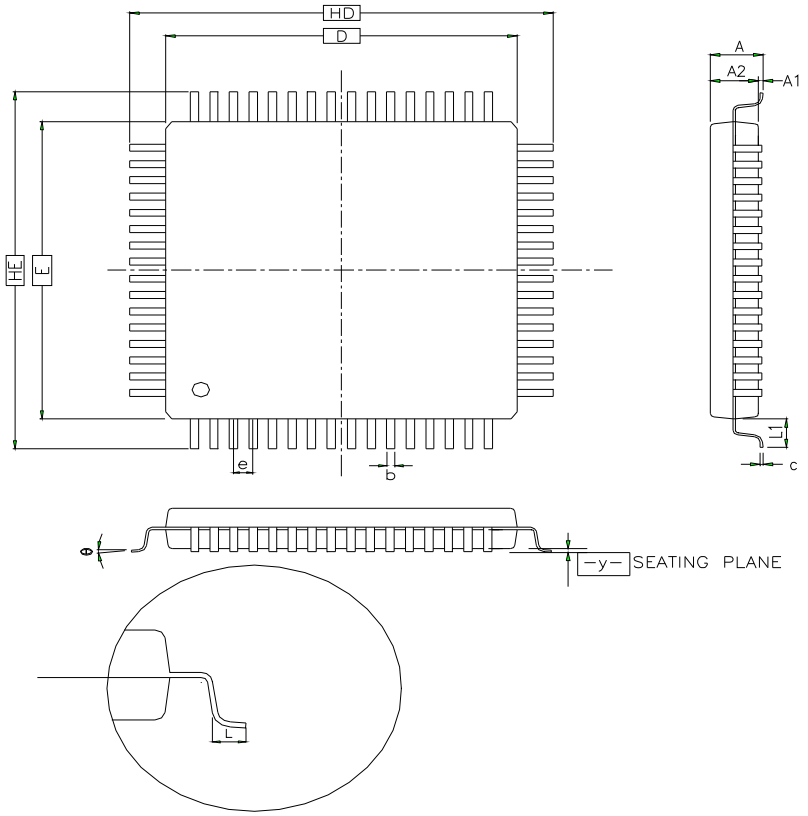
8.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



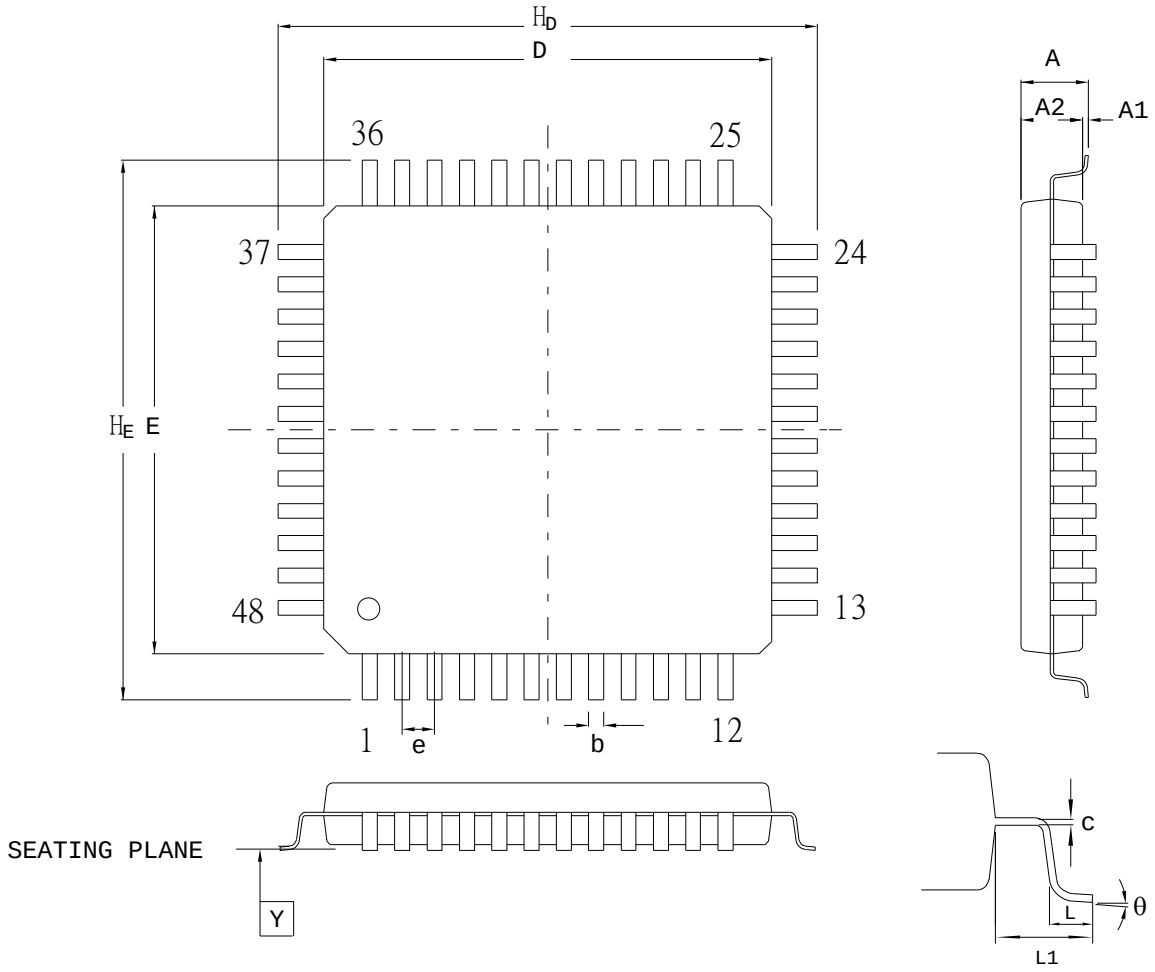
Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

8.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

8.3 48L LQFP (7x7x1.4mm footprint 2.0mm)

9 VISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	March 1, 2010	-	Preliminary version initial issued
V1.01	April 9, 2010	Ch4	Modify the block diagram
V1.02	May 31, 2010	7.2	Add operation current of DC characteristics
V1.03	Aug. 23, 2010	7.2	Modify operation current of DC characteristics
V2.00	Nov. 11, 2010	-	Update low density and selection table

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