

ISL6721EVAL3Z: Resonant Reset Forward Converters for Low Power Applications

Abstract

Low cost, isolated power supplies with multiple outputs are common in many applications such as automotive, security monitoring, telecom, medical instruments, etc. For these applications, multiple output rails are needed for integrated circuits (IC) with different operation voltages on the same printed circuit board (PCB). Usually the voltage regulation of these outputs are not tight, and the current level not high. Isolation between the converter's input and output is necessary for safety considerations and ground separation. Isolated power converters with multiple secondary side windings provide low cost solutions for these applications. Intersil's isolated power family products support these applications with both double-ended PWM controllers (ISL6740, ISL67401, ISL6742, ISL6743, ISL6745), and single-ended PWM controllers (ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845, ISL6721, ISL6722, and ISL6723). Single-ended flyback and forward converters based on ISL6721 are the most frequently used because of its high performance and low cost.

The ISL6721EVAL3Z board serves as a reference design for single switch resonant reset forward converter with multiple outputs for typical industry applications that need isolation. It can be used for security monitoring systems where an input voltage range of 21.6V to 52.8V is typical for operation from a battery source of 24V or 48V with 10% tolerance.

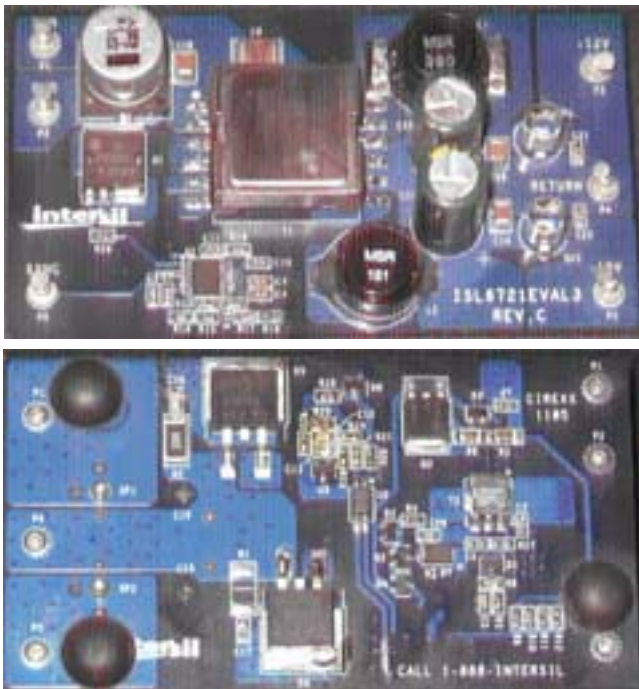


FIGURE 1. TOP AND BOTTOM VIEW OF THE PCB BOARD

Design Specifications

The evaluation board ISL6721EVAL3Z aims at the following design specifications.

- Switching Frequency, Fsw: 300kHz
- Input Voltage Range, V_{IN} : 21.6V DC to 52.8V DC
- Output Voltage 1, V_{OUT1} : 12V with 5% Absolute Regulation
- Output Current 1, I_{OUT1} : 2.5A
- Output Voltage 2, V_{OUT2} : 18V with 5% Absolute Regulation
- Output Current 2, I_{OUT2} : 1A
- Overall Output Power, P_{OUT} : 48W
- Full Load Efficiency: 80% under all Line and Load Conditions
- Output Voltage Ripple: 50mV_{p-p} on each Rail
- Minimum Load: 25% on 12V Rail, 20% on 18V Output.

Description of Circuit Operation

The ISL6721 is a high performance single-ended PWM controller intended for various isolated and non-isolated applications for telecom power supply, server power and industrial power supply. It can be used in various single transistor topologies including forward and flyback regulators, boost converters, buck-boost converters, and SEPIC converters. With the rich protection and control features, it provides optimal solutions for single ended current mode PWM controlled isolated power converters with minimum external components and high performance.

A single switch forward topology has higher efficiency over the cheap flyback converters, and is widely accepted for less than 100W applications. However, the forward transformer needs to be reset within each switching cycle. There are mainly three reset methods, that is, reset winding plus diode, active clamp switch, and resonant reset with capacitor. In a resonant reset converter (RRF), a reset capacitor is connected to the drain source of the transistor. As the main switch is turned off, a resonance is developed between the magnetizing/leakage inductance and the equivalent resonant capacitor. The high voltage across the drain of the switch resets the core of the transformer. Only one switch is used, and it does not need a reset winding or diode.

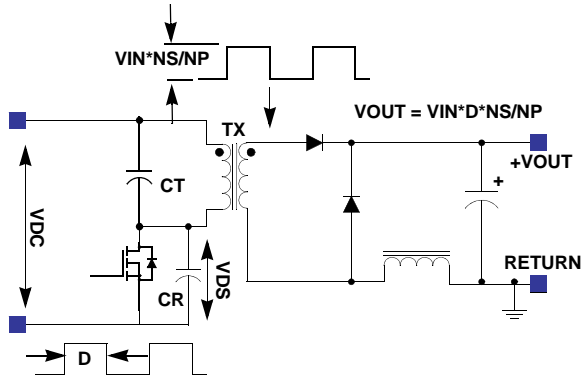


FIGURE 2. EQUIVALENT CIRCUIT SCHEMATIC OF A RESONANT RESET CONVERTER WITH TRANSFORMER

Figure 2 shows the simplified schematic of the resonant reset forward converter. The reset capacitance is formed by the drain source of the transistor C_{OSS} , the winding capacitance of the transformer C_t , and the external capacitor C_r . The circuit operation of the converter in steady state includes three intervals in each switching period.

At the very beginning, $t = t_1$, the interval 1 begins as the switch turns on. The voltage across the transistor and the resonant capacitor drops to zero. The transformer is magnetized with the input voltage V_{IN} . The magnetizing current linearly increases with the slope given by V_{IN}/L_m . The primary switch current is the sum of the magnetizing current and the reflected secondary side load current. The typical current and voltage waveforms are shown in Figure 3.

$$\Delta I_{mag} = ((V_{in})/(L_m))t_{on} \quad (EQ. 1)$$

At the end of this interval, $t = t_2$, the switch is turned off, and interval 2 begins. First, the resonant capacitor is quickly charged to V_{IN} by magnetizing current plus the reflected load current. Then the magnetizing current keeps flowing and charges up the resonant capacitor in a resonant way with the resonant frequency mainly determined by the magnetizing inductance. The equivalent resonant capacitance as given in Equation 2, and then discharges through the magnetizing inductance, thus reset the transformer core. The peak of the voltage across the resonant capacitor is given in Equation 3. The peak voltage across the resonant capacitor is the resonant voltage plus input voltage at one fourth of the resonant period, where I_{LM} is $0.5\Delta I_{mag}$ given in Equation 1.

$$f_R = \frac{1}{2\pi\sqrt{L_m(C_{oss} + C_r + C_t)}} \quad (EQ. 2)$$

$$V_{CR} = V_{in} + I_{LM}\sqrt{(L_m)/(C_r + C_t + C_{oss})} \quad (EQ. 3)$$

As the voltage across the resonant reset capacitor resets to V_{IN} , $t = t_3$, the interval 3 begins. In the secondary side, both of the two diodes in each output channel of the secondary side are on. The primary transistor remains

turned off, and the voltage across the drain of the transistor is clamped to V_{IN} .

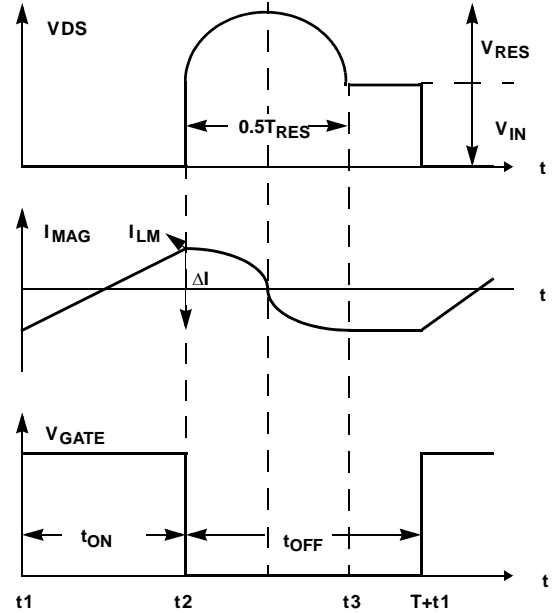


FIGURE 3. OPERATION WAVEFORMS DURING STEADY STATE

Circuit Design Description

The design of the power circuit and control circuit include the transformer design, main switch selection, rectifier diode selection, snubber selection, ISL6721 configuration, and will be detailed below.

Primary Side Circuit Design

The transformer design involves the following steps and may need several iterations for considerations of power loss, geometry and electric parameters.

- Calculate the primary and secondary winding currents.
- Select core geometry and material.
- Calculate the maximum flux density of operation.
- Select core size.
- Calculate the turns ratio.
- Calculate the wire gauge, number of strands, winding order and insulation requirements.
- Estimate the losses.
- Verify the design.

For this design example, a commonly used low profile EFD20 core, 3F3 material (or equivalent), was selected with effective core cross-sectional area, $A_e = 31\text{mm}^2$.

From the datasheet of the core material the maximum operation flux density can be set at 1750 gauss with 50% margin. Based on the core losses, the operational maximum flux density will be tweaked during the course of the design. Given the maximum flux density, the number of primary turns can be calculated using Faraday's Law, $V = N \text{ d}\Phi/\text{d}t$. Starting with a maximum

Application Note 1491

duty cycle assumption of 40% corresponding to low line, the minimum number of primary turns can be obtained from Equation 4.

$$N_{Pmin} = \frac{V_{in_{min}} \cdot D_{max} \cdot T_{sw}}{dB_{max} \cdot A_e} = \frac{21.6 \cdot 0.4 \cdot 3.3e-6}{0.175 \cdot 31e-6} = 5.3 \text{ Turns} \quad (\text{EQ. 4})$$

The number of turns on each secondary winding is derived by the voltage seen across the respective windings, which would be a diode drop (assumed to be 0.5V) greater than the nominal output voltage. In order to generate output voltages that are close to the specified values, the number of turns were rounded to the following numbers:

- $N_p = 8 \text{ T}$
- $N_{sec1} = 11 \text{ T}$
- $N_{sec2} = 16 \text{ T}$

The outputs of the two secondary windings are calculated in Equation 5.

$$V_{SEC1} = 12V + I_1 \cdot DCR_{L1} + V_f = 12.7V \quad (\text{EQ. 5})$$

$$V_{SEC2} = 18V + I_2 \cdot DCR_{L2} + V_f = 18.75V$$

Based on Equation 5, the actual maximum duty cycle can be calculated as shown in Equation 6.

$$D_{max} = \frac{V_{sec1} \cdot N_p}{V_{in_{min}} \cdot N_{sec1}} = \frac{12.7 \cdot 8}{21.6 \cdot 11} \cong 0.43 \quad (\text{EQ. 6})$$

Now the actual maximum operation flux density can be computed using Equation 2, to be approximately 123mT. From the datasheet figures, the approximate core losses for a 120mT change in flux density is about 1.24W.

To determine the wire gauge for the windings, skin effect is an important consideration. The skin effect can be calculated as shown in Equation 7.

$$D_{Skin} = \frac{2837}{\sqrt{F_{sw}}} = \frac{2837}{\sqrt{300 \times 10^3}} = 5.18 \text{ mils} \quad (\text{EQ. 7})$$

Assuming a typical current density J_m of 1A per 500 circular mils, the minimum effective cross-sectional area of the primary windings can be computed to be 0.65, where I_{INAV} is the average input current, that can be computed with an assumed typical efficiency of 86%.

$$A_{min} = \frac{I_{in_{av}}}{J_m} = \frac{2.58 \cdot 500 \text{ cirmils}}{1A} = 0.65 \text{ mm}^2 \quad (\text{EQ. 8})$$

Using 2 layers of 27AWG bifilar windings for the primary winding, a current density of 1.6A per 500 circular mils can be achieved. On similar lines, 2 layers of 27AWG unifilar windings were used for the 12V output, and 1 layer of double-stranded 27AWG windings was used for the 18V output.

The copper losses can be estimated by calculating the DC and AC resistances, based on the core geometry and the size of the wires selected. A detailed evaluation gives a

copper loss estimate of about 0.68W. Assuming Eddy current losses to be approximately half the copper losses, the total loss in the transformer amounts to about 2.26W. The final transformer schematic is shown in Figure 4 and the stack-up of the windings is illustrated in Figure 5.

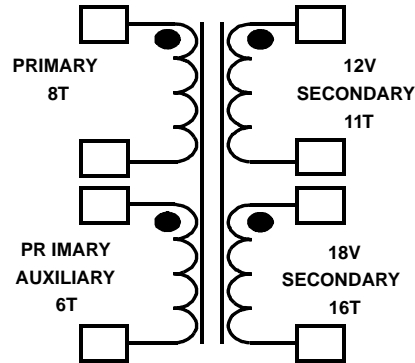


FIGURE 4. TRANSFORMER SCHEMATIC

8T X2 -27 AWG	PRIMARY – LAYER 1, PIN 2 TO 4
INSULATION TAPE	
16T X2 -27 AWG	SECONDARY 18V, PIN 7 TO 8
11T X1 -27 AWG	SECONDARY 12V, - LAYER 1
11T X1 -27 AWG	SECONDARY 12V, - LAYER 2
INSULATION TAPE	
6T X1 -30 AWG	PRIMARY – AUXILIARY WINDING
8T X2 -27 AWG	PRIMARY – LAYER 2, PIN 1 TO 3

FIGURE 5. TRANSFORMER WINDING STACK-UP

The main switching MOSFET was selected with consideration of voltage and current stresses seen by the device, and other factors such as thermal package and cost. The peak voltage was assumed to be twice the maximum input voltage, due to the ring during the resonant reset period at a frequency set primarily by the magnetizing and leakage inductance of the transformer, the output capacitance, C_{OSS} of the switching MOSFET, the transformer winding capacitance and other parasitic elements on the node. With a maximum specified input voltage of 52.8V, providing a design margin of 30%, a 150V device such as 2SK3593-01 need to be used. The MOSFET losses comprise of conduction, switching and gate drive losses. The conduction losses due to the FET r_{dsON} can be estimated as shown in Equation 9:

$$P_{cond} = I_{in_{RMS_{max}}}^2 \cdot R_{dsON} = 2.58^2 \cdot 37.5m\Omega = 250 \text{ mW} \quad (\text{EQ. 9})$$

The switching losses due to the overlap between the voltage and current waveforms is about 890mW according to Equation 10, where x is typically a factor between 4 and 6.

$$P_{sw} = V_{ds_{max}} \cdot \frac{I_{inRMS_{max}}}{D_{max}} \cdot F_{sw} \cdot \frac{(tr + tf)}{2 \cdot x} \quad (\text{EQ. 10})$$

$$= 105.6 \cdot \frac{2.58}{0.42} \cdot 300 \times 10^3 \cdot \frac{(30 + 25) \times 10^{-9}}{2 \cdot 6}$$

The gate charge loss is about 23mW according to Equation 11. The total MOSFET losses calculate out to be about 1.15W.

$$P_{gate} = Q_{g_{max}} \cdot V_{gs} \cdot F_{sw} = 7.8nC \cdot 10 \cdot 300 \times 10^3 = 23.5mW \quad (\text{EQ. 11})$$

Secondary Side Circuit Design

The output rectifiers need to have a low V_f at the output operating current to minimize the power loss, short reverse recovery period, and an appropriate peak breakdown voltage rating. The breakdown voltage can be estimated as shown in Equation 12.

$$V_R = \left(V_{in_{max}} \cdot \frac{N_{sec1}}{N_p} - V_f \right) \cdot 1.3 \quad (\text{EQ. 12})$$

Equation 12 yields a minimum voltage breakdown of voltage levels of 93.7V for the 12V rectifier, and 136.6V for the 18V diode selection. However, to account for the large di/dt spikes and the reflected resonant reset voltages observed, a 200V Schottky rectifier was selected for both outputs. A D2PAK package was selected for its low thermal resistance characteristics.

Assuming a junction temperature of +100°C, the forward drop on the diodes is about 0.48V according to the datasheet of the device. The full load diode loss is about 1.2W on the 12V output, and 0.48W on the 18V output rectifiers.

A ring of about 20MHz was observed on the diode waveforms. An RC snubber is needed on the 12V output across the freewheeling diode to provide sufficient damping. Based on the body capacitance of the diode, the snubber resistor can be selected as shown in Equation 13.

$$R_{sn} \cong \frac{1}{2 \cdot \pi \cdot f_{ring} \cdot C_{diode}} = \frac{1}{2 \cdot \pi \cdot 20MHz \cdot 500pF} = 15.91\Omega \quad (\text{EQ. 13})$$

A 20Ω resistor was selected for this application. The snubber capacitor was chosen based on the formula in Equation 14.

$$C_{sn} \cong \frac{1}{\pi \cdot f_{ring} \cdot R_{sn}} = \frac{1}{\pi \cdot 20MHz \cdot 20\Omega} = 796pF \quad (\text{EQ. 14})$$

An 820pF capacitor is used in this application. A 1Ω resistor is used to handle the power loss given by Equation 15.

$$P_{sn} = C \cdot V_{diode}^2 \cdot F_{sw} = 820pF \cdot 52.8^2 \cdot 300 \times 10^3 = 0.69W \quad (\text{EQ. 15})$$

The output filter inductor selection is pretty straightforward. Since the volt-second product across the inductor is constant, the output inductance can be calculated with either the on time or the off time. Assuming DI to be the minimum load at which the output is critically continuous at low line, the inductance value can be calculated as in Equation 16, where V_L is the inductor voltage, V_S is the voltage across the secondary winding, V_{OUT} is the output voltage.

$$L = \frac{\left(\frac{V_{in} \cdot N_s}{N_p} - V_f - V_o \right)}{\Delta I} \cdot \frac{D_{max}}{F_{sw}} \quad (\text{EQ. 16})$$

The border for continuous mode of conduction was set at 25% of full load on the 12V output and 20% on the 18V output at low line. Using Equation 16, the inductor values were chosen to be 39μH and 180μH respectively. These are off-the-shelf drum core, surface-mount shielded inductors. Care was taken to accommodate operation under an overcurrent condition before shutdown occurs. This is reflected in the current rating of the inductors selected.

Two important factors to consider while selecting the output capacitor would be the ripple current rating and the ESR. The worst-case pk-pk ripple current can be calculated from Equation 17 corresponding to high line voltage or minimum duty cycle. Using the inductance values selected, and providing a 50% margin, the maximum RMS ripple current, $\Delta I/\sqrt{3}$ calculates out to be about 0.98A on the 12V output and about 0.32A on the 18V rail. Using these numbers for RMS ripple current seen by the inductor and the maximum DCR numbers from the datasheet, the total I^2R losses across the chokes can be estimated at about 0.81W.

In order to keep the voltage ripple below 50mV, the maximum ESR of the capacitor can be calculated from Equation 17.

$$ESR \leq \frac{\text{VoltageRipple}}{\text{RippleCurrent}} \quad (\text{EQ. 17})$$

Providing a margin factor of 2 to compensate for increase in ESR over-temperature, the maximum allowable ESRs for the 12V and the 18V capacitors are 24mW and 88mW respectively. Since the outputs are regulated, the output voltage ratings on the capacitors selected are 16V and 25V respectively. Low ESR OSCONS were selected with high ripple current ratings, to account for the nature of the continually switching loads. Ceramic capacitors were added to share the stress on the filter capacitors, and for high frequency decoupling. The power losses estimation can be summarized in Table 1, and correspondingly the full load efficiency is about 87% at low line.

Application Note 1491

TABLE 1. POWER LOSS ANALYSIS

DEVICE	POWER DISSIPATED (WATTS)
Transformer	2.26
Rectifiers	1.68
Primary MOSFET	1.13
Chokes	0.81
Snubber	0.69
Fixed Control Estimate	0.5
Capacitors and CST	0.07
Total Loss Estimate	7.14

Feedback, OCP and Slope Compensation

Slope compensation is a technique to add additional slope to the current signal for current mode PWM with duty ratio larger than 50% to improve noise immunity. The downslope required is assumed to be 150mV during the off time, for a slope compensation corresponding to the maximum duty cycle of 42% (see Equation 18).

$$\text{Downslope} = \frac{150\text{mV} \cdot F_{\text{sw}}}{(1 - D_{\text{max}})} = \frac{150\text{mV} \cdot 300 \times 10^3}{(1 - 0.42)} \cong 78 \frac{\text{mV}}{\mu\text{s}} \quad (\text{EQ. 18})$$

The amount of voltage that needs to be added to the current sense signal is given by Equation 19.

$$V_{\text{slope}} = \frac{\text{Downslope}}{2} \cdot \frac{D_{\text{max}}}{F_{\text{sw}}} = \frac{1}{2} \cdot \frac{78}{1 \times 10^{-3}} \cdot \frac{0.42}{300 \times 10^3} \cong 55\text{mV} \quad (\text{EQ. 19})$$

From the datasheet, the minimum capacitance required for slope compensation is shown in Equation 20.

$$C_{\text{slope}_{\text{min}}} = \frac{4.24 \times 10^6}{V_{\text{slope}}} \cdot \frac{D_{\text{max}}}{F_{\text{sw}}} = \frac{4.24 \times 10^6}{55\text{mV}} \cdot \frac{0.42}{300 \times 10^3} \cong 108\text{pF} \quad (\text{EQ. 20})$$

An appropriate value for slope compensation capacitance would be between 1/2 and 1/3 of the calculated minimum value, giving a range between 36pF and 53pF. The effective slope voltage added to the current sense signal can be calculated according to Equation 19, which is about 160mV with the equivalent capacitance 47pF.

The current level that corresponds to the overcurrent threshold must be chosen to allow for the dynamic behavior of a wide-input voltage range converter. The current limit threshold, ISET was set using a simple resistor divider at 1.07V, which is near its maximum value, in order to minimize noise effects. Setting the current limit to about 130% of maximum output power, corresponding to maximum duty cycle or low line, the current sense components can be calculated as follows in Equation 21.

Selecting a current sense transformer with a turns ratio of 1:50, the burden resistor needs to be set, taking into

$$I_{\text{OCP}} = I_{\text{in}_{\text{peak}}} \cdot 1.3 = \frac{I_{\text{inRMS}_{\text{max}}} \cdot 1.3}{D_{\text{max}}} = \frac{2.58 \cdot 1.3}{0.43} = 7.8\text{A} \quad (\text{EQ. 21})$$

account the additional voltage on the current sense signal induced by the slope compensation s shown in Equation 22.

$$V_{\text{ISET}} = (V_{\text{ISENSE}} \cdot 0.8) + 0.1 + V_{\text{slope}} \quad (\text{EQ. 22})$$

From Equation 17, V_{ISENSE} needs to be about 1.015V. The current sense resistor can be selected according to Equation 23.

$$R_{\text{sense}} = \frac{V_{\text{ISENSE}} \cdot N_{\text{CST}}}{I_{\text{OCP}}} = \frac{1.015 \cdot 50}{7.8} = 6.5\Omega \quad (\text{EQ. 23})$$

A 6.49Ω, 1% resistor can be used. The current sense signal is filtered by means of an RC filter, with a detection time constant of about 100ns.

The small signal model for multiple-output current mode control and the compensation network design is available in the ISL6721 datasheet. The feedback of the two outputs has been weighted at 80-20% between the 12V and 18V, to provide the 12V rail with the tighter regulation.

Typical Performance Characteristics

The major performance will be examined in terms of efficiency, and load/line regulation, and shown in Tables 2 through 4 for input voltages $V_{IN} = 22V$, $34V$ and $52.8V$, respectively.

The performance closely matches the design specifications. While the efficiency varies over different combinations of line and load, the full-load efficiency target of 80% has been comfortably met under all input voltage conditions. As expected, the worst regulation is seen at extreme input voltage conditions, and when one rail is at full load with the other rail at minimum load. Since the feedback has been weighted at 80% to 20% between the 12V and 18V, to provide the 12V rail with the tighter regulation. The regulation of the 18V output is well maintained for normal operation conditions, while becomes loose as either one of the outputs is less than 20% of full load.

TABLE 2. REGULATION AND EFFICIENCY - $V_{IN} = 21.6V$

$V_{IN} = 21.6V$					
I_{OUT1} (A)	I_{OUT2} (A)	V_{OUT1} (V)	V_{OUT2} (V)	I_{IN} (A)	EFFICIENCY (%)
0.5	0.2	11.989	17.779	0.5110	86.53
0.5	0.4	12.003	17.677	0.6830	88.61
1.0	0.2	11.978	17.919	0.8110	88.84
0.5	0.6	12.013	17.598	0.8570	89.49
1.0	0.4	11.989	17.823	0.9880	89.59
0.5	0.8	12.022	17.524	1.0310	89.94
1.5	0.2	11.963	18.029	1.1220	88.92
1.0	0.6	11.997	17.744	1.1690	89.68
0.5	1.0	12.031	17.449	1.2110	89.70
1.5	0.4	11.977	17.935	1.3061	89.11
1.0	0.8	12.003	17.673	1.3490	89.71
2.0	0.2	11.957	18.165	1.4440	88.32
1.5	0.6	11.988	17.859	1.4930	88.99
1.0	1.0	12.009	17.606	1.5360	89.26
2.0	0.4	11.969	18.049	1.6340	88.28
1.5	0.8	11.997	17.788	1.6800	88.81
2.5	0.2	11.937	18.314	1.7790	87.19
2.0	0.6	11.979	17.967	1.8270	88.03
1.5	1.0	12.005	17.719	1.8730	88.31
2.5	0.4	11.954	18.166	1.9760	87.04
2.0	0.8	11.987	17.895	2.0210	87.71
2.5	0.6	11.966	18.077	2.1780	86.64
2.0	1.0	11.995	17.826	2.2220	87.13
2.5	0.8	11.974	18.005	2.3790	86.29
2.5	1.0	11.983	17.936	2.5890	85.64

TABLE 3. REGULATION AND EFFICIENCY - $V_{IN} = 34V$

$V_{IN} = 34.0V$					
I_{OUT1} (A)	I_{OUT2} (A)	V_{OUT1} (V)	V_{OUT2} (V)	I_{IN} (A)	EFFICIENCY (%)
0.5	0.2	12.021	17.800	0.3580	78.63
0.5	0.4	12.012	17.663	0.4720	81.45
1.0	0.2	11.982	17.925	0.5570	82.20
0.5	0.6	12.022	17.578	0.5860	83.10
1.0	0.4	11.996	17.813	0.6720	83.69
0.5	0.8	12.031	17.503	0.7000	84.11
1.5	0.2	11.917	18.026	0.7610	83.02
1.0	0.6	12.004	17.737	0.8580	77.63
0.5	1.0	12.038	17.427	0.8160	84.51
1.5	0.4	11.983	17.924	0.8790	84.13
1.0	0.8	12.011	17.668	0.9060	84.88
2.0	0.2	11.956	18.134	0.9680	83.67
1.5	0.6	11.991	17.845	0.9980	84.56
1.0	1.0	12.015	17.600	1.0260	84.90
2.0	0.4	11.968	18.025	1.0890	84.12
1.5	0.8	11.998	17.775	1.1170	84.83
2.5	0.2	11.943	18.281	1.1829	83.33
2.0	0.6	11.977	17.945	1.2110	84.33
1.5	1.0	12.004	17.706	1.2400	84.71
2.5	0.4	11.957	18.137	1.3060	83.66
2.0	0.8	11.983	17.873	1.3330	84.43
2.5	0.6	11.965	18.053	1.4310	83.74
2.0	1.0	11.990	17.803	1.4580	84.29
2.5	0.8	11.972	17.980	1.5550	83.82
2.5	1.0	11.978	17.909	1.6830	83.63

TABLE 4. REGULATION AND EFFICIENCY - $V_{IN} = 52.8V$

$V_{IN} = 52.8V$					
I_{OUT1} (A)	I_{OUT2} (A)	V_{OUT1} (V)	V_{OUT2} (V)	I_{IN} (A)	EFFICIENCY (%)
0.5	0.2	12.010	17.823	0.2590	69.98
0.5	0.4	12.027	17.677	0.3320	74.64
1.0	0.2	11.993	17.955	0.3870	76.27
0.5	0.6	12.040	17.557	0.4060	77.22
1.0	0.4	12.012	17.806	0.4620	78.44
0.5	0.8	12.050	17.447	0.4790	79.01
1.5	0.2	11.984	18.041	0.5200	78.61
1.0	0.6	12.024	17.712	0.5380	79.74
0.5	1.0	12.054	17.342	0.5530	80.04
1.5	0.4	12.001	17.904	0.5960	79.96
1.0	0.8	12.030	17.638	0.6130	80.76

TABLE 4. REGULATION AND EFFICIENCY - $V_{IN} = 52.8V$ (Continued)

$V_{IN} = 52.8V$					
I_{OUT1} (A)	I_{OUT2} (A)	V_{OUT1} (V)	V_{OUT2} (V)	I_{IN} (A)	EFFICIENCY (%)
2.0	0.2	11.968	18.140	0.6540	79.82
1.5	0.6	12.010	17.828	0.6730	80.80
1.0	1.0	12.033	17.560	0.6890	81.35
2.0	0.4	11.983	18.014	0.7310	80.76
1.5	0.8	12.015	17.757	0.7490	81.49
2.5	0.2	11.942	18.259	0.7910	80.23
2.0	0.6	11.991	17.934	0.8090	81.33
1.5	1.0	12.018	17.683	0.8270	81.78
2.5	0.4	11.960	18.111	0.8680	81.05
2.0	0.8	11.999	17.866	0.8860	81.85
2.5	0.6	11.967	18.027	0.9470	81.46
2.0	1.0	12.006	17.794	0.9650	82.05
2.5	0.8	11.970	17.950	1.0250	81.83
2.5	1.0	11.970	17.877	1.1040	82.01

Operation Waveforms

The schematics and bill of material are shown at the end of this application note. Gerber files of this evaluation board are available upon request. Typical performance waveforms can be found in Figures 6 through 9.

Figure 6 shows the start-up waveform of the output voltages of the two rails, 12V and 18V. With the external soft-start up capacitor, this period can be configured conveniently. Figures 7, 8 and 9 show the drain-source voltages of the primary side MOSFET for input 25V and 50V, respectively. The three intervals of operations can be easily observed.

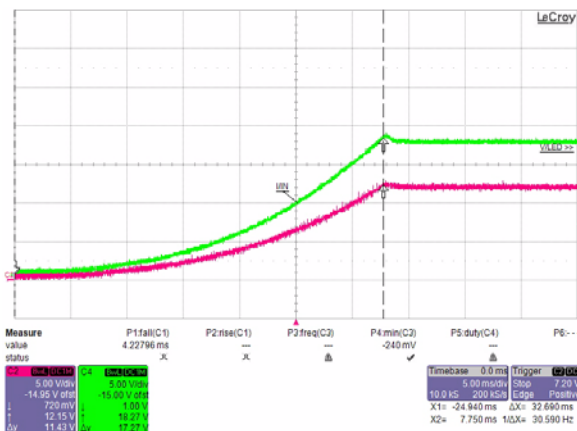


FIGURE 6. START-UP WITH 32V INPUT, $I_{OUT1} = 2A$, $I_{OUT2} = 1A$

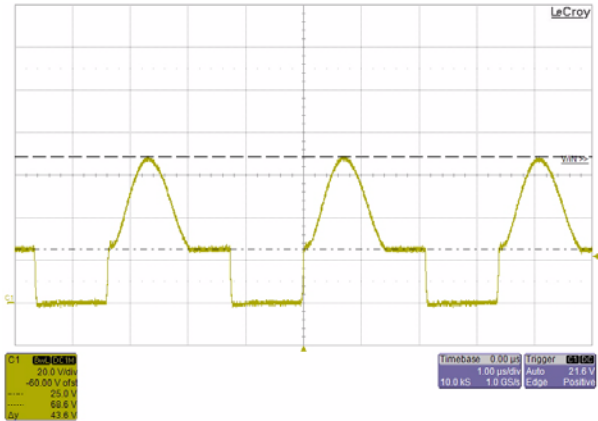


FIGURE 7. DRAIN-SOURCE VOLTAGE FOR $V_{IN} = 25V$, $I_{LOAD12V} = 0.5A$, $I_{LOAD18V} = 0.5A$

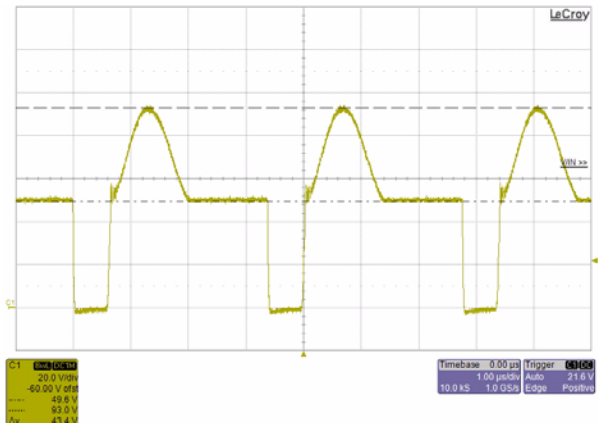


FIGURE 8. DRAIN SOURCE VOLTAGE FOR $V_{IN} = 50V$, $I_{LOAD12V} = 0.5A$, $I_{LOAD18V} = 0.5A$

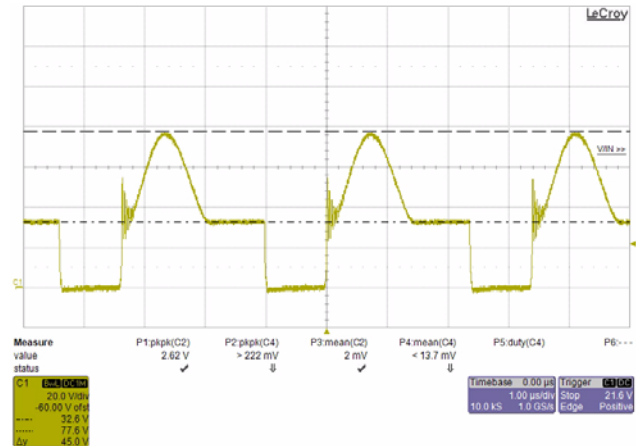


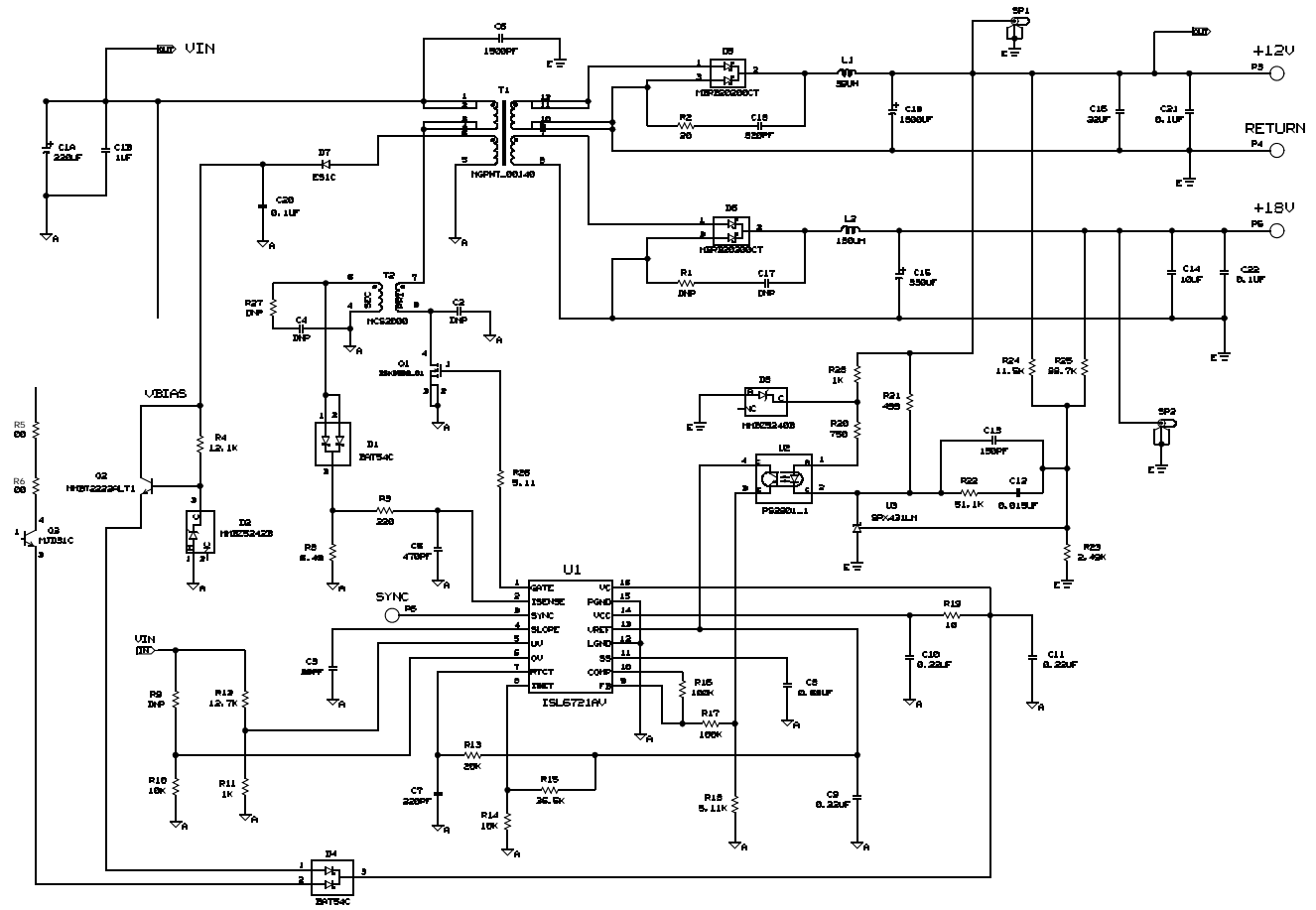
FIGURE 9. DRAIN-SOURCE VOLTAGE FOR $V_{IN} = 32V$, $I_{LOAD12V} = 2A$, $I_{LOAD18V} = 1A$

Reference:

ISL6721 datasheet FN9110, Intersil Corporation

ISL6745 datasheet FN9161, Intersil Corporation

Schematic of ISL6721EVAL3



Application Note 1491

TABLE 5. BILL OF MATERIALS

PART NUMBER	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MFR
ISL6721EVAL3Z	1	ea		PWB-PCB, ISL6721EVAL3Z, REVA, ROHS	TBD
16ME1800WG	1	ea	C19	RADIAL, 10x23, 1800µF, 16V, 20%, 12mW, ALUM. ELEC., ROHS	SANYO
35ME330AX	1	ea	C15	CAP, RADIAL, 10x20mm, 330µF, 35V, 20%, ALUM. ELEC., ROHS	SANYO
C3225X7R1C226M-T	1	ea	C16	CAP, SMD, 1210, 22µF, 16V, 2 0%, X7R, ROHS	TDK
C3225X7R1E106M-T	1	ea	C14	CAP, SMD, 1210, 10µF, 25V, 20%, X7R, ROHS	TDK
C3225X7R2A105M-T	1	ea	C1B	CAP, SMD, 1210, 1.0µF, 100V, 20%, X7R, ROHS	TDK
EEV-FK1J221Q	1	ea	C1A	CAP, SMD, H13, 220µF, 63V, 2 0%, ALUM. ELEC	PANASONIC
H1045-0010425V10T	3	ea	C20 to C22	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	MURATA
H1045-00151-50V5-T	1	ea	C13	CAP, SMD, 0603, 150pF, 50V, 5%, NPO, ROHS	PANASONIC
H1045-00153-25V10T	1	ea	C12	CAP, SMD, 0603, 0.015µF, 25V, 10%, X7R, ROHS	PANASONIC
H1045-00221-100V5-T	1	ea	C7	CAP, SMD, 0603, 220pF, 100V, 5%, C0G, ROHS	VENKEL
H1045-00224-25V20-T	3	ea	C9 to C11	CAP, SMD, 0603, 0.22µF, 25V, 20%, X7R, ROHS	VENKEL
H1045-00390-50V5-T	1	ea	C3	CAP, SMD, 0603, 39pF, 50V, 5%, NPO, ROHS	PANASONIC
H1045-00471-50V5-T	1	ea	C5	CAP, SMD, 0603, 470pF, 50V, 5%, NPO, ROHS	PANASONIC
H1045-00684-10V10-T	1	ea	C8	CAP, SMD, 0603, 0.68µF, 10V, 10%, X5R, ROHS	MURATA
H1046-00471-100V5-T	1	ea	C18	CAP, SMD, 0805, 470pF, 100V, 5%, NPO, ROHS	PANASONIC
GA355DR7GC152KY0L	1	ea	C6	CAP, SMD, 2220, 1500pF, 250V, 10%, X7R, ROHS	MURATA
MHS5022-390-TM	1	ea	L1	COIL-PWR INDUCTOR, SMD, 16x22, 39µH, 20%, 4A, 0.0860W	MSR ELECTRONICS,INC
MOS-5022-181-TM	1	ea	L2	COIL-PWR INDUCTOR, SMD, 18x15, 180µH, 20%, 1.9A, SHILED	MSR ELECTRONICS,INC
131-4353-00	0	ea	DNP	CONN-SCOPE PROBE TEST PT, COMPACT, PCB MNT, ROHS	TEKTRONIX
1514-2	6	ea	P1 to P6	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE
BAT54C-T	2	ea	D1, D4	DIODE-RECTIFIER, SMD, SOT23, 3P, 30V, 200mA, ROHS	FAIRCHILD
ES1C-13-F	1	ea	D7	DIODE-RECTIFIER, SMD, 2P, SMA, 150V, 1A, ROHS	DIODES INC.
MBRB20200CTG	2	ea	D5, D6	DIODE-RECTIFIER, SMD, D2PAK, 3P, 200V, 20A, ROHS	ON SEMICONDUCTOR
MMBZ5240B-7-F-T	2	ea	D3, D8	DIODE-ZENER, SMD, SOT-23, 3P, 10V, 350mW, ROHS	DIODES INC.
MMBZ5242B-7-F-T	1	ea	D2	DIODE-ZENER, SMD, SOT-23, 3P, 12V, 350mW, ROHS	DIODES, INC.
ISL6721AVZ	1	ea	U1	IC-FLEXIBLE PWM CONTROLLER, 16P, TSSOP, ROHS	INTERSIL
PS2801-1-A	1	ea	U2	IC-HI ISO PHOTOCOUPLER, 4P, SSOP, ROHS	CALIFORNIA EASTERN LABORATORIES
SPX431LM-L	1	ea	U3	IC-ADJ. PREC.SHUNT REGULATOR, 3P, SOT-23, ROHS	SIPEX
2SK3593-01	1	ea	Q1	TRANSISTOR-MOS, N-CHANNEL, SMD, TFP, 150V, 57A, ROHS	FUJI ELECTRIC
MJD31CG	1	ea	Q3	TRANSISTOR, NPN, 3P, DPAK369C, 100V, 3A, BIPOLAR, ROHS	ON SEMICONDUCTOR
MMBT2222ALT1G-T	1	ea	Q2	TRANSISTOR, NPN, 3LD, SOT23, 40V, 600mA, ROHS	
H2511-00100-1/16W1-T	1	ea	R19	RES, SMD, 0603, 10W, 1/16W, 1%, TF, ROHS	PANASONIC

Application Note 1491

PART NUMBER	QTY	UNIT	REFERENCE DESIGNATOR	DESCRIPTION	MFR
H2511-01001-1/10W1-T	1	ea	R11	RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	PANASONIC
H2511-01002-1/10W1-T	2	ea	R10, R14	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA
H2511-01003-1/16W1-T	2	ea	R16, R17	RES, SMD, 0603, 100k, 1/16W, 1%, TF, ROHS	PANASONIC
H2511-01152-1/16W1-T	1	ea	R24	RES, SMD, 0603, 11.5k, 1/16W, 1%, TF, ROHS	PANASONIC
H2511-01212-1/16W1-T	1	ea	R4	RES, SMD, 0603, 12.1k, 1/16W, 1%, TF, ROHS	PANASONIC
H2511-01272-1/16W1-T	1	ea	R12	RES, SMD, 0603, 12.7k, 1/16W, 1%, TF, ROHS	PANASONIC
H2511-02002-1/10W1-T	1	ea	R13	RES, SMD, 0603, 20k, 1/10W, 1%, TF, ROHS	VENKEL
H2511-02200-1/10W1-T	1	ea	R3	RES, SMD, 0603, 220W, 1/10W, 1%, TF, ROHS	YAGEO
H2511-02491-1/10W1-T	1	ea	R23	RES, SMD, 0603, 2.49k, 1/10W, 1%, TF, ROHS	KOA
H2511-03652-1/16W1-T	1	ea	R15	RES, SMD, 0603, 36.5k, 1/16W, 1%, TF, ROHS	PANASONIC
H2511-04990-1/10W1-T	1	ea	R21	RES, SMD, 0603, 499W, 1/10W, 1%, TF, ROHS	KOA
H2511-05111-1/16W1-T	1	ea	R18	RES, SMD, 0603, 5.11k, 1/16W, 1%, TF, ROHS	PANASONIC
H2511-05112-1/10W1-T	2	ea	R7, R22	RES, SMD, 0603, 51.1k, 1/10W, 1%, TF, ROHS	VENKEL
H2511-05R11-1/10W1-T	1	ea	R26	RES, SMD, 0603, 5.11W, 1/10W, 1%, TF, ROHS	YAGEO
H2511-06R49-1/10W1-T	1	ea	R8	RES, SMD, 0603, 6.49W, 1/10W, 1%, TF, ROHS	VENKEL
H2511-07500-1/10W1-T	1	ea	R20	RES, SMD, 0603, 750W, 1/10W, 1%, TF, ROHS	VENKEL
H2511-08872-1/16W1-T	1	ea	R25	RES, SMD, 0603, 88.7k, 1/16W, 1%, TF, ROHS	PANASONIC
H2512-01001-1/10W1-T	1	ea	R28	RES, SMD, 0805, 1k, 1/10W, 1%, TF, ROHS	PANASONIC
H2513-01000-1/4W1-T	2	ea	R5, R6	RES, SMD, 1206, 100W, 1/4W, 1%, TF, ROHS	STACKPOLE
H2515-00200-1W5	1	ea	R2	RES, SMD, 2512, 20W, 1W, 5%, TF, ROHS	
MCS-2050-TM	1	ea	T2	TRANSFORM-CURRENT SENSE, SMD, 6P, 0.7mH, 25%, 20A	MSR ELECTRONICS,INC
MGPWT-00140-REVA	1	ea	T1	TRANSFORMER-SMD, 12P, 90μH, 30%, CUSTOM REVA, ROHS	CoEV/TYCO
SJ-5003-BLACK	4	ea	Four Corners.	BUMPONS, 0.44in Wx0.20in H, DOMETOP, BLACK	3M
8x12-STATIC-BAG	1	ea	Place Assembled PCB in Bag.	BAG, STATIC, 8x12, ZIP LOC	INTERSIL COMMON STOCK
DNP	0	ea	C2, C4, C17	DO NOT POPULATE OR PURCHASE	
DNP	0	ea	R1, R9, R2	DO NOT POPULATE OR PURCHASE	
LABEL-SERIAL NUMBER	1	ea		LABEL, FOR SERIAL NUMBER AND BOM REV #	

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

For information regarding Intersil Corporation and its products, see www.intersil.com