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ZL9101EVAL1Z Digital DC/DC 12A Module Evaluation Board

Description

The ZL9101M is a 12A variable output, step-down power supply module. Included in the module is a high-performance digital PWM controller, power MOSFETs, an inductor, and all the passive components required for a complete DC/DC power solution. The ZL9101M operates over a wide input voltage range and supports an output voltage range of 0.6V to 4V, which can be set by external resistors or via the PMBus. This high-efficiency power module is capable of delivering 12A. Only bulk input and output capacitors are needed to finish the design. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation.

The ZL9101EVAL1Z is a 6-layer board that provides a single-phase power rail up to 12A loads. The board is designed to efficiently transfer heat away from the module with passive cooling.

A USB to SMBus adapter is used to connect the ZL9101EVAL1Z board to a PC. The PMBus command set is accessed by using the PowerNavigator™ evaluation software.

Key Features

- Complete Switch Mode Power Supply
- 12A DC Output Current
- Adjustable +0.6V to +4V Output Range
- Up to 90% Efficiency
- Digital Control PWM
- Fixed 615kHz Switching Frequency
- Fast Transient Response
- Enable Function Option
- Power-Good Indicator
- Convenient Power Connection
- Multiple Power Options
- Single Supply Operation
- Configurable Through SMBus

Key Specifications

The ZL9101EVAL1Z has been designed and optimized for the following parameters:

- V_{IN} = 12V
- V_{OUT} = 1.2V
- $I_{OUT(MAX)}$ = 15A
- F_{SW} = 615kHz
- $V_{OUT(RIPPLE)}$ < 1%
- Transient Response = 3% (3A to 9A step at 2.5V/µs)

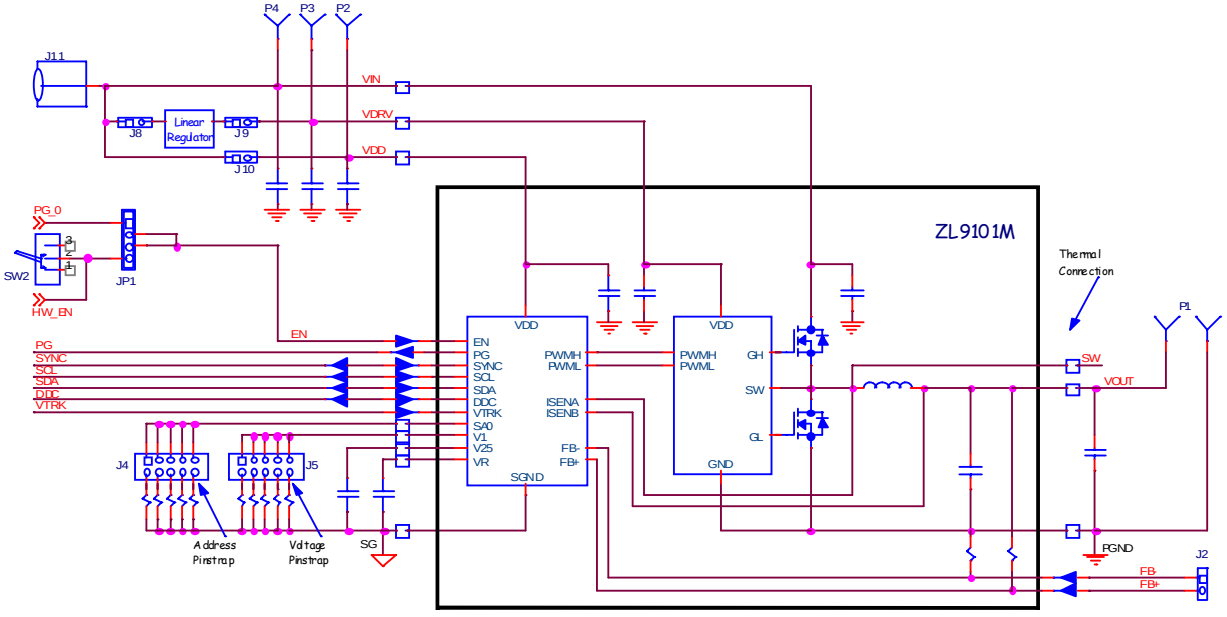

FIGURE 1. ZL9101EVAL1Z EVALUATION BOARD BLOCK DIAGRAM

Functional Description

The ZL9101EVAL1Z evaluation board provides all the circuitry required to evaluate the features of the ZL9101M module. The ZL9101EVAL1Z has a performance-optimized, single-phase ZL9101M circuit layout that allows operation up to the maximum rated output current. Power options and load connections are provided through plug-in sockets and shorting jumpers.

Figure 1 shows a functional block diagram of the ZL9101EVAL1Z board. The SMBus address is selectable through J4 located on the top side of the board. All power to the board (V_{IN} and I^2C bus) must be removed before changing the jumpers.

The hardware enable function is controlled by a toggle switch on the ZL9101EVAL1Z board. The power-good (PG) LED indicates the state of PG when external power is applied to the ZL9101EVAL1Z board. The right-angle headers at opposite ends of the board are for connecting a USB to an SMBus adapter board or for daisy-chaining of multiple evaluation boards.

Figure 2 shows the ZL9101EVAL1Z operational circuit. The circuit consists of the ZL9101M module and supporting components.

Figure 3 shows the ZL9101EVAL1Z interface schematic.

Figures 4 through 9 show the layers of the ZL9101EVAL1Z evaluation board.

Basic Operation

The ZL9101EVAL1Z evaluation board is easy to set up and operate. It is optimally configured, out of the box, to provide 1.2V at 12A from a 12V source. All input and output connections should be made before applying power.

The ZL9101M module requires a configuration file in order to operate. The ZL9101M supports pinstrap configuration for output voltage and SMBus address. All other parameters must be configured with a text-based configuration file. See application note AN2031 for more information on writing configuration files. An example configuration file is listed at the end of this document.

Pinstraps

The ZL9101M requires a configuration file for normal operation; however, there are two pinstrap functions to be configured: Voltage and SMBus address. Ensure that input power is removed, and then set the address and voltage pinstraps using J4 and J6. Apply V_{DD} power, and the new settings will be in effect.

PMBus Operation

The ZL9101M utilizes the PMBus protocol. The PMBus functionality can be controlled via USB from a PC running the PowerNavigator™ evaluation software in a Windows XP or Windows 2000/NT operating system.

Install the PowerNavigator™ software using the CD included in the ZL9101EVAL1Z kit. For PMBus operation, connect the USB-to-SMBus dongle board to J7 of the ZL9101EVAL1Z board. Connect the desired load and an appropriate power supply to the input. Place the ENABLE switch in “DISABLE” and turn on the power. The PowerNavigator™ evaluation software allows modification of all ZL9101M PMBus parameters. See Application Note AN2033 for PMBus command details. Use the mouse-over pop-ups for PowerNavigator™ help. Manually configure the ZL9101M through PowerNavigator™ or load a predefined scenario from a configuration file.

The ENABLE switch can then be moved to “ENABLE” and the ZL9101M can be tested. Alternately, the PMBus ONOFF, CONFIG, and OPERATION commands can be used.

Single-Supply Operation

The ZL9101EVAL1Z board was designed to facilitate operation from a single power supply input. The single input power mode reduces the number of connections but results in a minor reduction of efficiency.

The driver bias is supplied by an onboard linear regulator. Figure 3 shows the onboard regulator circuit for powering the ZL9101M driver. Jumpers J8 and J9 connect the supply power to the linear regulator that is used to power the driver, and J6 connects input power to the ZL9101M digital module. If single-supply operation is desired, J6, J8, and J9 must be installed.

Multi-Supply Operation (External Driver Supply)

To operate the ZL9101EVAL1Z driver from an external power supply, remove J8 and J9, and connect an external power supply to the driver connector, P3, between 4.5V to 6.5V.

To operate the ZL9101EVAL1Z board using different power supplies for the controller and FETs, remove J6 and apply an external power supply to power the FETs to P4 to between 3.0V and 14V.

Apply a power supply voltage to the ZL9101M module through the P2 connector.

If the V_{DD} voltage is $4.5V \le V_{DD} \le 5.5V$, then apply 4.5V to 5.5V to P2, and connect V_R to V_{DD}. Do not exceed 5.5V while V_R is connected to V_{DD} or permanent damage will result.

If the V_{DD} voltage is $5.5V \le V_{DD} \le 14V$, then apply 5.5V to 14V to P2, and do not connect to V_R.

The ZL9101EVAL1Z comes configured to use hardware Enable. Toggle the power switch to the Enable position to power on. Use the GUI to change the configuration, if desired.

Power Good

The ZL9101M provides a Power-Good (PG) signal, which indicates that the output voltage is within a specified tolerance of its target level and that no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the polarity of the pin may be changed via the I^2C/SMBus interface. See Application Note AN2033 for details.

A PG delay period is defined as the time from when all conditions within the ZL9101M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL9101M PG delay is set equal to the soft-start ramp time setting of 10ms. The PG delay may be set independently of the soft-start ramp by using the I^2C/SMBus as described in Application Note AN2033.

Switching Frequency and PLL

The ZL9101M incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin via J7 or J14. When using the internal oscillator, the SYNC pin can be configured as a clock source.

The internal switching frequency of the ZL9101M is 615kHz. Operation below 615kHz will increase the inductor ripple current and cause permanent damage.

Loop Compensation

The ZL9101M operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. The module is internally compensated via the I^2C/SMBus interface. The PID settings are included in the configuration file stored on the ZL9101M; the settings are shown in "Default Configuration File" on page 6 for reference. The compensation tool, CompZL™ can be used to generate appropriate PID settings for other circuit configurations.

Adaptive Diode Emulation

Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, thus reducing energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

NOTE: The overall bandwidth of the device may be reduced when in diode emulation mode. It is recommended that diode emulation be disabled prior to applying significant load steps.

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL9101M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device remains in shutdown until instructed to restart.

Connectors and Jumpers

Connector and jumpers are shown in Figure 10.

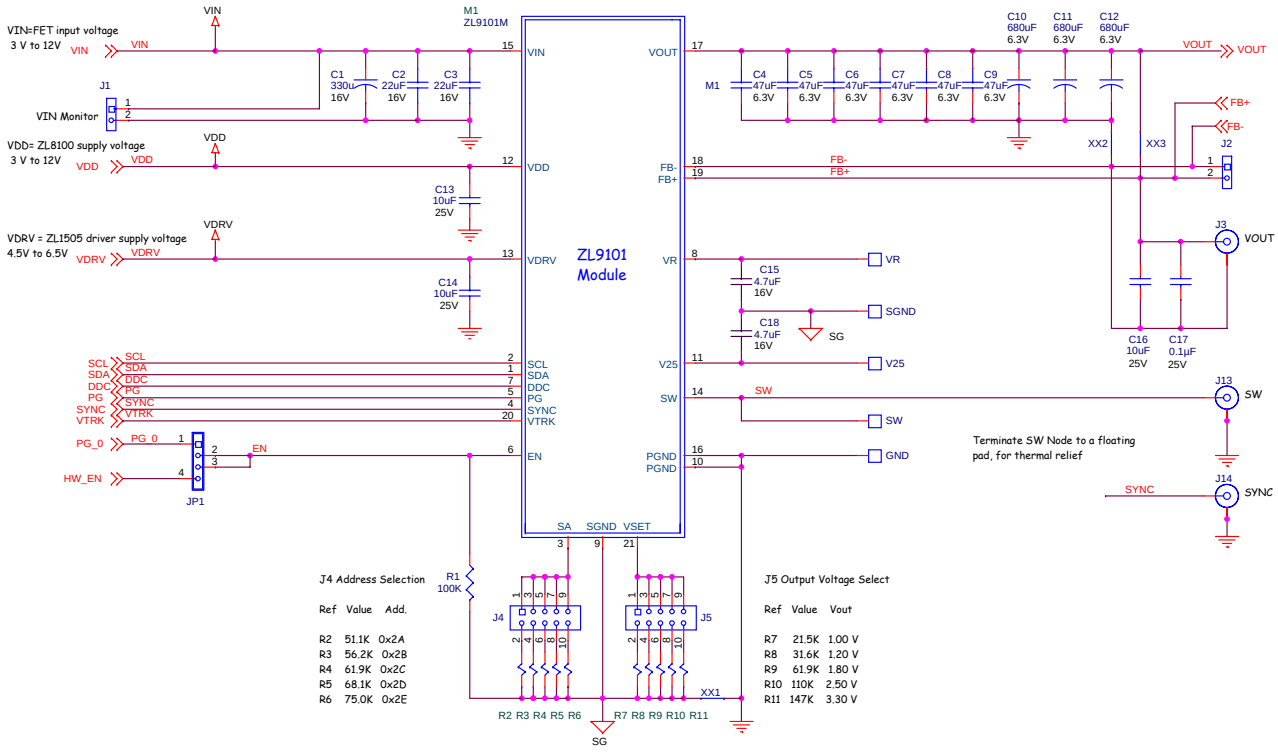

FIGURE 2. ZL9101EVAL1Z CIRCUIT SCHEMATIC

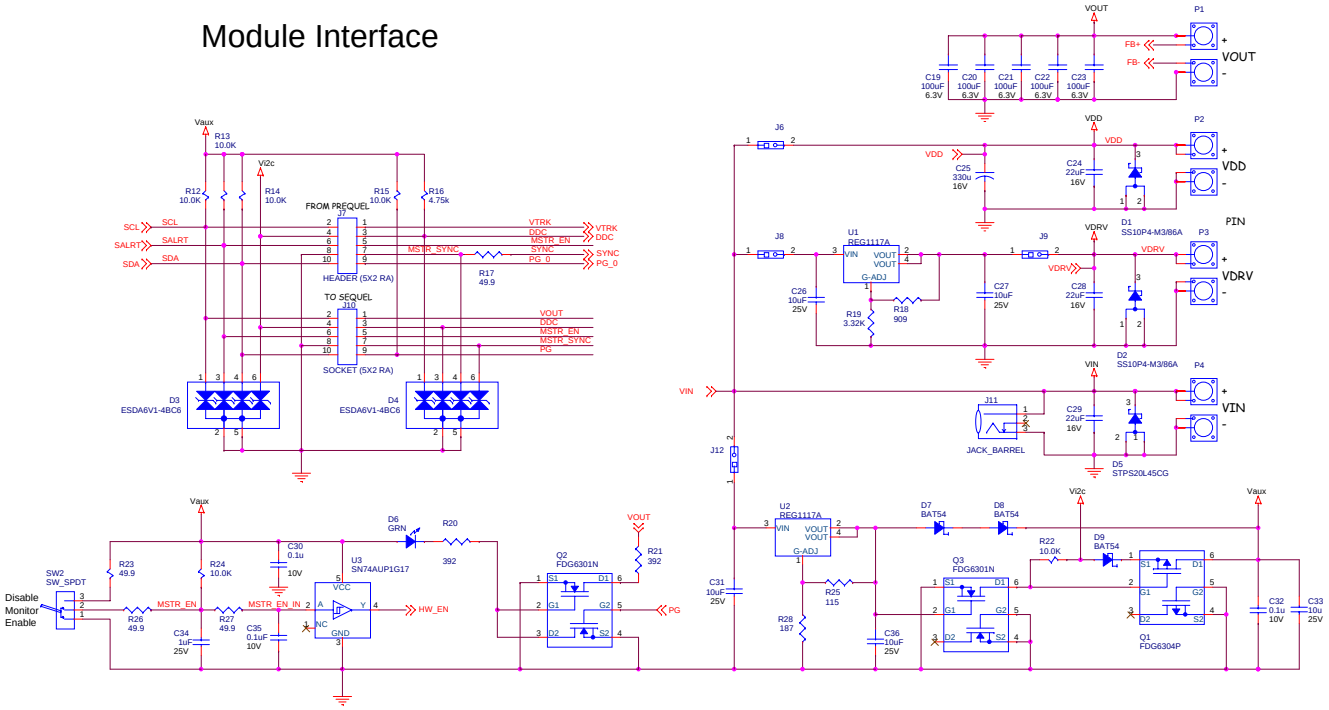

FIGURE 3. ZL9101EVAL1Z INTERFACE SCHEMATIC

Default Configuration File

The following text is loaded into the ZL9101M devices on the ZL9101EVAL1Z evaluation board as the default settings. This configuration file can be loaded using the PowerNavigator™ software, ConfigCheck™ software, or a user-created application. The # symbol denotes a comment line.

```
# Intersil ZL9101M 12/20/2010
# ZL Configuration File Revision 2
# Schematic revision level
# BOM revision level
# ZL Author
# Change log:

RESTORE_FACTORY
STORE_DEFAULT_ALL
STORE_USER_ALL
RESTORE_DEFAULT_ALL
```

MFR_ID	Intersil
MFR_MODEL	ZL9101EVAL1Z
MFR_REVISION	REV_2.0
MFR_LOCATION	Austin
MFR_DATE	12_20_2010
MFR_SERIAL	1p2V_15A
ON_OFF_CONFIG	0x1A
#VOUT_COMMAND	
#VOUT_OV_FAULT_LIMIT	
#VOUT_MAX	
#VOUT_UV_FAULT_LIMIT	
#VOUT_MARGIN_HIGH	
#VOUT_MARGIN_LOW	
#VOUT_DROOP	
#POWER_GOOD_ON	5
#POWER_GOOD_DELAY	5
IOUT_SCALE	1.556
IOUT_CAL_OFFSET	-2.30
TON_DELAY	5
TON_RISE	5
TOFF_DELAY	5
TOFF_FALL	5
FREQUENCY_SWITCH	615
VOUT_OV_FAULT_RESPONSE	0x80
VOUT_UV_FAULT_RESPONSE	0x80
OVUV_CONFIG	0x80
IOUT_OC_FAULT_LIMIT	25
IOUT_AVG_OC_FAULT_LIMIT	25

IOUT_UC_FAULT_LIMIT	-20
IOUT_AVG_UC_FAULT_LIMIT	-20
MFR_IOUT_OC_FAULT_RESPONSE	0x80
MFR_IOUT_UC_FAULT_RESPONSE	0x80
MFR_VMON_OV_FAULT_LIMIT	7.0
VMON_OV_FAULT_RESPONSE	0x80
MFR_VMON_UV_FAULT_LIMIT	4.5
VMON_UV_FAULT_RESPONSE	0x80
VIN_OV_WARN_LIMIT	14.3
VIN_OV_FAULT_LIMIT	14.5
VIN_OV_FAULT_RESPONSE	0x80
VIN_UV_WARN_LIMIT	4.2
VIN_UV_FAULT_LIMIT	4.0
VIN_UV_FAULT_RESPONSE	0x80
OT_WARN_LIMIT	110.0
OT_FAULT_LIMIT	125
OT_FAULT_RESPONSE	0x80
UT_WARN_LIMIT	-20
UT_FAULT_LIMIT	-40
UT_FAULT_RESPONSE	0x00
PID_TAPS	A=16133.25, B=-27119.00, C=10998.50
DEADTIME	0x3838
DEADTIME_CONFIG	0x8C06
DEADTIME_MAX	0x2828
MAX_DUTY	92
#TRACK_CONFIG	
#XTEMP_SCALE	1.0
#XTEMP_OFFSET	10.0
MFR_CONFIG	0x8311
NLR_CONFIG	0x00000000
USER_CONFIG	0x0031
TEMPCO_CONFIG	0x28
MISC_CONFIG	0x8880
ISHARE_CONFIG	0x0000
INTERLEAVE	0x0000
SEQUENCE	0x0000
DDC_GROUP	0x00000000
DDC_CONFIG	0x0000
INDUCTOR	0.30

STORE_DEFAULT_ALL

RESTORE_DEFAULT_ALL

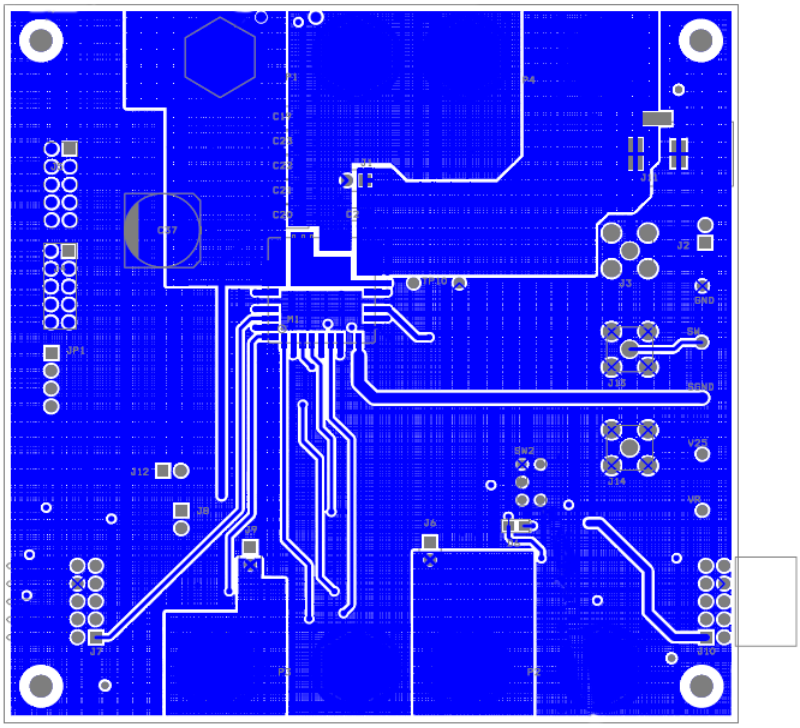

FIGURE 4. TOP LAYER

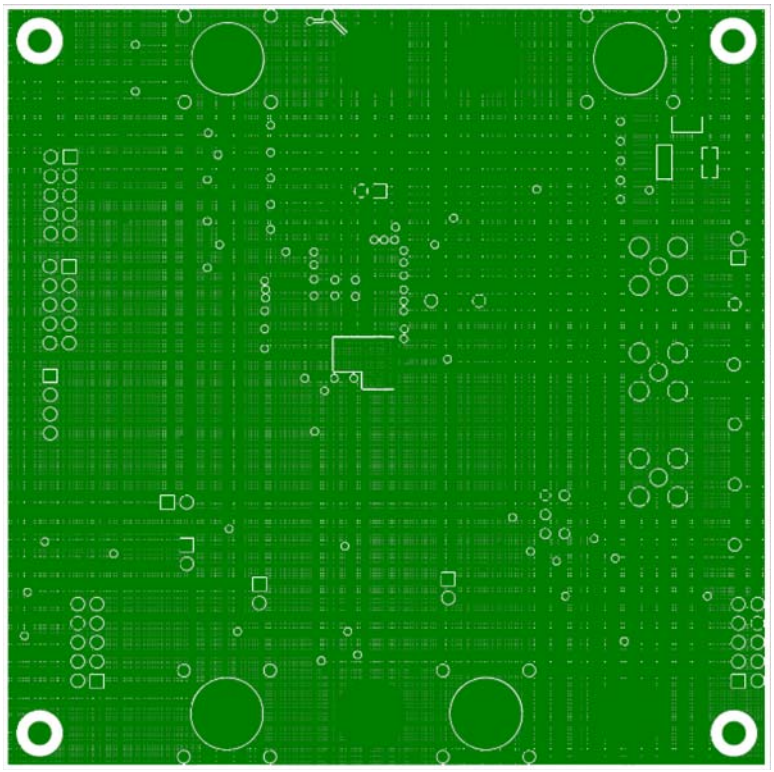

FIGURE 5. INNER_1

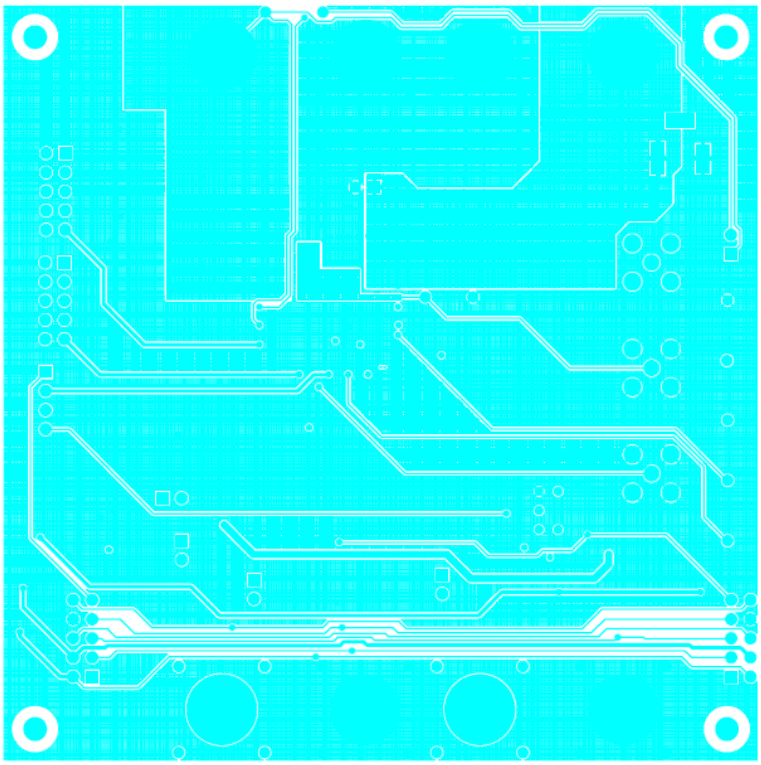

FIGURE 6. INNER_2

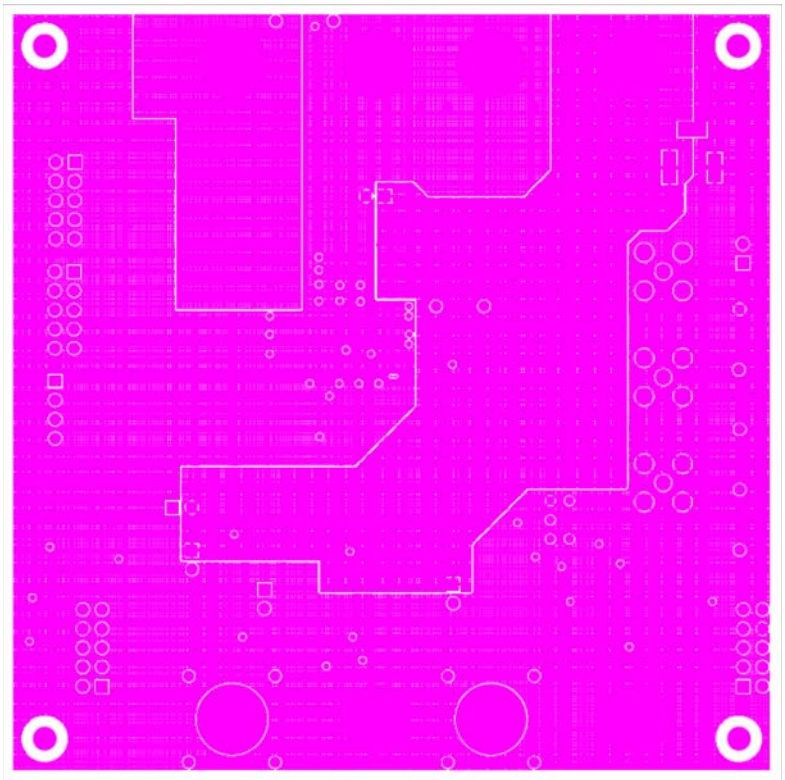

FIGURE 7. INNER_3

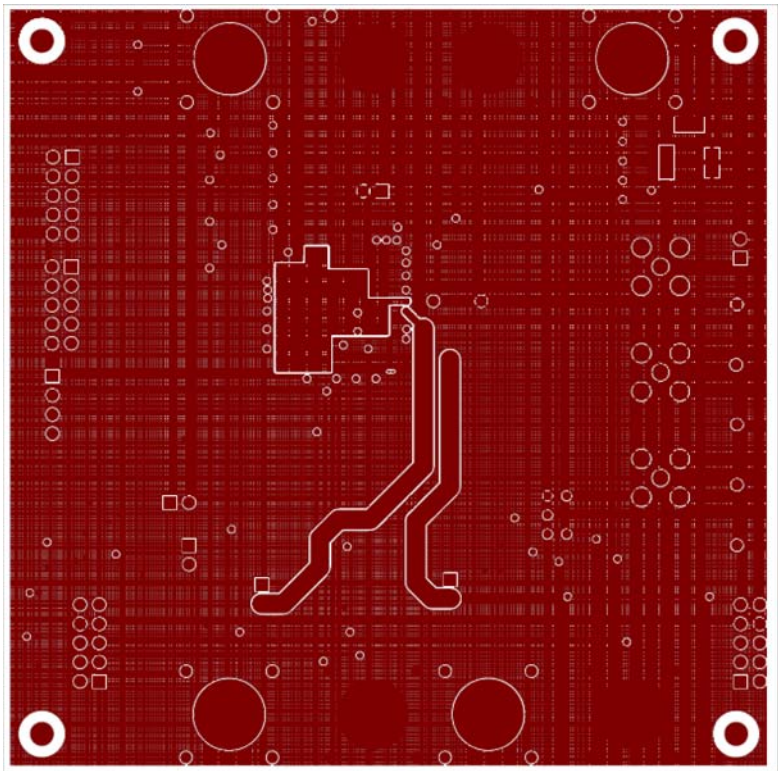

FIGURE 8. INNER_4

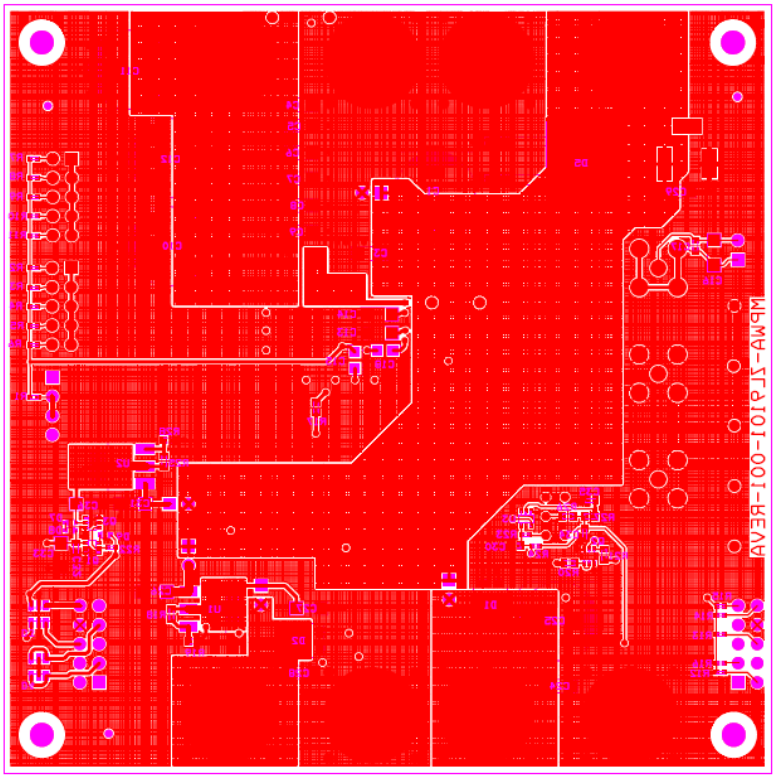

FIGURE 9. BOTTOM

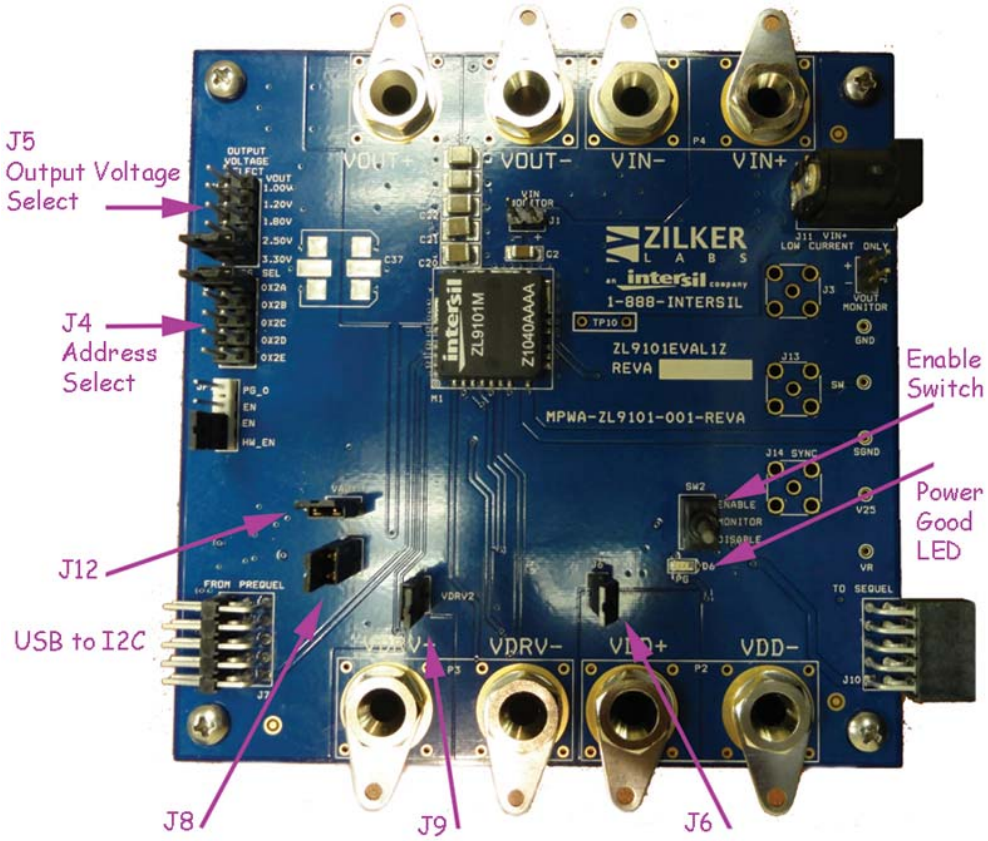

FIGURE 10. PHOTO SHOWING JUMPERS AND CONNECTORS