LM5008A Evaluation Board

National Semiconductor
Application Note 1925
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Introduction

The LM5008AEVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 5V output over an input range of 8V to 75V. The circuit delivers load currents to 300 mA, with current limit set at a nominal 440 mA.

The board's specification are:

- Input Voltage: 8V to 75V
- Output Voltage: 5V
- Maximum load current: 300 mA
- Minimum load current: 0A
- Current Limit: 440 mA (nominal)
- Measured Efficiency: 92.4% (V_{IN} = 8V, I_{OUT} = 100 mA)
- Nominal Switching Frequency: 130 kHz
- Size: 2.6 in. x 1.6 in.

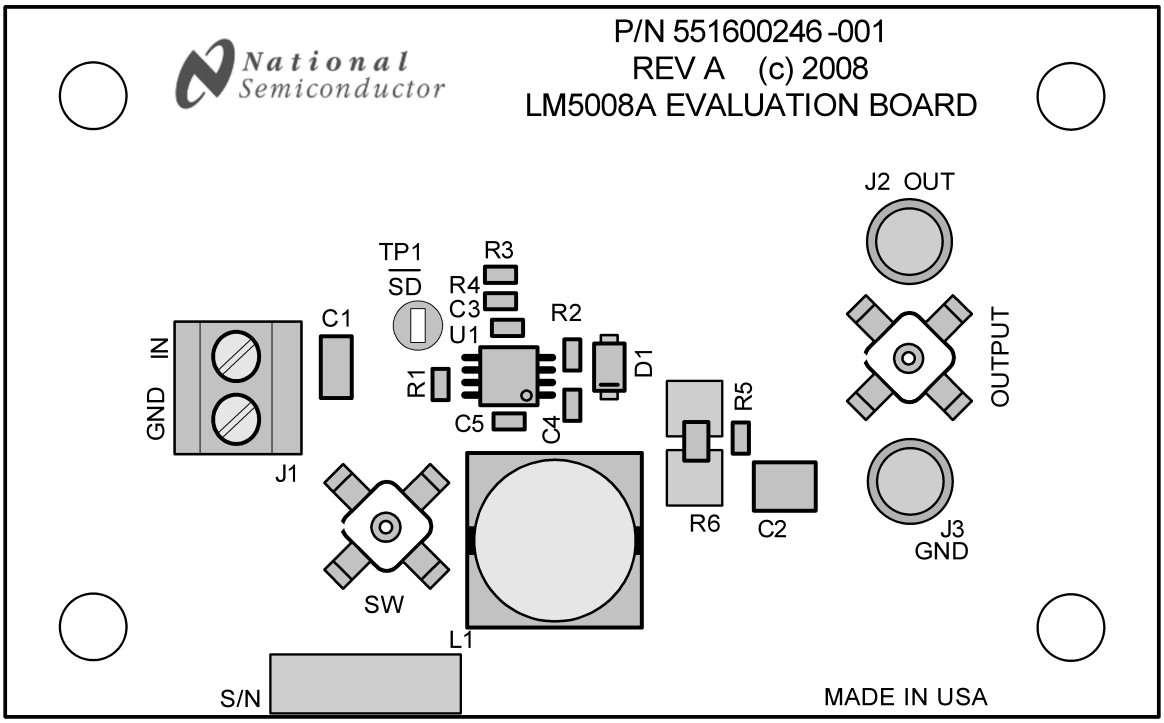


FIGURE 1. Evaluation Board - Top Side

Theory of Operation

Refer to the evaluation board schematic in *Figure 5*. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and VIN according to the equation:

$$t_{ON} = \frac{1.385 \times 10^{-10} \times R1}{V_{IN}}$$

The on-time of this evaluation board ranges from ≅4.85 µs at VIN = 8V, to ≅517 ns at VIN = 75V. The on-time varies inversely with VIN to maintain a nearly constant switching frequency. At the end of each on-time the Minimum Off-Timer ensures the buck switch is off for at least 300 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C2). When the output voltage falls sufficiently that the voltage at FB is below 2.5V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. The current limit threshold is ≅470 mA at Vin = 8V, and ≅415 mA at Vin = 75V. Refer to the LM5008A data sheet for a more detailed block diagram, and a complete description of the various functional blocks.

Board Layout and Probing

The pictorial in *Figure 1* shows the placement of the circuit components. The following should be kept in mind when the board is powered:

1) When operating at high input voltage and high load current, forced air flow may be necessary.

2) The LM5008A, and diode D1 may be hot to the touch when operating at high input voltage and high load current.

3) Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.

4) At maximum load current, the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

Board Connection/Start-up

The input connections are made to the J1 connector. The load is connected to the J2 (OUT) and J3 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 8V, at which time the output voltage should be 5V. If the output voltage is correct with 8V at VIN, then increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 75V AT VIN.

Output Ripple Control

The LM5008A requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple at V_{OUT}, through the feedback resistors as described in Option A below. Options B and C provide lower output ripple with one or two additional components.

Option A) Lowest Cost Configuration: In this configuration R5 is installed in series with the output capacitance (C2). Since ≥25 mVp-p are required at the FB pin, R5 must be chosen to generate ≥50 mVp-p at V_{OUT}, knowing that the minimum ripple current in this circuit is ≅66 mAp-p at minimum V_{IN}. Using 0.82Ω for R5, the ripple at V_{OUT} ranges from ≅54 mVp-p to ≅135 mVp-p over the input voltage range. If the application can accept this ripple level, this is the most economical solution. The circuit is shown in *Figure 2*. See *Figure 8*.

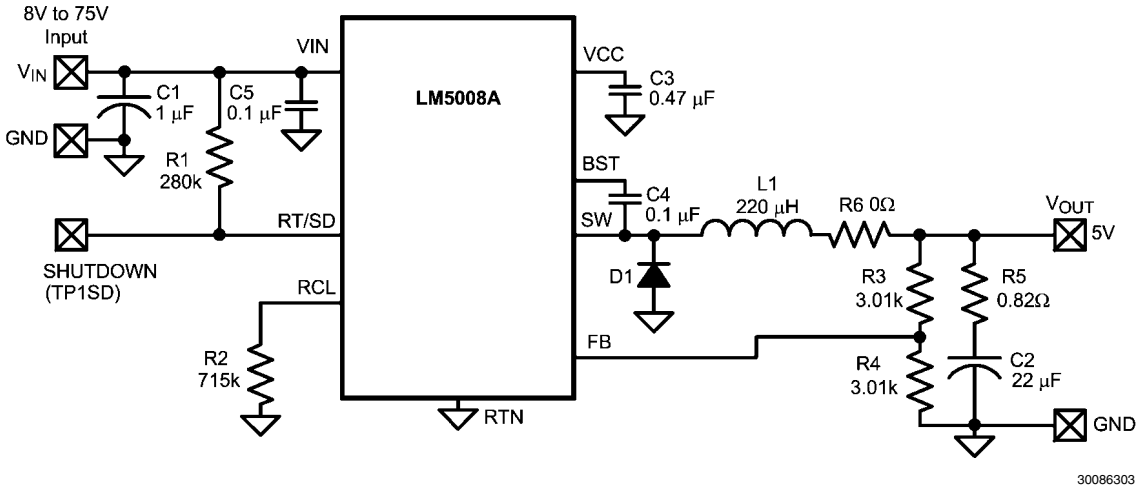


FIGURE 2. Lowest Cost Configuration

Option B) Intermediate Ripple Configuration: This configuration generates less ripple at V_{OUT} than option A above by the addition of one capacitor (Cff) across R3, as shown in *Figure 3*.

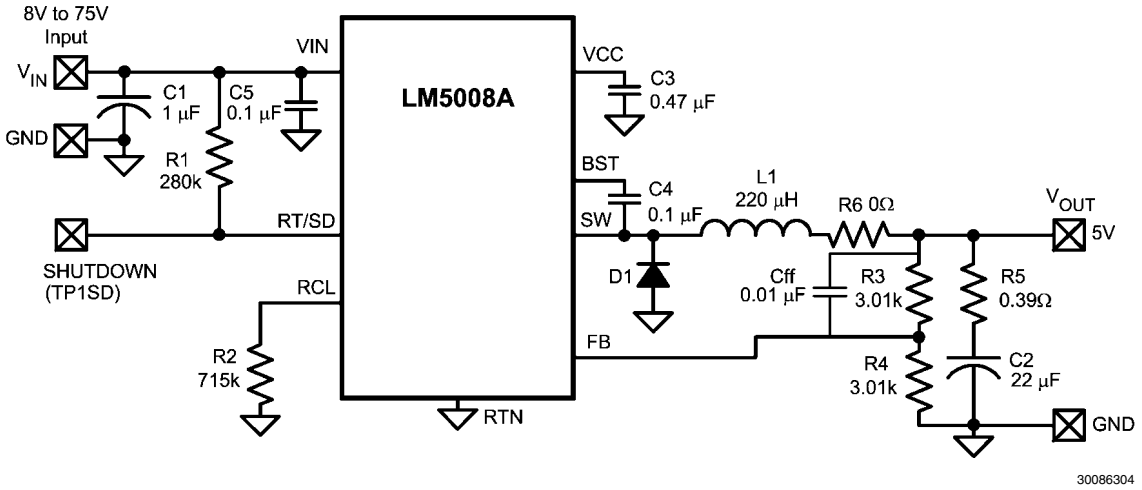


FIGURE 3. Intermediate Ripple Configuration

Since the output ripple is passed by Cff to the FB pin with little or no attenuation, R5 can be reduced so the minimum ripple at V_{OUT} is ≅25 mVp-p. The minimum value for Cff is calculated from:

$$Cff \geq \frac{3 \times t_{ON\,(max)}}{(R3//R4)}$$

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and R3//R4 is the parallel equivalent of the feedback resistors. The ripple at V_{OUT} ranges from 26 mVp-p to 64 mVp-p over the input voltage range. See *Figure 8*.

Option C) Minimum Ripple Configuration: To obtain minimum ripple at V_{OUT}, R5 is set to 0Ω, and RA, CA, and CB are added to generate the required ripple for the FB pin. In this configuration, the output ripple is determined primarily by the characteristics of the output capacitance and the inductor's ripple current. See *Figure 4*.

The ripple voltage required by the FB pin is generated by RA, and CA since the SW pin switches from -1V to V_{IN}, and the right end of CA is a virtual ground. The values for RA and CA are chosen to generate a 50-100 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through CB. The following procedure is used to calculate values for RA, CA and CB:

1) Calculate the voltage V_A:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN})))$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 0.6V), and V_{IN} is the minimum input voltage. For this circuit, V_A calculates to 4.78V. This is the approximate DC voltage at the RA/CA junction, and is used in the next equation.

2) Calculate the RA x CA product:

$$RA \times CA = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V}$$

where t_{ON} is the maximum on-time (≅4.85 µs), V_{IN} is the minimum input voltage, and ΔV is the desired ripple amplitude at the RA/CA junction, 50 mVp-p for this example.

$$RA \times CA = \frac{(8V - 4.78V) \times 4.85\ \mu s}{0.05V} = 3.12 \times 10^{-4}$$

RA and CA are then chosen from standard value components to satisfy the above product. Typically CA is 3000 to 10000 pF, and RA is 10 kΩ to 300 kΩ. CB is chosen large compared to CA, typically 0.1 µF. The ripple at V_{OUT} is typically less than 10 mVp-p. See *Figure 4* and *Figure 8*.

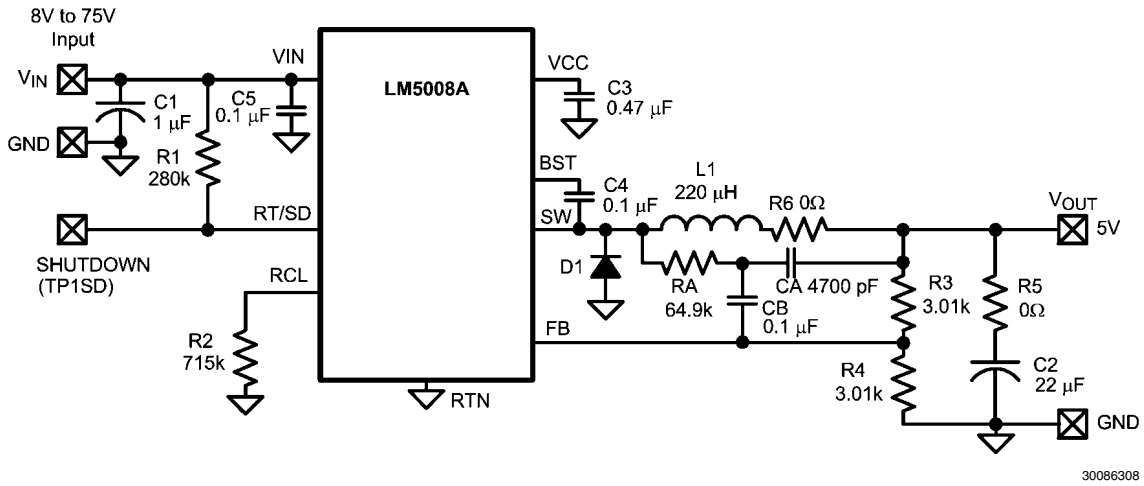


FIGURE 4. Minimum Output Ripple Configuration

Current Limit Off-Time

When current limit is detected the on-time period is immediately terminated, and the off-time forced by the LM5008A must be greater than the maximum normal off-time, which occurs at maximum input voltage. The longer-than-normal off-time is necessary to allow the inductor current to decrease at least as much, if not more, than the current increase which occurred during the on-time leading to the current limit detection. The forced off-time is determined by the resistor at the RCL pin (R2), and is calculated from the following:

$$T_{OFF} = 10^{-5}/(0.285 + (V_{FB}/6.35 \times 10^{-6} \times R2))$$

where V_{FB} is the voltage at the FB pin at the time of the current limit detection. In this evaluation board, the maximum normal off-time is approximately 7.2 µs (at 75V). Due to the 25% tolerance of the on-time, the off-time tolerance is also 25%, yielding a maximum possible off-time of 9 µs. Allowing for the response time of the current limit detection circuit (350 ns) the maximum off-time, for the purpose of this calculation, is increased to 9.35 µs. This is increased an additional 25% to 11.7 µs to allow for the tolerances of the above equation. Using the above equation, R2 calculates to 691 kΩ at V_{FB} = 2.5V. A standard value 715 kΩ resistor is used.

Monitor The Inductor Current

The inductor's current can be monitored or viewed on a scope with a current probe. Remove R6, and install an appropriate current loop across the two large pads where R6 was located. In this way the inductor's ripple current and peak current can be accurately determined.

Scope Probe Adapters

Scope probe adapters are provided on this evaluation board for monitoring the waveform at the SW pin, and at the circuit's output (V_{OUT}), without using the probe's ground lead which can pick up noise from the switching waveforms. The probe adapters are suitable for Tektronix P6137 or similar probes, with a 0.135" diameter.

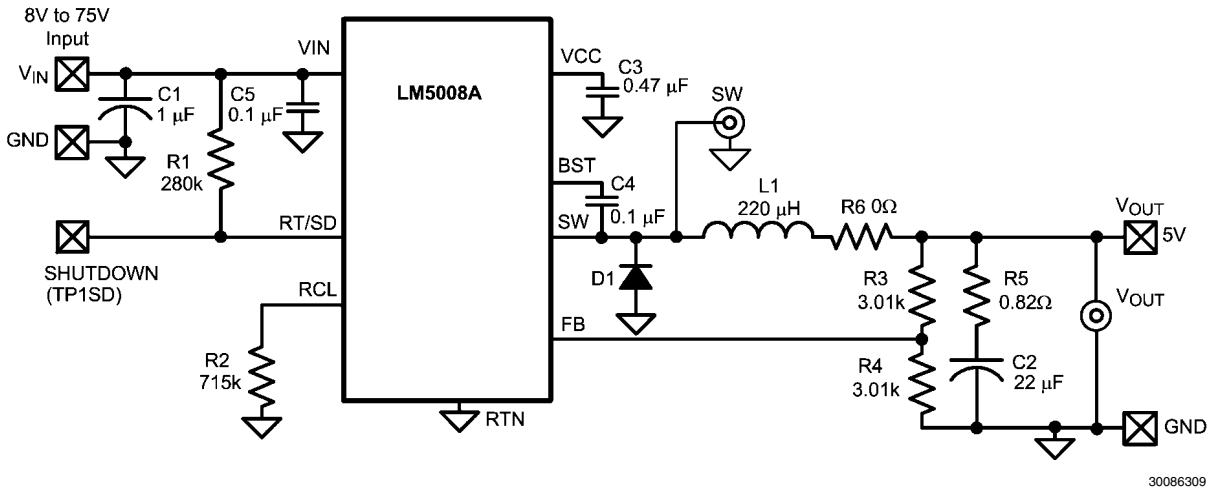


FIGURE 5. Complete Evaluation Board Schematic (As Supplied)

Bill of Materials

Item	Description	Mfg., Part Number	Package	Value
C1	Ceramic Capacitor	TDK C3216X7R2A105M or Murata GRM31CR72A105KA01L	1206	1 µF, 100V
C2	Ceramic Capacitor	TDK C3225X7R1C226M or Murata GRM32ER71C226KE18L	1210	22 µF, 16V
C3	Ceramic Capacitor	TDK C1608X7R1C474M or TDK C1608X7R1C474K	0603	0.47 µF, 16V
C4	Ceramic Capacitor	TDK C1608X7R1H103M	0603	0.01 µF, 50V
C5	Ceramic Capacitor	TDK C2012X7R2A104M or Murata GRM188R72A104KA35D	0805	0.1 µF, 100V
D1	Schottky Diode	Diodes Inc. DFLS1100 or Central Semi CMMSH1-100	Power DI123	100V, 1A
L1	Power Inductor	Coiltronics DR1050-221-R or TDK SLF10145T-221MR65	10mm x 10mm	220 µH
R1	Resistor	Vishay CRCW06032803F	0603	280k
R2	Resistor	Vishay CRCW06037153F	0603	715k
R3, R4	Resistor	Vishay CRCW06033011F	0603	3.01k
R5	Resistor	Panasonic ERJ-3RQFR82V	0603	0.82 ohms
R6	Resistor	Vishay CRCW08050000Z	0805	0Ω Jumper
U1	Switching Regulator	National Semiconductor LM5008AMM	MSOP-8	

Circuit Performance

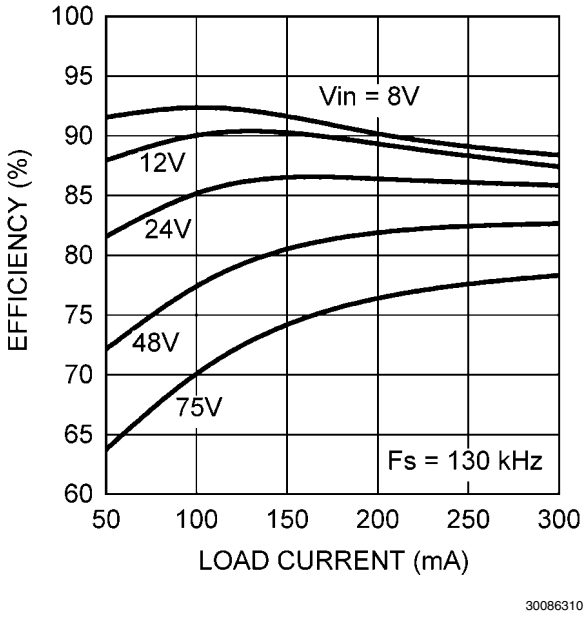


FIGURE 6. Efficiency vs Load Current

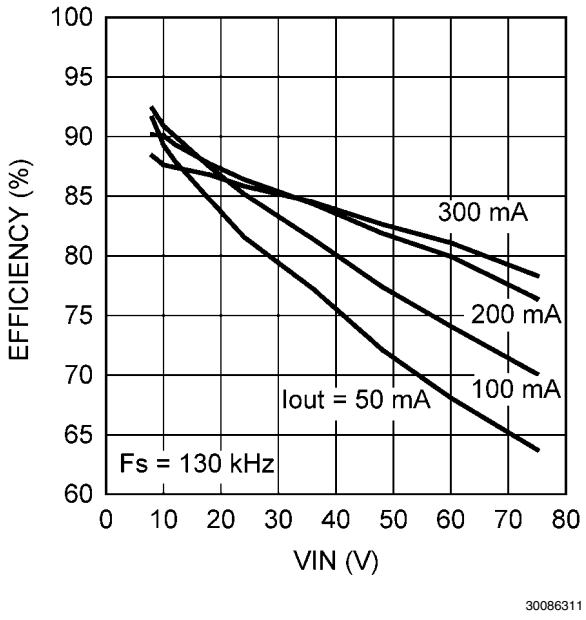


FIGURE 7. Efficiency vs Input Voltage

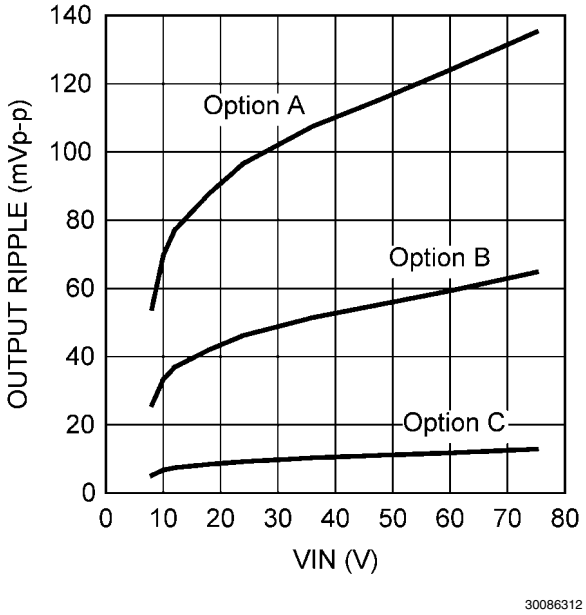


FIGURE 8. Output Voltage Ripple

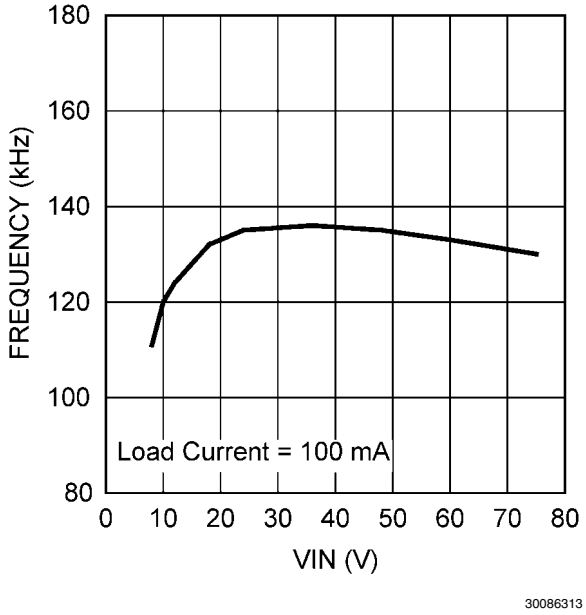


FIGURE 9. Switching Frequency vs. Input Voltage

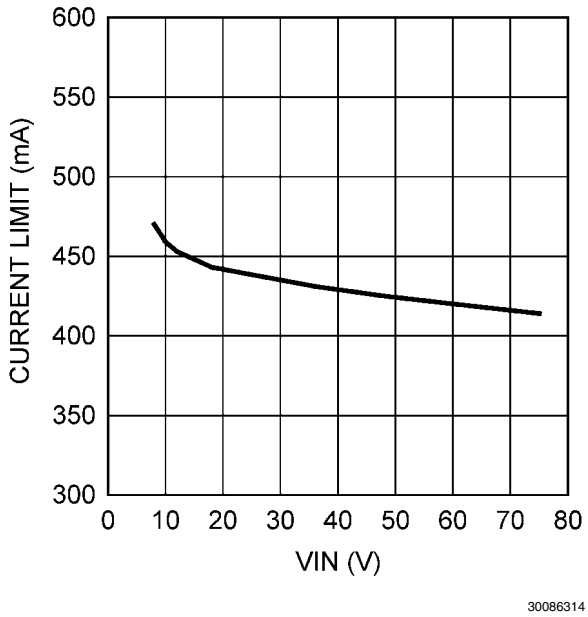


FIGURE 10. Current Limit vs Input Voltage

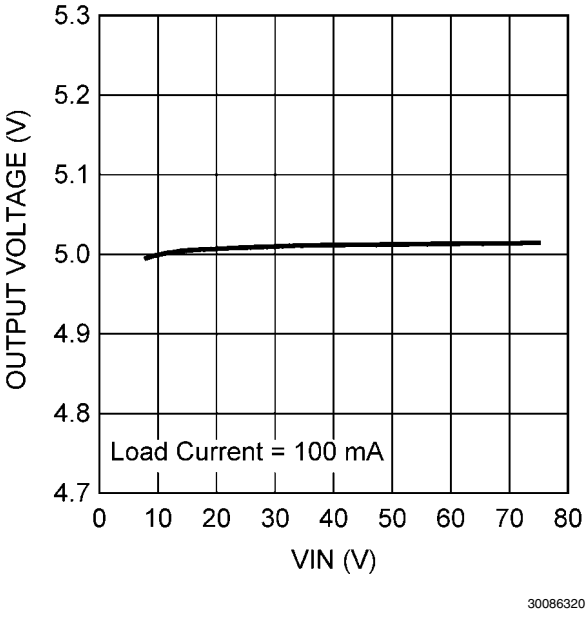


FIGURE 11. Line Regulation

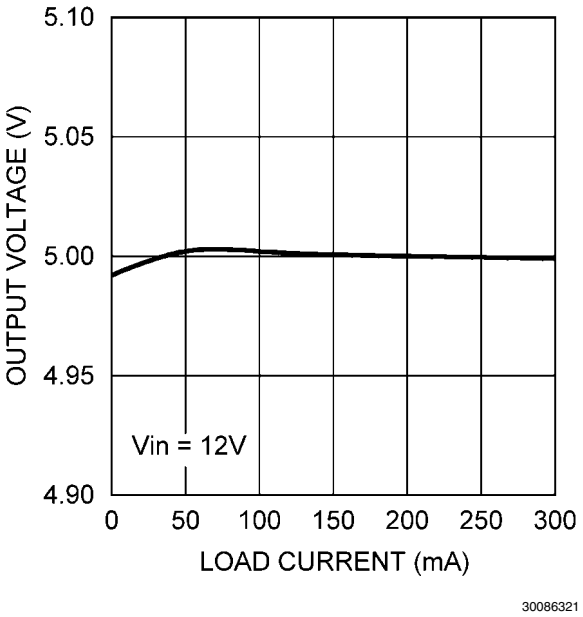
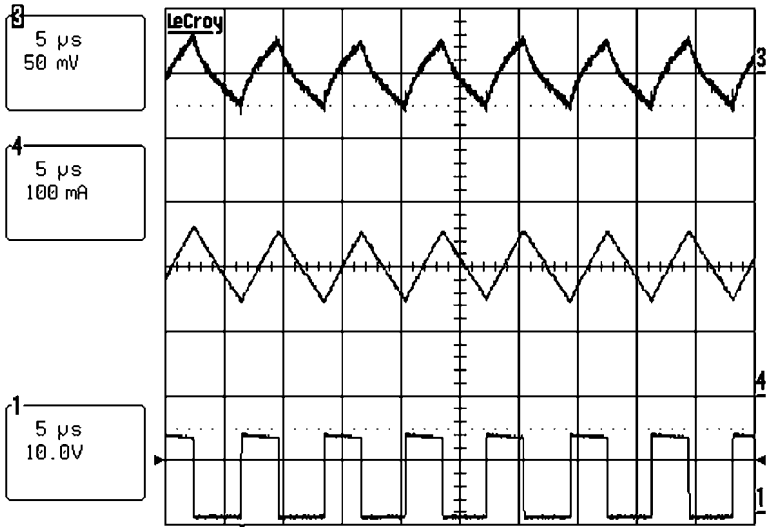


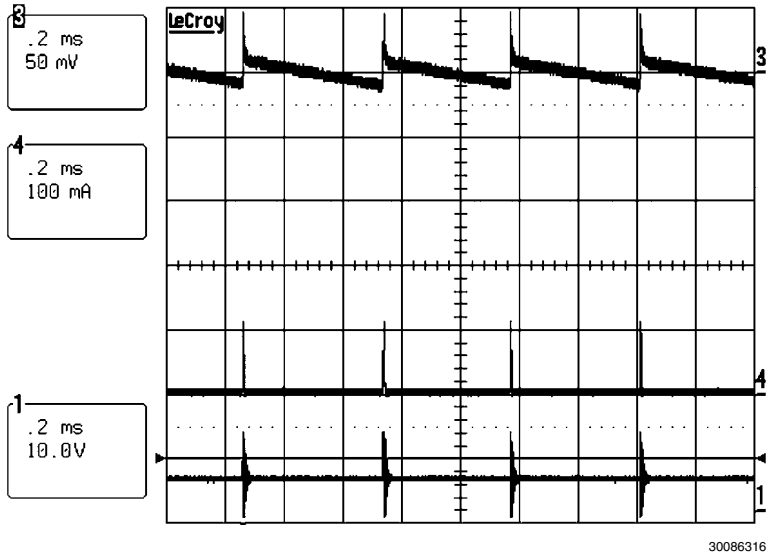
FIGURE 12. Load Regulation

Typical Waveforms



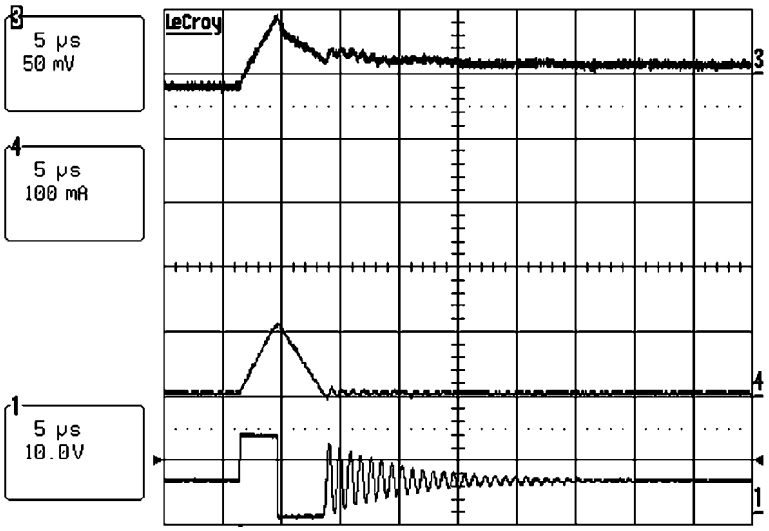
Trace 1 = SW Pin
Trace 3 = V_{OUT}
Trace 4 = Inductor Current
Vin = 12V, Iout = 200 mA

FIGURE 13. Continuous Conduction Mode



Trace 1 = SW Pin
Trace 3 = V_{OUT}
Trace 4 = Inductor Current
Vin = 12V, Iout = 0 mA

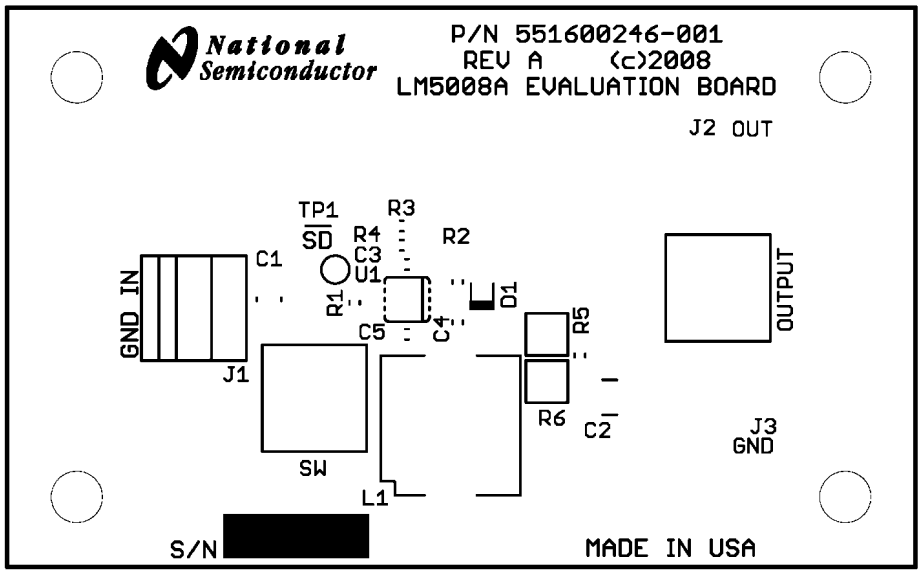
FIGURE 14. Discontinuous Conduction Mode



Trace 1 = SW Pin
Trace 3 = V_{OUT}
Trace 4 = Inductor Current
Vin = 12V, Iout = 0 mA

FIGURE 15. Discontinuous Conduction Mode

PC Board Layout



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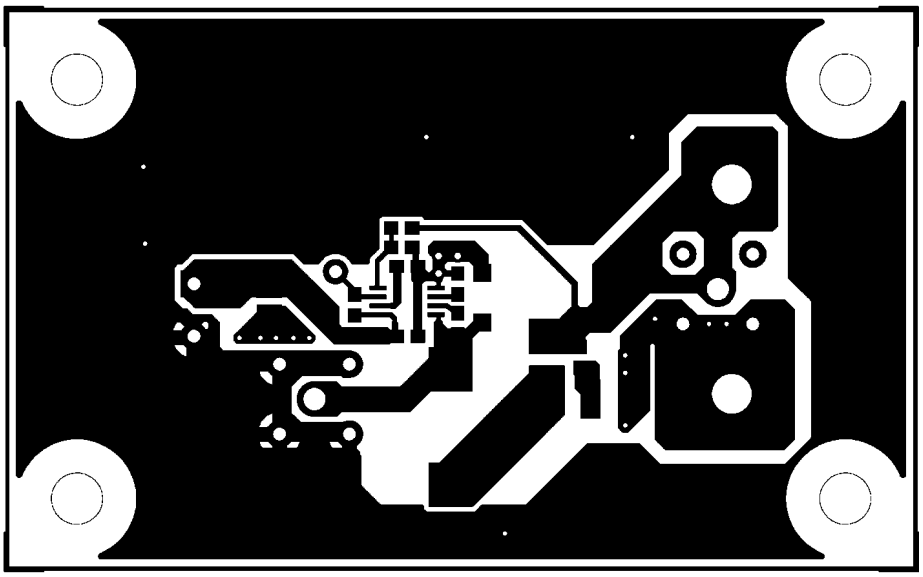
Board Silkscreen



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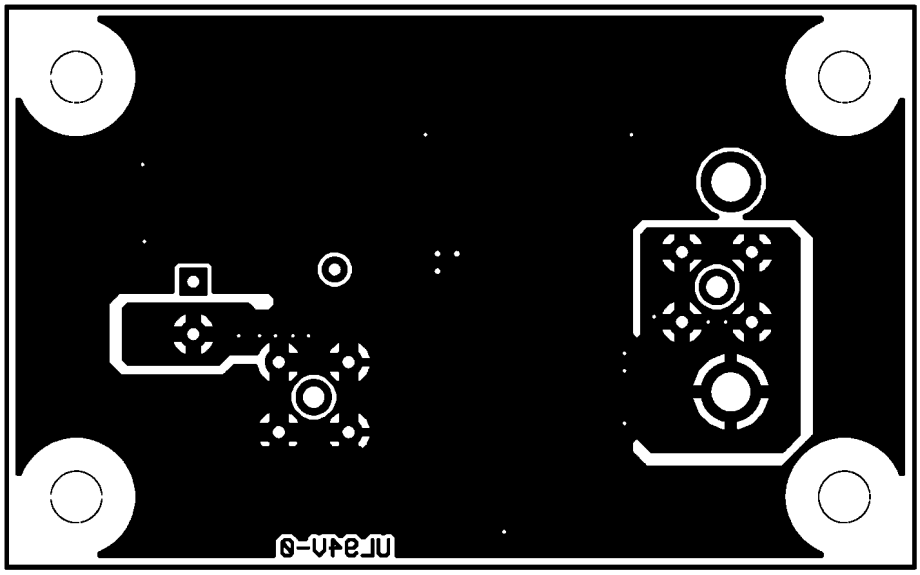
Board Top Layer



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Board Bottom Layer (Viewed from Top)

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