# AS1372

## 350mA Dual Rail Linear Regulator

## 1 General Description

The AS1372 is a Dual Supply Rail Linear Regulator designed for providing ultra-low voltages.

In a typical application the battery is directly connected to VBIAS and VIN is connected to the output of a DC-DC Converter.

The very low quiescent currents together with the excellent transient features and the superior dropout are making the AS1372 an ideal device for applications running on batteries.

The robust design ensures that no under-voltage failure can occur and the device is also equipped with an internal protection against over-temperature and over-current.

The device is available in fixed output voltages from 0.5V up to 2.2V in 100mV steps (50mV from 0.5V to 1.1V).

The AS1372 is available in a 5-bumps CS-WLP package and is qualified for -40°C to +85°C operation.

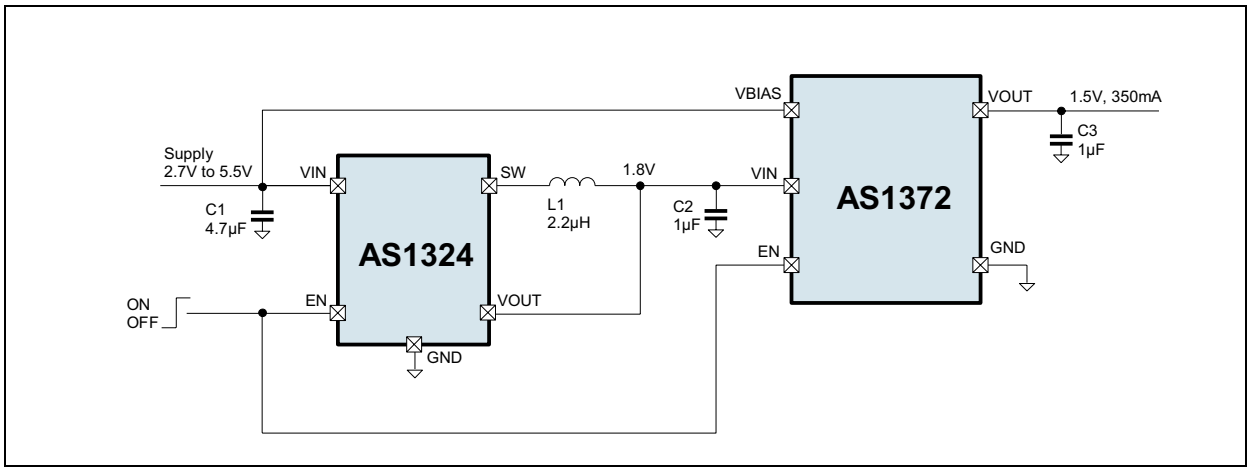
## 2 Key Features

- Input Voltage: 0.7V to 4.5V
- Bias Supply Voltage: 2.5V to 5.5V
- Output Voltage: 0.5V to 2.2V in 100mV steps
- Output Voltage Accuracy: ±1.5%
- Dropout Voltage 135mV @ 350mA load
- Max. Output Current: 350mA
- Load Transient Response: ±15mV (typ.)
- Superior Efficiency
- Low Shutdown Current: 10nA
- High PSRR: >80dB @ 10Hz-1kHz, 60db @100kHz
- Noise Voltage: 50µ$V_{RMS}$ from 10Hz to 1000kHz
- Integrated Overtemperature/Overcurrent Protection
- Chip Enable Input
- Operating Temperature Range: -40°C to +85°C
- 5-bumps CS-WLP Package

## 3 Applications

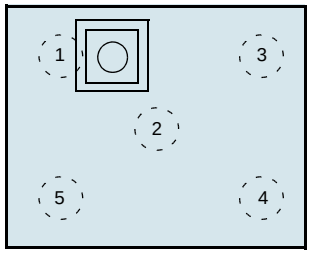
The devices are ideal for powering cordless and mobile phones, MP3 players, PDAs, hand-held computers, digital cameras, and any other hand-held and/or battery-powered device.

*Figure 1. AS1372 - Typical Application Diagram*



# 4 Pin Assignments

*Figure 2. Pin Assignments (Top View)*




## Pin Descriptions

*Table 1. Pin Descriptions*

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | VOUT | **Regulated Output Voltage**. Bypass this pin with a capacitor to GND. |
| 2 | GND | **Ground.** |
| 3 | EN | **Enable.** Pull this pin to low to disable the device. This pin has an internal 1.6MΩ (typ.) pull-down resistor. |
| 4 | VBIAS | **Bias Supply Voltage.** 2.5V to 5.5V, Bypass this pin with a capacitor to GND. |
| 5 | VIN | **Unregulated Input Voltage**. 0.7V to 4.5V, $V_{IN} \leq V_{BIAS}$, Bypass this pin with a capacitor to GND. |

# 5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*Table 2. Absolute Maximum Ratings*

| Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|
| VIN, VBIAS and EN to GND | -0.3 | +6.5 | V | VIN < VBIAS or equal in operating conditions |
| VOUT to GND | -0.3 | $V_{IN}$ + 0.3 | V | |
| Output Short-Circuit Duration | | Indefinite | | |
| ESD | 2 | | kV | *HBM MIL-Std. 883E 3015.7* methods |
| Latch-Up | -100 | +100 | mA | *JEDEC 78* |
| Operating Temperature Range | -40 | +85 | ºC | |
| Storage Temperature Range | -65 | +150 | ºC | |
| Junction Temperature | | +125 | ºC | |
| Package Body Temperature | +260 | | ºC | The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn). |

# 6 Electrical Characteristics

$V_{IN}$ = $V_{OUT}$ + 0.2V, $V_{BIAS}$ = $V_{OUT}$ + 1.5V (or 2.5V whichever is larger), EN = $V_{BIAS}$, $C_{IN}$ = $C_{OUT}$ = $C_{BIAS}$ = 1µF, $T_{AMB}$ = -40°C to +85ºC, Typical Values are at $T_{AMB}$ = +25ºC (unless otherwise specified).

*Table 3. Electrical Characteristics*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | $V_{IN} \leq V_{BIAS}$ | 0.7 | | 4.5 | V |
| $V_{BIAS}$ | Bias Supply Voltage | | 2.5 | | 5.5 | V |
| $V_{OUT}$ | Output Voltage | Available in 50mV or 100mV steps (see Ordering Information on page 13) | 0.5 | | 2.2 | V |
| $V_{OUT(NOM)}$ - $V_{OUT}$ | Output Voltage Accuracy $V_{OUT}$ > 1.2V | $I_{OUT}$ = 100µA | -1.5 | | +1.5 | % |
| | | $I_{OUT}$ = 100µA to 350mA, $V_{IN}$ = $V_{OUT(NOM)}$+0.2V to 4.5V, $V_{BIAS}$ = $V_{OUT(NOM)}$+1.5V to 5.5V | -2 | | +2 | |
| | Output Voltage Accuracy $V_{OUT} \leq$ 1.2V | $I_{OUT}$ = 100µA | -2 | | +2 | % |
| | | $I_{OUT}$ = 100µA to 350mA, $V_{IN}$ = $V_{OUT(NOM)}$+0.2V to 4.5V, $V_{BIAS}$ = $V_{OUT(NOM)}$+1.5V to 5.5V | -2.5 | | +2.5 | |
| $\Delta V_{OUT}$ / $\Delta V_{IN}$ | Line Regulation $V_{IN}$ | $V_{IN}$ = $V_{OUT(NOM)}$+0.2V to 4.5V, $V_{BIAS}$ = 5.5V, $I_{OUT}$ = 100µA | | 40 | | µV/V |
| $\Delta V_{OUT}$ / $\Delta V_{BIAS}$ | Line Regulation $V_{BIAS}$ | $V_{BIAS}$ = $V_{OUT(NOM)}$+1.5V to 5.5V, $I_{OUT}$ = 100µA | | 100 | | µV/V |
| $\Delta V_{LDR}$ | Load Regulation | $I_{OUT}$ = 1mA to 350mA | | 6 | | µV/mA |
| $I_{OUT}$ | Output Current[1] | | 350 | | | mA |
| $I_{LIM}$ | Current Limit | | | 500 | | mA |
| $V_{DROP}$ - $V_{IN}$ | Output Voltage Dropout $V_{IN}$ | $V_{BIAS}$ = $V_{OUT}$ + 1.5V, $I_{OUT}$ = 350mA | | 135 | | mV |
| | | $V_{BIAS}$ = $V_{OUT}$ + 1.8V, $I_{OUT}$ = 350mA | | 115 | | |
| | | $V_{BIAS}$ = 5.5V, $I_{OUT}$ = 350mA | | 110 | | |
| $V_{DROP}$ - $V_{BIAS}$ | Output Voltage Dropout $V_{BIAS}$ | $I_{OUT}$ = 100mA | | 1.1 | 1.5 | V |
| $E_N$ | Output Voltage Noise | $V_{OUT} \leq$ 1.2V, f = 10Hz to 100kHz | | 50 | | $\mu V_{RMS}$ |
| PSRR - $V_{IN}$ | Power-Supply Rejection Ratio Sine modulated $V_{IN}$ | f = 100Hz | | 85 | | dB |
| | | f = 1kHz | | 80 | | |
| | | f = 10kHz | | 70 | | |
| | | f = 100kHz | | 60 | | |
| PSRR - $V_{BIAS}$ | Power-Supply Rejection Ratio Sine modulated $V_{BIAS}$ | f = 100Hz | | 75 | | dB |
| | | f = 1kHz | | 60 | | |
| | | f = 10kHz | | 50 | | |
| | | f = 100kHz | | 50 | | |
| $I_{Q\_VBIAS}$ | Quiescent Current into $V_{BIAS}$ | | | 40 | 75 | µA |
| $I_{Q\_VIN}$ | Quiescent Current into $V_{IN}$ | $I_{OUT}$ = 0mA | | 6.5 | 10 | |

*Table 3. Electrical Characteristics*

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{SHDN}$ - $V_{BIAS}$ | Shutdown Current into $V_{BIAS}$ | $V_{EN}$ = 0V | | 10 | | nA |
| $I_{SHDN}$ - $V_{IN}$ | Shutdown Current into $V_{IN}$ | | | 10 | | |
| **Logic Levels** | | | | | | |
| $V_{IH}$ | Enable Input Threshold | | 1 | | | V |
| $V_{IL}$ | | | | | 0.4 | |
| $I_{EN}$ | Enable Input Bias Current | EN = GND | | 0.01 | | nA |
| **Thermal Protection** | | | | | | |
| $T_{SHDN}$ | Thermal Shutdown Temperature | | | 150 | | ºC |
| $\Delta T_{SHDN}$ | Thermal Shutdown Hysteresis | | | 25 | | ºC |
| **Transient Characteristics** | | | | | | |
| $\Delta V_{OUT}$ | Dynamic Load Transient Response | Pulsed $I_{LOAD}$ from 0mA to 300mA in 10µs rise time | | 15 | | mV |
| $t_{ON}$ | Exit Delay from Shutdown | $V_{OUT} \leq$ 1.2V, setting to 95% | | 70 | | µs |
| $C_{OUT}$ | Output Capacitor | Load Capacitor Range | 1 | | 10 | µF |
| | | Maximum ESR Load | 1 | | 500 | mΩ |

1. guaranteed by design

**Note:** All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

# 7 Typical Operating Characteristics

VIN = 1.2V, VBIAS = 2.5V, VOUT = 1.0V, EN = VBIAS, CIN = COUT = CBIAS = 1µF, TAMB = -40°C to +85ºC, Typical Values are at TAMB = +25ºC (unless otherwise specified).

*Figure 3. Bias Supply Current vs. Bias Supply Voltage*

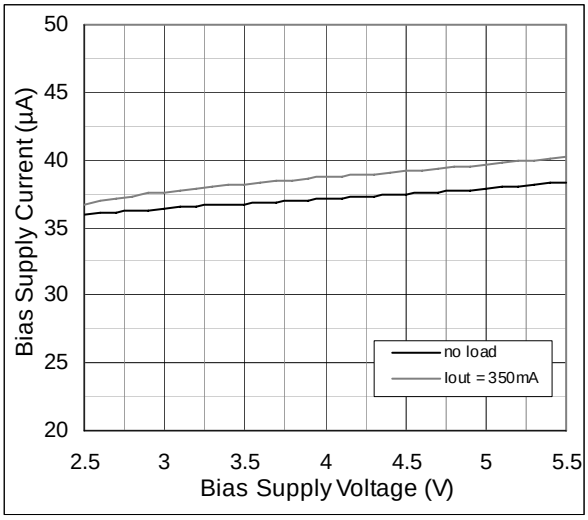



*Figure 4. Bias Supply Current vs. Bias Supply Voltage*

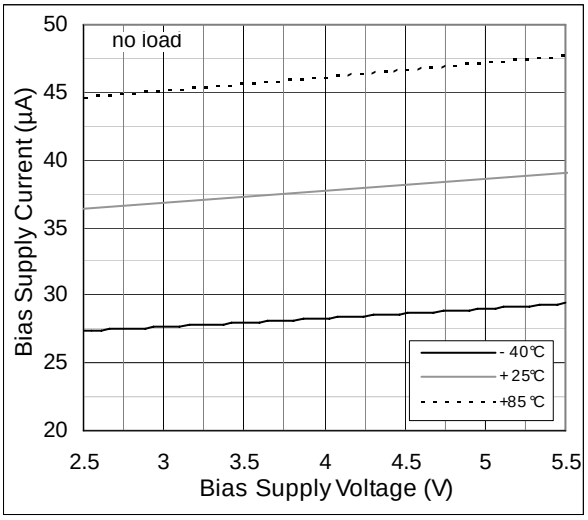



*Figure 5. Ground Current vs. VIN; VBIAS = 5.5V*

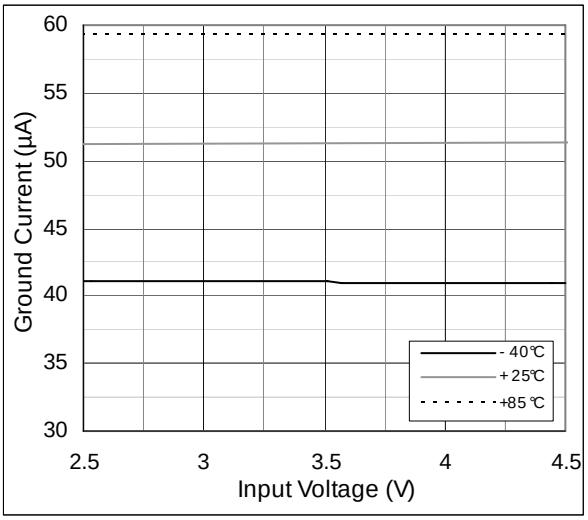



*Figure 6. Ground Current vs. VIN / VBIAS;*

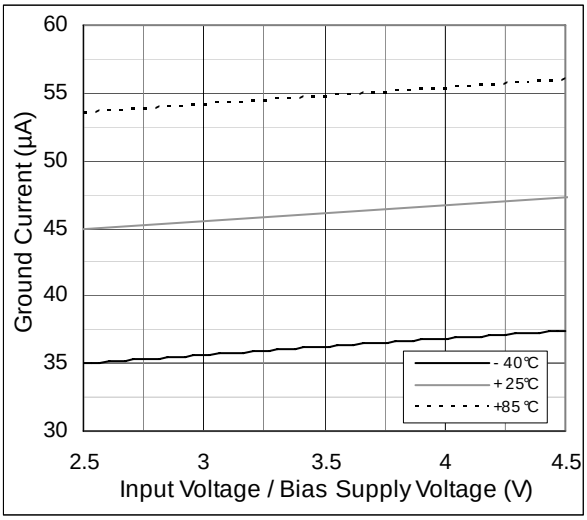



*Figure 7. Ground Current vs. Bias Supply Voltage*

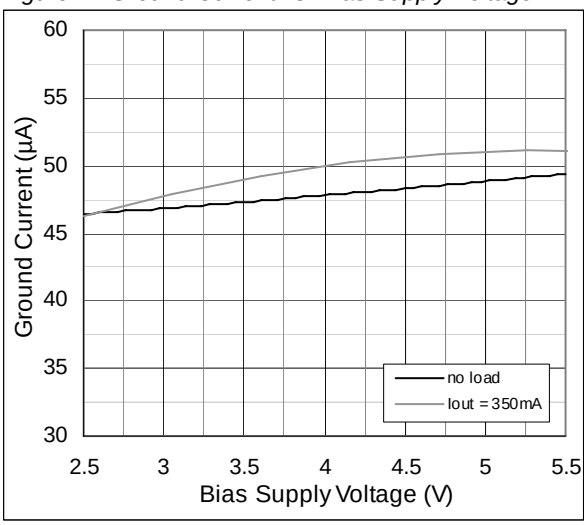



*Figure 8. Ground Current vs. Load Current*

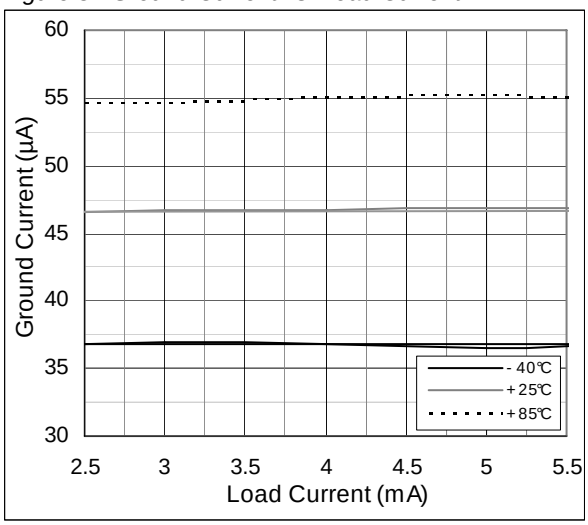


*Figure 9. PSRR $V_{IN}$; $V_{IN}$ = 3$V_{DC}$ + 250m$V_{pk}$*

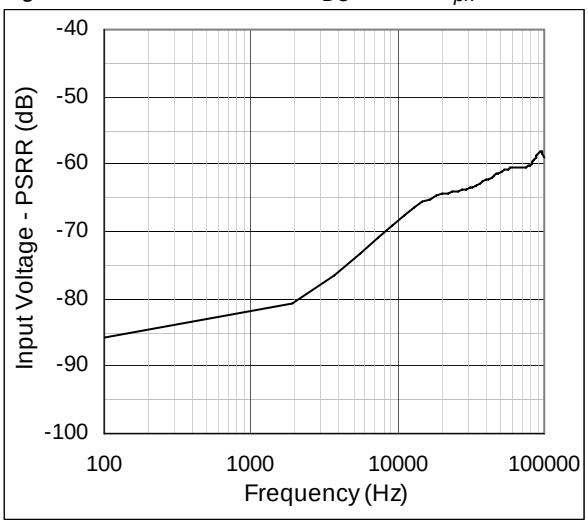



*Figure 10. PSRR $V_{BIAS}$; $V_{BIAS}$ = 3.5$V_{DC}$ + 500m$V_{pk}$*

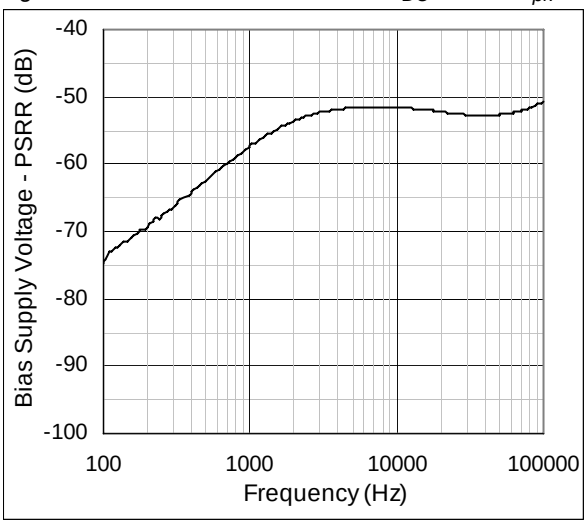



*Figure 11. Line Regulation: $V_{OUT}$ vs. $V_{IN}$; $V_{BIAS}$ = 5.5V*

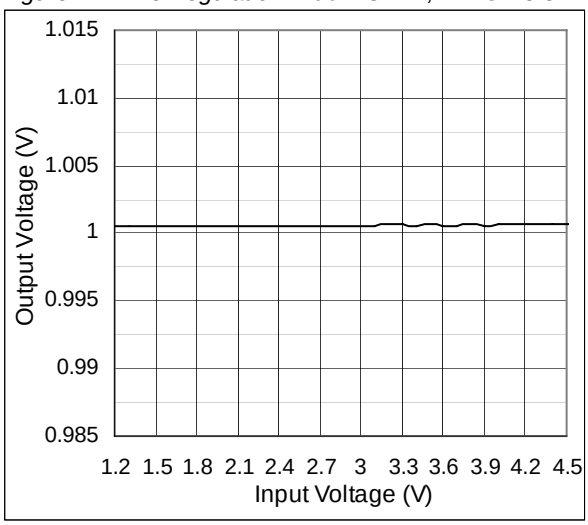



*Figure 12. Line Regulation: $V_{OUT}$ vs. $V_{BIAS}$*

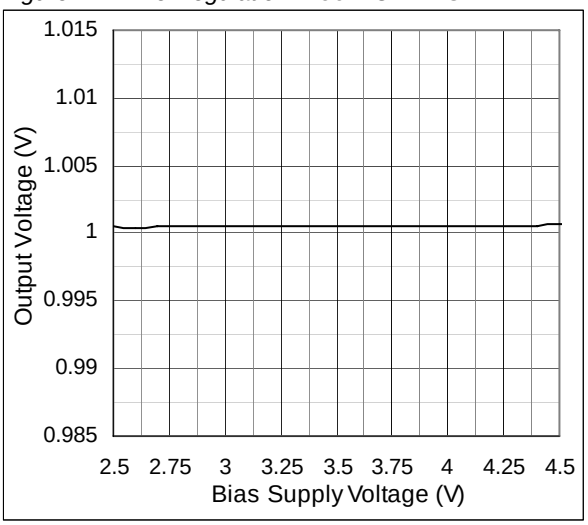



*Figure 13. Load Regulation: $V_{OUT}$ vs. $I_{OUT}$*

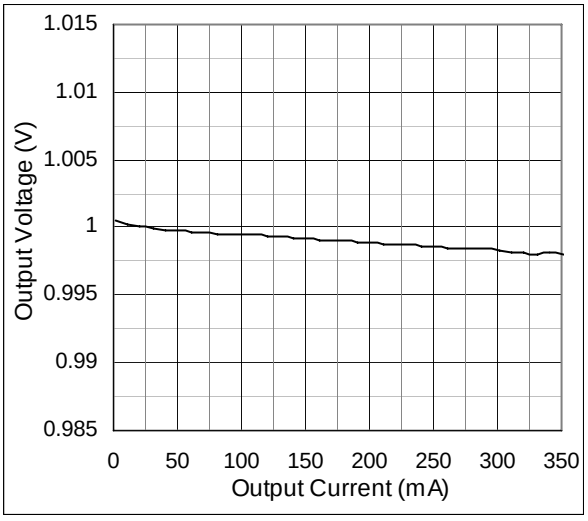



*Figure 14. Output Voltage vs. Temperature; $I_{OUT}$ = 1mA*

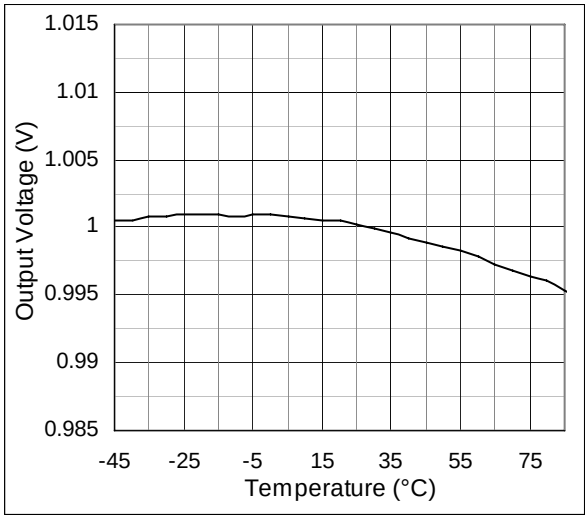


*Figure 15. Dropout $V_{IN}$ vs. Temp.; $I_{OUT}$ = 350mA*

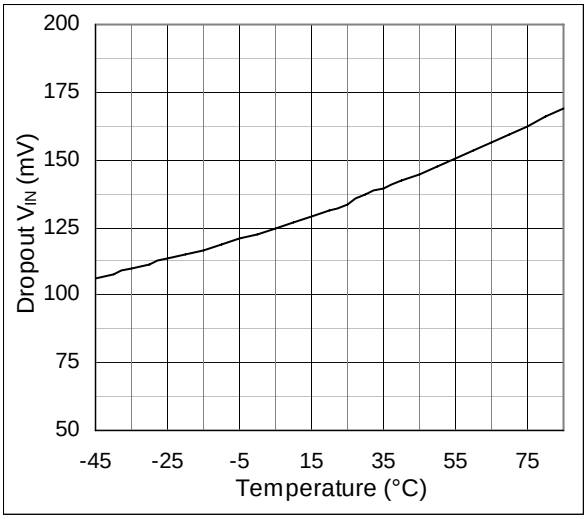



*Figure 16. Enable Start-up*

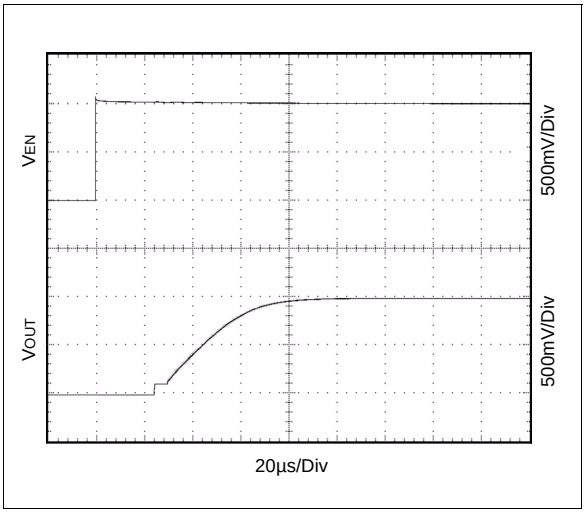



*Figure 17. Line Transient Response; $I_{OUT}$ = 350mA*

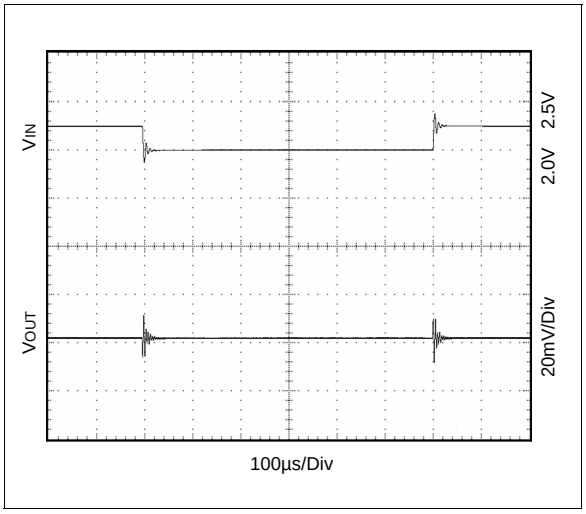
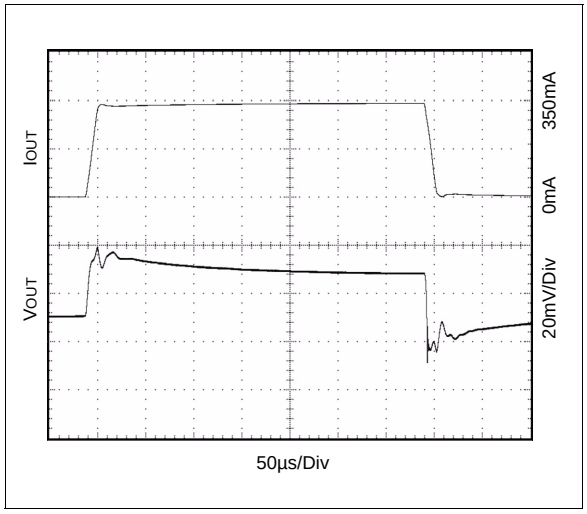



*Figure 18. Load Transient Response; $V_{IN}$ = 2.0V*



# 8 Detailed Description

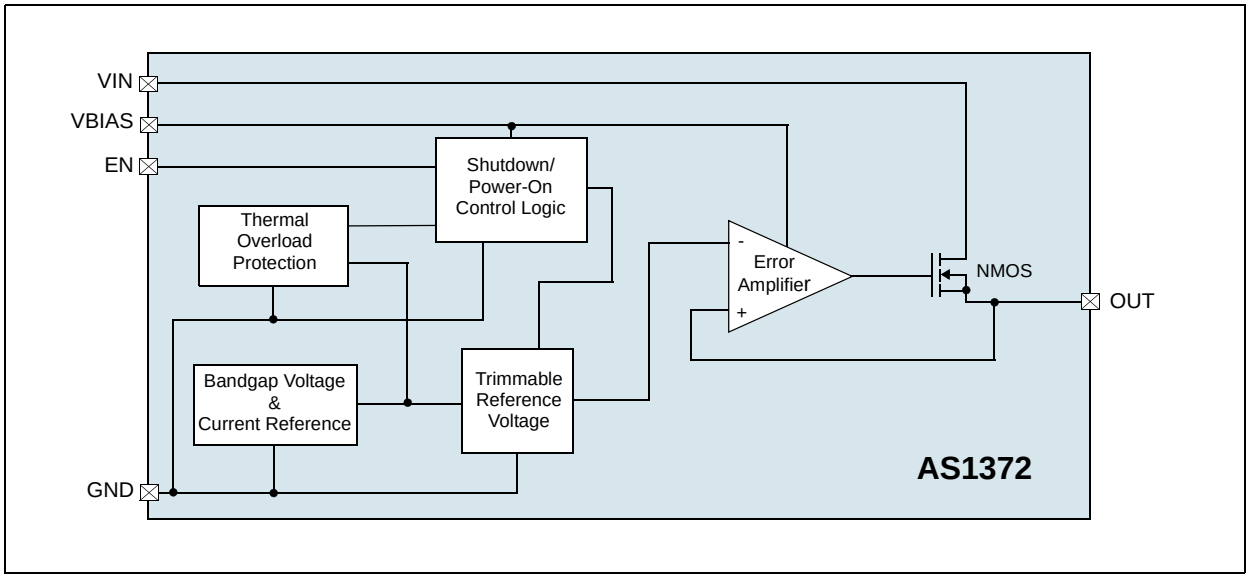
The AS1372 is a low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 350mA. All devices come with fixed output voltage from 0.5V to 2.2V. (see Ordering Information on page 13).

Shutdown current for the whole regulator is typically 10nA. The device features integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 150°C. This is a useful protection when the device is under sustained short circuit conditions.

As illustrated in Figure 19, the devices comprise voltage reference, error amplifier, N-channel MOSFET pass transistor, internal voltage divider, current limiter, thermal sensor and shutdown logic.

The bandgap reference is connected to the inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the N-channel MOSFET gate is pulled higher, allowing more current to pass to the output, and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled down, allowing less current to pass to the output. The output voltage feeds back through an internal resistor voltage divider connected to pin OUT.

*Figure 19. AS1372 - Block Diagram*




## Output Voltages

Standard products are factory-set with output voltages from 0.5V to 2.2V. A two-digit suffix of the part number identifies the nominal output (see Ordering Information on page 13). Non-standard devices are available.

For more information contact: http://www.austriamicrosystems.com/contact

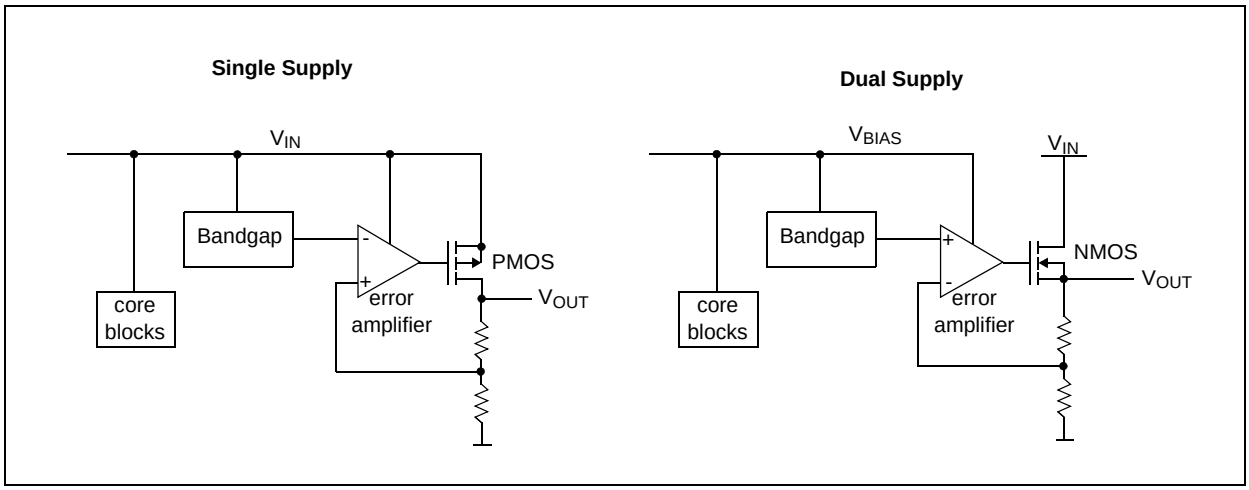
# 9 Application Information

### Advantages of dual supply architecture vs. traditional single supply approach.

If compared to the traditional single supply approach, the dual rail architecture ensures improved performances in a LDO at the expense of an additional supply voltage and a dedicated pin.

Anyhow, it is worth to note that the additional supply voltage comes for free in all those applications where the LDO is supplied by the output of a DCDC step-down converter: Vin pin is coupled to the step-down output and Vbias is shorted to the DCDC converter supply.

*Figure 20. Single vs. Dual Supply*




The former is based on a PMOS output transistor connected in a common source configuration: the supply voltage at its source is shared with all the circuit. On the other side, the dual supply approach is based on a NMOS transistor in common drain configuration having its source coincident with the regulated output of the LDO: the supply voltage at the drain is not shared with the remaining blocks of the circuit and its value can be chosen independently.

The second solution allows improved efficiency and dropout at low output reference voltage and faster transient time response.

### Improved efficiency

At heavy current load the power consumption is almost entirely located in the output transistor. This means that keeping drain to source voltage, that is the difference between input and output voltage of the LDO, as small as possible is the key factor for a good efficiency. It holds, approximately: *Efficiency = (Vout / Vin)x100 [%]*

While this achievement is little challenging in case the output voltage is large enough, traditional implementations based on a PMOS device face a serious bottleneck at low output voltage. In fact the supply voltage cannot be made consequently small because of dynamic range limitations in the core of the LDO circuitry. In many commercial cases the supply voltage cannot be made smaller than 2 or 2,5V which gives only 25% or 20% efficiency for a 500mV reference output.

On the contrary, the possibility to have a dedicated supply voltage for the output transistor offers the possibility to set the drain to source voltage of the output transistor independently from the dynamic range limitations inside the core of the circuit. Thus, even at very small output voltage, the drain to source voltage can be made quite small and guarantee optimal efficiency performance. For instance, by setting Vin at 800mV makes more than 60% efficiency for an output voltage as small as 500mV still ensuring excellent analog performances in the LDO.

### Improved dropout

Dropout mainly refers to the resistivity of the output transistor when its gate is driven to ground and the feedback regulation loop is open. Moreover when the output transistor is in dropout input and output voltages are nearly coincident. In this way, in a traditional approach, the gate to source voltage that determines the resistivity of the output PMOS in dropout is nearly equal to the output voltage. This means that a smaller output voltage brings worse dropout performances. In the dual supply approach, on the contrary, in dropout conditions the gate of the output transistor is pushed to Vbias voltage and only Vin drops nearly coincident to Vout. As Vbias can be chosen independently from Vin, even at small output voltages a large overdrive at the output transistor can be ensured and an extremely reduced dropout value comes out.

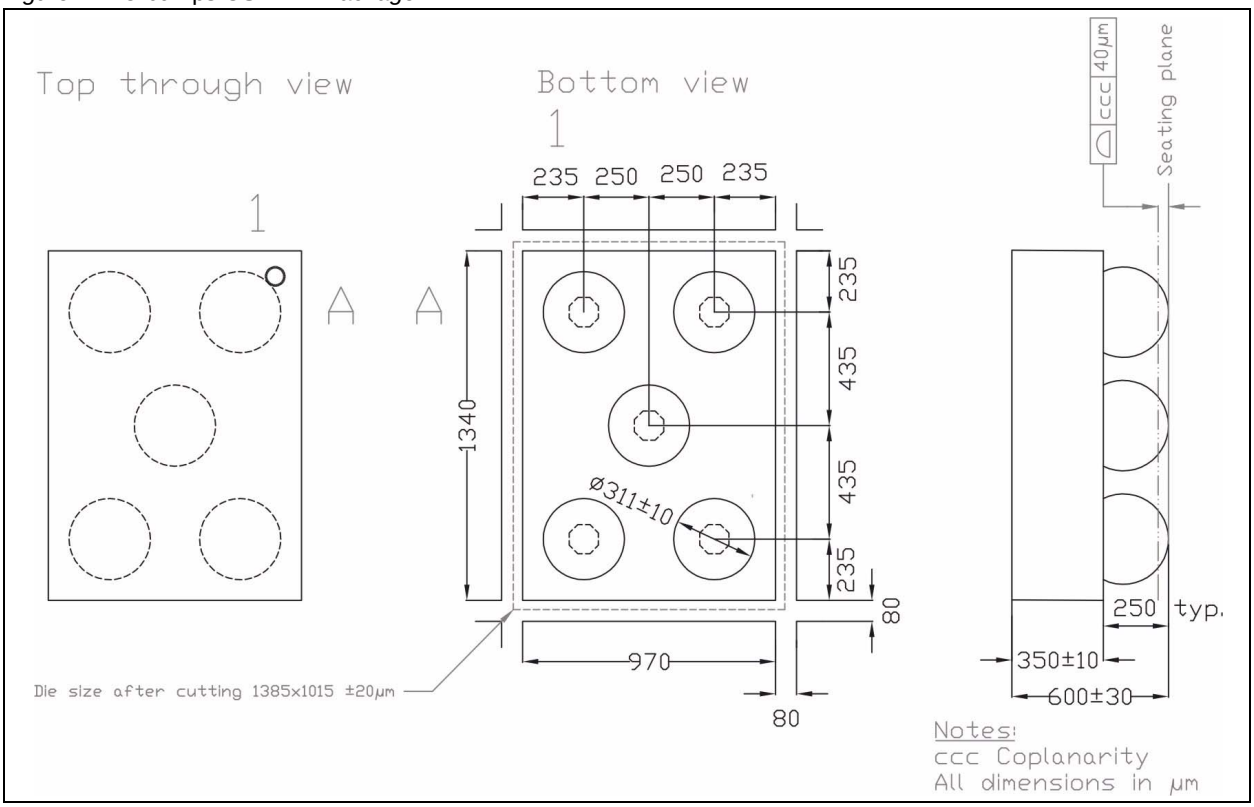
### Faster response

In a traditional approach, the output of the LDO is coincident with the drain of the output PMOS transistor. In this way, if the load current suddenly changes, any variation at the output voltage is not able to vary the output current of the LDO until it is amplified to the gate of the output PMOS by the error amplifier. A delay comes, unavoidably. On the contrary, in the dual supply approach it is the source of the output transistor to be coincident with the output voltage. In this way a change in the output voltage immediately modulates the current from the LDO and a better regulation in fast load transient is achieved.

# 10 Package Drawings and Markings

The device is available in a 5-bumps CS-WLP package.

*Figure 21.* 5-bumps CS-WLP *Package*



# 11 Ordering Information

The device is available as the standard products listed in Table 4.

*Table 4. Ordering Information*

| Ordering Code | Marking | Output | Description | Delivery Form | Package |
|---|---|---|---|---|---|
| AS1372-BWLT-07 | *) | 0.7V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-10 | ASSN | 1.0V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-12 | ASSQ | 1.2V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-13 | ASSO | 1.3V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-14 | *) | 1.4V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-15 | ASSR | 1.5V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-16 | *) | 1.6V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-18 | ASSS | 1.8V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-20 | *) | 2.0V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-24 | *) | 2.4V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-28 | *) | 2.8V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-30 | *) | 3.0V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |
| AS1372-BWLT-33 | *) | 3.3V | 350mA Dual Rail Linear Regulator | Tape and Reel | 5-bumps CS-WLP |

*) on request

Non-standard devices from 0.5V to 1.1V are available in 50mV steps and from 1.1V to 2.2V in 100mV steps. For more information and inquiries contact http://www.austriamicrosystems.com/contact

**Note:** All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

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