National Semiconductor

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LM3450

LED Driver with Active Power Factor Correction and Phase Dimming Decoder

General Description

The LM3450 is a power factor controller (PFC) with separate phase dimming decoder. The PFC regulates an accurate output voltage while maintaining excellent power factor at the input. The phase dimming decoder interprets the phase angle and remaps it to a 500Hz PWM output. This combination of features is ideal for implementing a dimmable off-line LED driver for 10-100W loads.

The phase dimming decoder has several unique features. A programmable mapping from input to output increases design flexibility, while a dynamic filter and variable sampling rate provide a fast, smooth response to dimmer movement. A dynamic hold circuit ensures that the phase dimmer angle is decoded properly while minimizing the extra power losses associated with holding current.

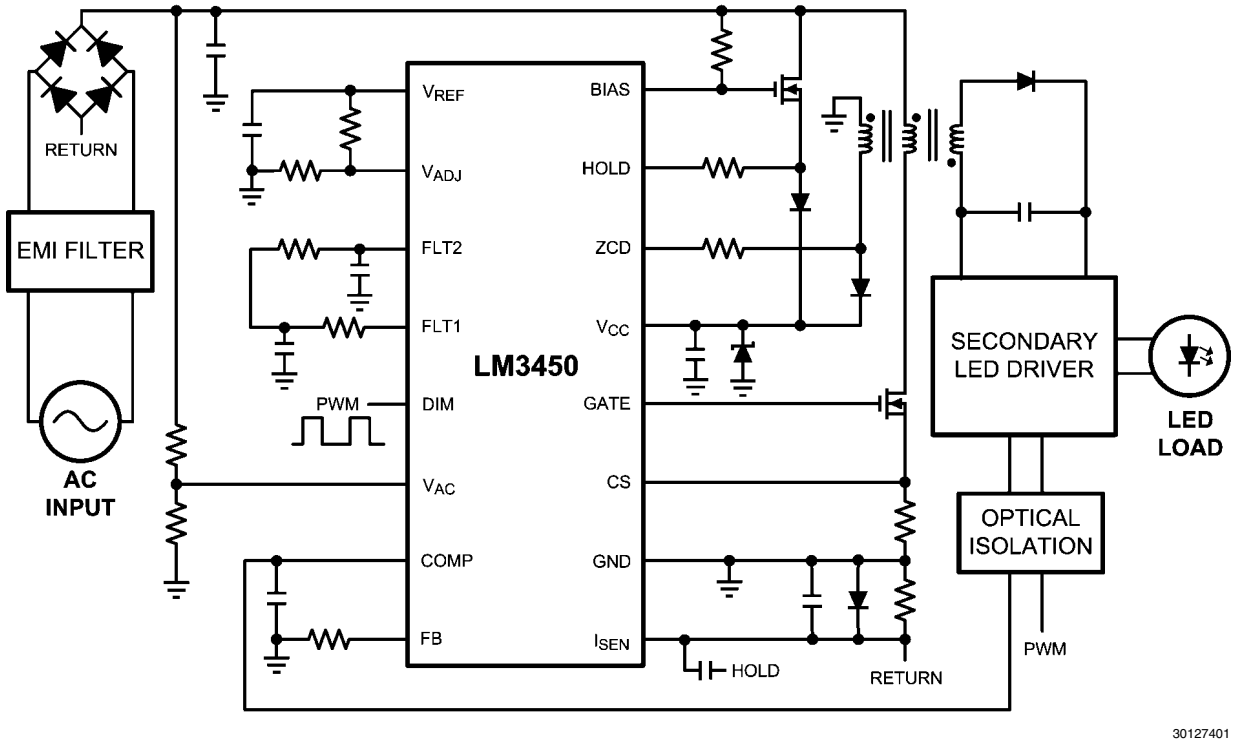
Features

- Critical conduction mode PFC
- Over-voltage protection
- Feedback short circuit protection
- 70:1 PWM decoded from phase dimmer
- Analog dimming
- Programmable dimming range
- Digital angle and dimmer detection
- Dynamic holding current
- Smooth dimming transitions
- Low power operation
- Start-up pre-regulator bias
- Precision voltage reference

Applications

- Dimmable downlights, troffers, and lowbays
- Indoor and outdoor area SSL
- Power supply PFC

Typical Application



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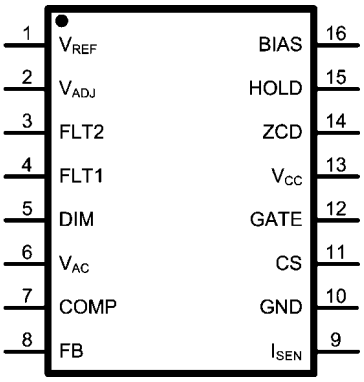
Connection Diagram

Top View



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16-Lead TSSOP
NS Package Number MTC16

Ordering Information

Order Number	Spec.	Package Type	NSC Package Drawing	Supplied As
LM3450	NOPB	TSSOP-16	MTC16	92 Units, Rail
LM3450MTX	NOPB	TSSOP-16	MTC16	2500 Units, Tape and Reel

Pin Descriptions

Pin	Name	Description	Application Information
1	V_{REF}	3V Reference	Reference Output: Connect directly to V_{ADJ} or to resistor divider feeding V_{ADJ} and to necessary external circuits.
2	V_{ADJ}	Analog Adjust	Analog Dim and Phase Dimming Range Input: Connect directly to V_{REF} to force standard 70% phase dimming range. Connect to resistor divider from V_{REF} to extend usable range of some phase dimmers or for analog dimming. Connect to GND for low power mode.
3	FLT2	Filter 2	Ramp Comparator Input: Connect a series resistor from FLT1 capacitor and a capacitor to GND to establish second filter pole.
4	FLT1	Filter 1	Angle Decoder Output: Connect a series resistor to a capacitor to GND to establish first filter pole.
5	DIM	500 Hz PWM Output	Open Drain PWM Dim Output: Connect to dimming input of output stage LED driver (directly or with isolation) to provide decoded dimming command.
6	V_{AC}	Sampled Rectified Line	Multiplier and Angle Decoder Input: Connect to resistor divider from rectified AC line.
7	COMP	Compensation	Error Amplifier Output and PWM Comparator Input: Connect a capacitor to GND to set the compensation.
8	FB	Feedback	Error Amplifier Inverting Input: Connect to output voltage via resistor divider to control PFC voltage loop for non-isolated designs. Connect a 5.11kΩ resistor to GND for isolated designs (bypasses error amplifier). Also includes over-voltage protection and shutdown modes.
9	I_{SEN}	Input Current Sense	Input Current Sense Non-Inverting Input: Connect to diode bridge return and resistor to GND to sense input current for dynamic hold. Connect a 0.1µF capacitor and Schottky diode to GND, and a 0.22µF capacitor to HOLD.
10	GND	Power Ground	System Ground
11	CS	Current Sense	MosFET Current Sense Input: Connect to positive terminal of sense resistor in PFC MosFET source.
12	GATE	Gate Drive	Gate Drive Output: Connect to gate of main power MosFET for PFC.
13	V_{CC}	Input Supply	Power Supply Input: Connect to primary bias supply. Connect a 0.1µF bypass capacitor to ground.
14	ZCD	Zero Crossing Detector	Demagnetization Sense Input: Connect a 100kΩ resistor to transformer/inductor winding to detect when all energy has been transferred.
15	HOLD	Dynamic Hold	Open Drain Dynamic Hold Input: Connect to holding resistor which is connected to source of passFET.
16	BIAS	Pre-regulator Gate Bias	Pre-regulator Gate Bias Output: Connect to gate of passFET and through resistor to rectified AC (drain of passFET) to aid with startup.

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}, HOLD, DIM, BIAS	-0.3V to 25.0V
HOLD Power	250 mW Continuous
BIAS Current	5.0mA Continuous
ZCD Current	+/- 10mA
COMP, FB, V_{AC}, FLT1, FLT2, V_{REF}, CS, V_{ADJ}	-0.3V to 7.0V
I_{SEN}	-7.0V to 7.0V
GATE	-0.3V to 18V Continuous -2.5V for 100ns 20.5V for 100ns -1mA to +1mA Continuous
Continuous Power Dissipation	Internally Limited
Maximum Junction Temperature	Internally Limited
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Solder and Reflow) (*Note 2*)	260°C
ESD Susceptibility (*Note 3*)	
HBM	2kV
MM	200V
FICDM	750V

Operating Conditions (*Note 1*)

V_{CC} Range	8.5V to 20V
Junction Temperature Range	-40°C to +125°C

Electrical Characteristics (*Note 1*)

Unless otherwise specified V_{CC} = 14V. Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = –40°C to +125°C). Typical values represent the most likely parametric norm at $T_A = T_J$ = +25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min (*Note 4*)	Typ (*Note 5*)	Max (*Note 4*)	Units
SUPPLY VOLTAGE INPUT (V_{CC})						
$V_{CC-RISE}$	Controller Enable Threshold	V_{CC} Rising	**12.2**	13.0	**13.6**	V
$V_{CC-FALL}$	Controller Disable Threshold	V_{CC} Falling	**7.4**	7.9	**8.5**	
	Glitch Filter Delay			9		µs
	Turn-on Delay			40		
I_Q	V_{CC} Quiescent Current	No Switching		1.6		mA
I_{Q-SD}	V_{CC} Shutdown Current	V_{FB} = 0V		515	**625**	µA
ERROR AMPLIFIER & COMPENSATION (FB, COMP)						
V_{FB}	FB Reference (Normal Operation)		**2.43**	2.50	**2.57**	V
	Input Bias Current	V_{FB} = 2.5V		100		nA
G_M	Transconductance	V_{FB} = 2.5V	**69**	115	**161**	µS
	Output Source / Sink Capability		**60**	85	**110**	µA
	FB Pull-up Current Source	V_{FB} < 1.8V	**43**	51	**59**	
	COMP Pull-up Resistor			5		kΩ
V_{CMP-B}	COMP Low Threshold (Burst)	V_{CMP} Falling		V_{THM} -0.08		V
	COMP Low Hysteresis			20		mV
V_{FB-SD}	Low Threshold (Shutdown)	V_{FB} Falling	**150**	168	**186**	
	FB Low Hysteresis			20		
V_{FB-EAD}	FB Mid Threshold (EA Disabled)	V_{FB} Falling	**328**	346	**368**	
	FB Mid Hysteresis			20		
V_{FB-OV}	FB High Threshold (Over-voltage)			1.20 x V_{FB}	**1.22 x V_{FB}**	V
	COMP Pre-bias Source Current	V_{CMP} = 0.5V		415		µA
V_{THM}	Minimum COMP Voltage (Normal)			1.47		V
ANGLE DEMODULATION & MULTIPLIER (COMP, V_{AC})						
V_{AC-DET}	V_{AC} Angle Detection Threshold		**334**	356	**378**	mV
	Angle Demodulation Delay Time	Both edges		8		µs
	VAC Dynamic Input Voltage Range		0 to 5.5			V
	COMP Dynamic Input Voltage Range		V_{THM} to V_{THM} +2			
	V_{AC} Input Impedance			500		kΩ

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
K_M	Multiplier Gain (Includes Internal Resistor Divider)	V_{AC} = 3V, V_{CMP} = V_{THM}+1.5V		0.5		1/V
ZERO CURRENT DETECTOR (ZCD)						
$V_{ZCD-RIS}$	ZCD Input Threshold	V_{ZCD} Rising	**1.45**	1.5	**1.55**	V
	Hysteresis		**150**	200	**250**	mV
	Delay to Output			135		ns
V_{ZCD-H}	Positive Clamp Voltage	I_{ZCD} = 1mA		6.0		V
V_{ZCD-L}	Negative Clamp Voltage	I_{ZCD} = -50µA		0.61		
PWM COMPARATOR (CS)						
V_{OS}	PWM Comparator Input Offset Voltage			30		mV
	PWM Comparator Input Bias Current			20		nA
V_{LIM}	CS Current Limit Threshold		**1.40**	1.50	**1.60**	V
	CS Delay to Output			100		ns
	CS Blanking Sinking Impedance			1		kΩ
t_{LEB}	Leading Edge Blanking (LEB) Time			140		ns
ANALOG ADJUST INPUT (V_{ADJ})						
V_{ADJ-LP}	V_{ADJ} Low Threshold (Low Power Mode)	V_{ADJ} Falling	**56**	75		mV
	V_{ADJ} Low Hysteresis			50		
	V_{ADJ} Pull-up Current Source			1		µA
	V_{ADJ} Open Voltage	V_{ADJ} Open		3		V
DYNAMIC HOLD CIRCUIT (HOLD, I_{SEN})						
$R_{DSON-HD}$	HOLD MosFET On-Resistance	ISEN Short to GND	**22**	30	**42**	Ω
$V_{SEN-REF}$	I_{SEN} Reference Voltage		**162**	200	**232**	mV
	I_{SEN} Bias Current			5		µA
PRE-REGULATOR GATE DRIVE OUTPUT (BIAS)						
V_{BIAS}	BIAS High Voltage @ 100µA	V_{CC} < $V_{CC-FALL}$	**18.8**	21	**22.6**	V
	BIAS Low Voltage @ 100µA	V_{CC} > $V_{CC-RISE}$	**13.5**	14	**14.5**	
GATE DRIVER OUTPUT (GATE)						
V_{GATE-H}	GATE Voltage High	I_{GATE} = 20mA		11.5		V
		I_{GATE} = 200mA		10.5		
	GATE Pull Down Resistance			2	**8**	Ω
	GATE Peak Current	(Note 6)		±1.5		A
REFERENCE VOLTAGE OUTPUT (V_{REF})						
V_{REF}	Reference Voltage	No Load	**2.85**	3	**3.15**	V
	Current Limit		**1.5**	2.0	**3.0**	mA
DIMMING OUTPUT (DIM, FLT1, FLT2)						
	FLT1 Output Impedance	Standby Mode		500		kΩ
		Transition Mode		1.6		
	Triangle Waveform Compared to FLT2	High		1.49		V
		Low		15		mV
f_{DIM}	DIM Frequency		**180**	460	**700**	Hz
OFF-TIMERS						
$t_{OFF-MAX}$	Maximum Off-Time (Normal Operation)			340		µs
t_{OFF-LP}	Off-Time (Low Power Mode)			42		

Symbol	Parameter	Conditions	Min (*Note 4*)	Typ (*Note 5*)	Max (*Note 4*)	Units
THERMAL SHUTDOWN						
	Thermal Limit Threshold	(*Note 6*)		160		°C
	Thermal Limit Hysteresis			20		
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	TSSOP-16 (*Note 6*, *Note 7*)		38.0		°C/W
θ_{JC}	Junction to Case			10.0		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed and do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

Note 2: Refer to National's packaging website for more detailed information and mounting techniques. http://www.national.com/analog/packaging/

Note 3: Human Body Model, applicable std. JESD22-A114-C. Machine Model, applicable std. JESD22-A115-A. Field Induced Charge Device Model, applicable std. JESD22-C101-C.

Note 4: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 5: Typical numbers are at 25°C and represent the most likely norm.

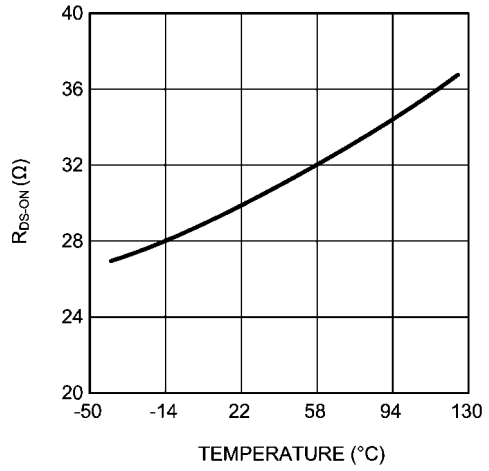
Note 6: These electrical parameters are guaranteed by design, and are not verified by test.

Note 7: Junction-to-ambient thermal resistance is highly board-layout dependent. In applications where high maximum power dissipation exists, namely driving a large MOSFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C for Q1, or 150°C for Q0), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} - (\theta_{JA} \times P_{D\text{-}MAX})$.

Typical Performance Characteristics

T_A=+25°C and V_{CC} = 14V unless otherwise specified

HOLD R_{DSON} vs. Junction Temperature



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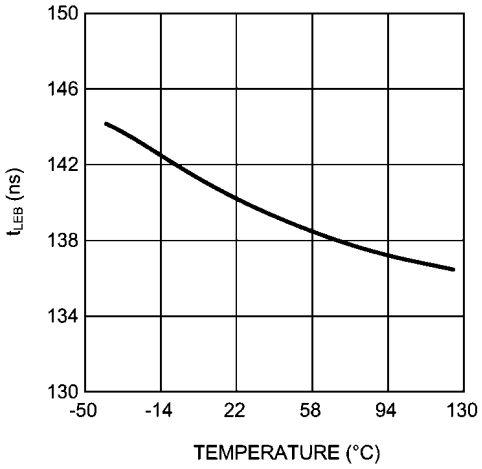
Leading Edge Blanking vs. Junction Temperature



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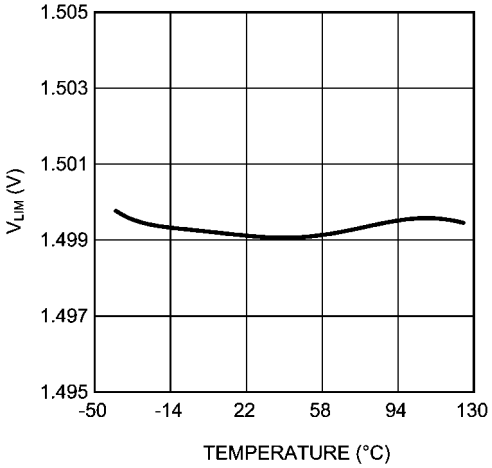
Current Limit Threshold vs. Junction Temperature
V_{AC} = 3V; V_{CMP} = V_{THM} + 1.5V



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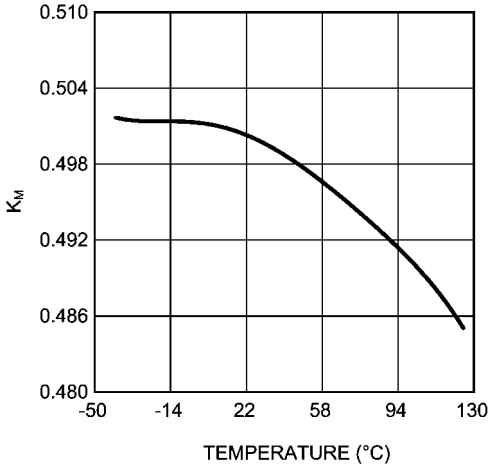
Multiplier Gain vs. Junction Temperature
V_{AC} = 3V; V_{CMP} = V_{THM} + 1.5V



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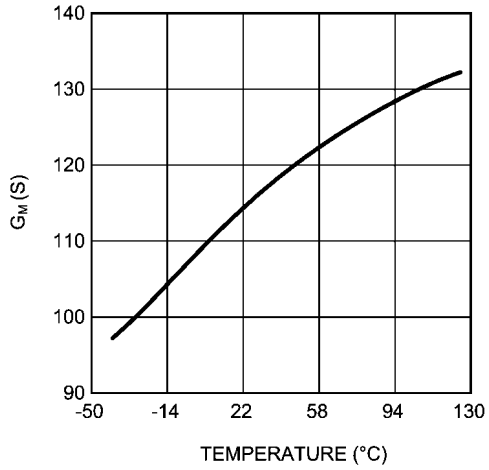
Transconductance
V_{FB} = 2.5V; ΔV_{FB} = 50mV



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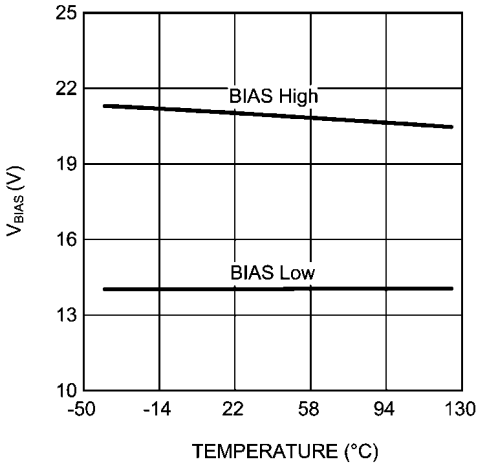
BIAS Voltage vs. Junction Temperature
High @ V_{CC} < V_{CCFALL}; Low @ V_{CC} > V_{CCRISE}



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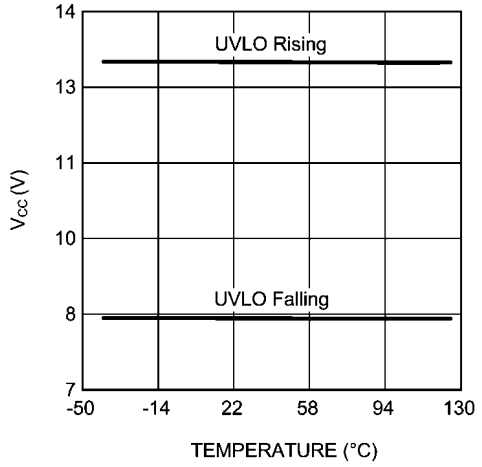
V_{CC} UVLO Threshold vs. Junction Temperature



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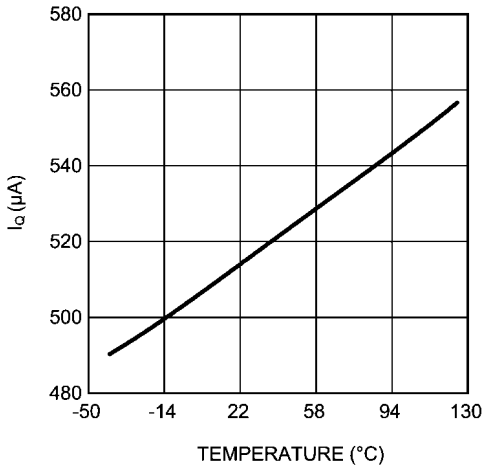
Shutdown Current vs. Junction Temperature



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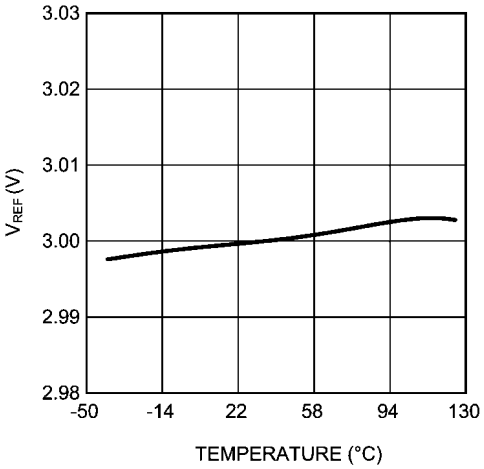
V_{REF} Reference vs. Junction Temperature



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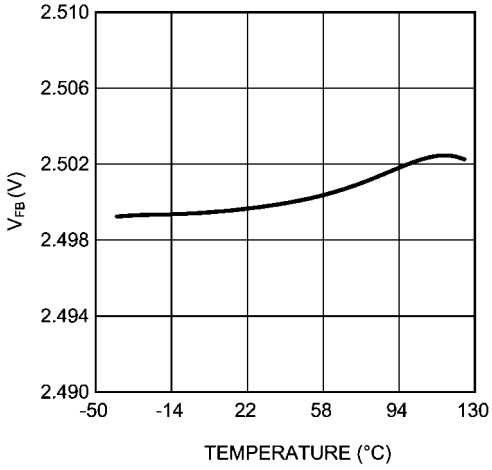
FB Reference vs. Junction Temperature



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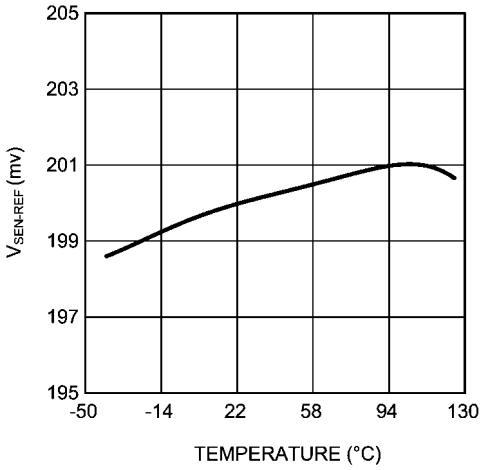
I_{SEN} Reference vs. Junction Temperature



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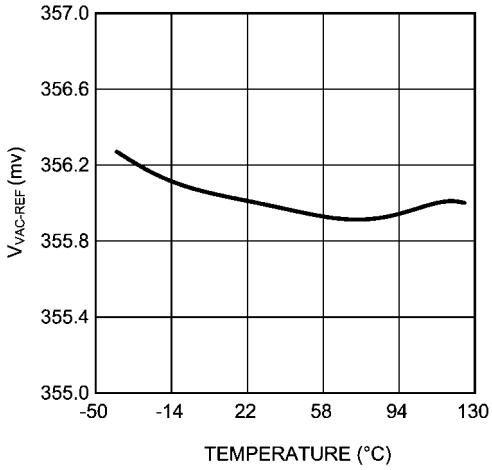
V_{AC} Detection Threshold vs. Junction Temperature



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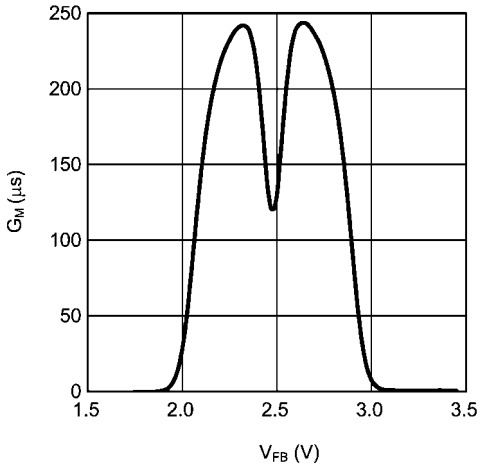
Transconductance vs. V_{FB}



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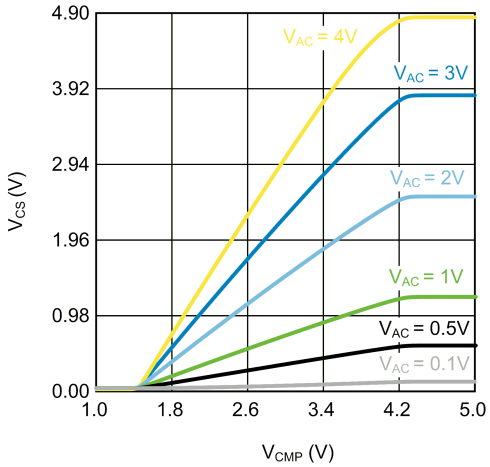
Current Sense Threshold vs. V_{COMP} and V_{AC}



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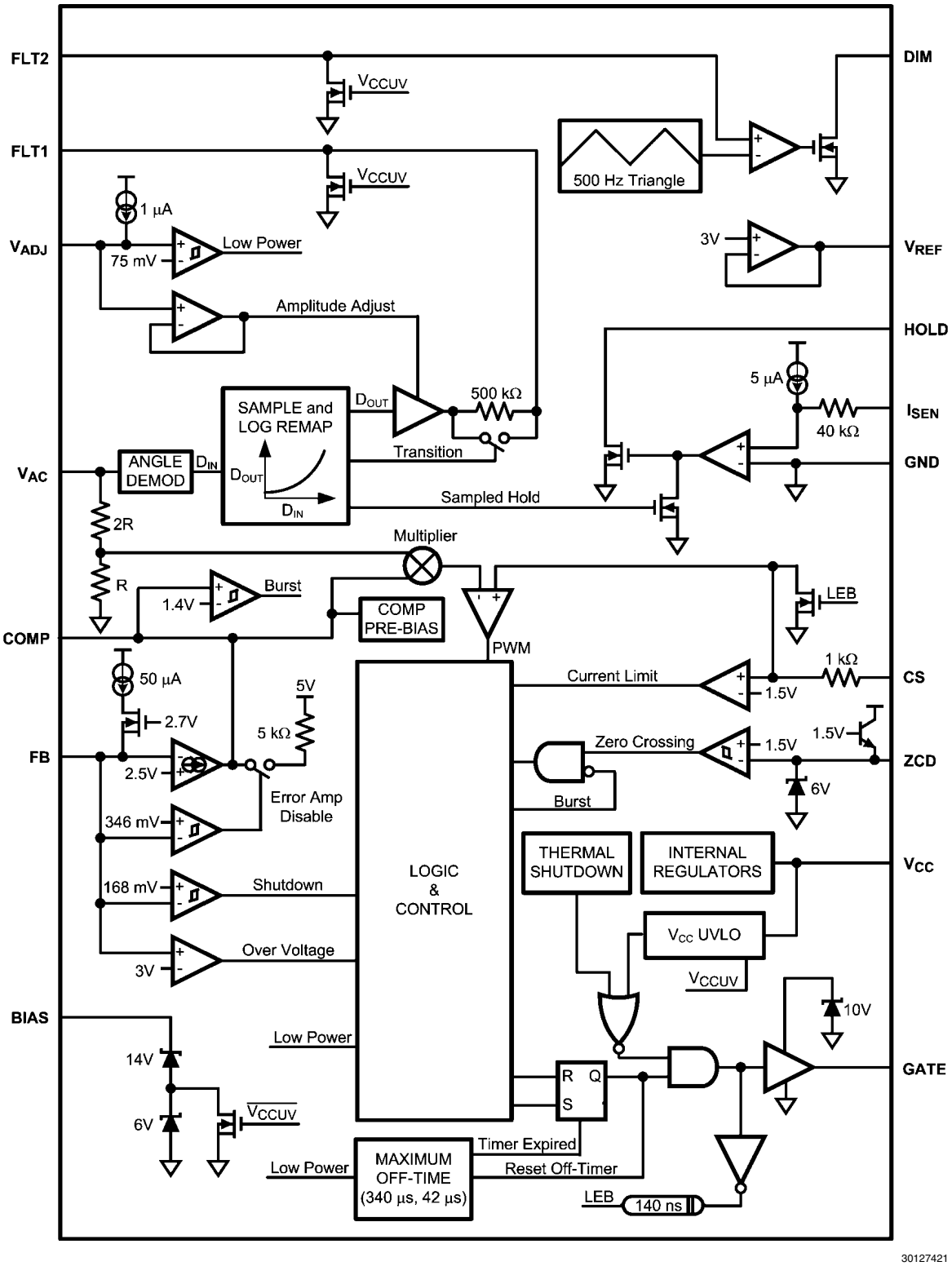
Block Diagram



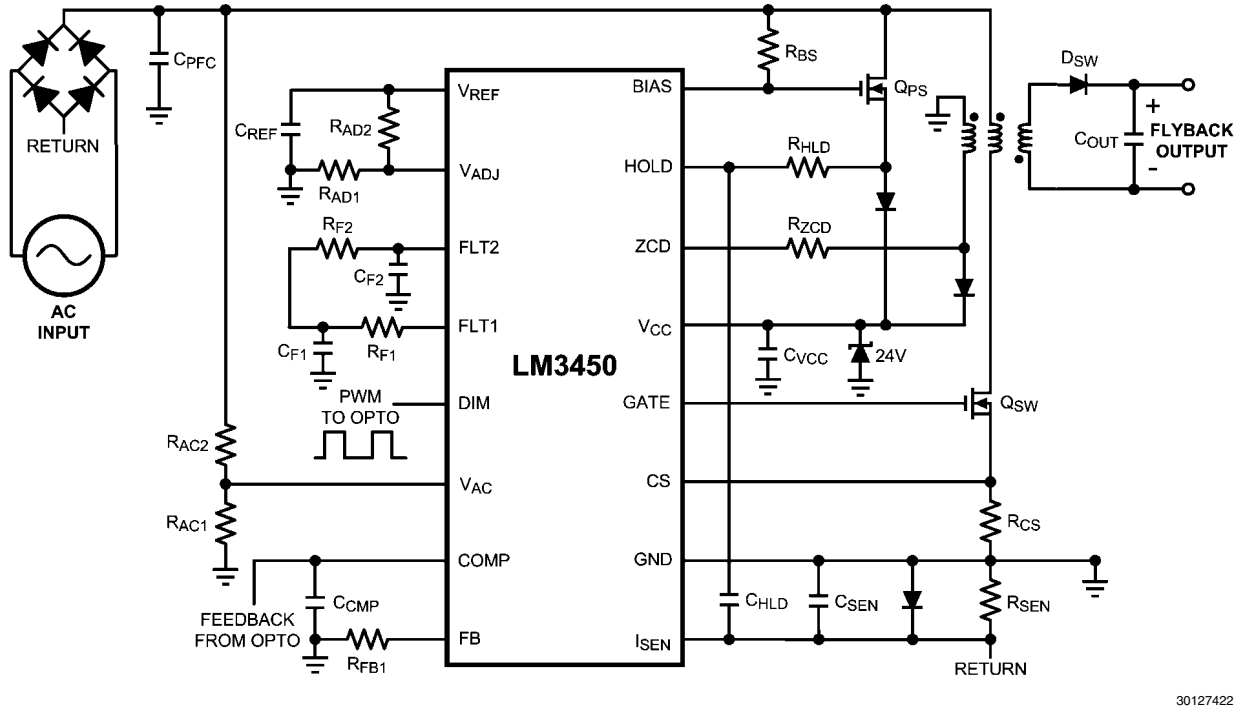


FIGURE 1. Typical Flyback Application

Theory of Operation

The LM3450 is a single device with both power factor control (PFC) and phase dimming decoder functions. This device is designed to control isolated flyback converters and provide active power factor correction. In addition to being a PFC, the LM3450 can interpret a phase dimming (frequently called triac dimming) input and provide a corresponding PWM output to properly dim an LED load. This combination of features provides an excellent method to convert a standard AC mains input to a dimmable LED output of 10-100W. It should be noted that the LM3450 can control a boost converter in a similar manner. However, this datasheet will focus mostly on the flyback topology due to the high demand for isolated LED driver applications. Discussion of the LM3450 functionality will refer to *Figure 1* component designators.

The PFC control operates in critical conduction mode (CRM) using zero crossing detection (ZCD) to terminate the off-time. The PFC portion of this device includes an error amplifier, multiplier, current sense circuit, zero crossing detector, and gate driver. The internal error amplifier is used for feedback of the output voltage in non-isolated designs. However, it can be disabled for isolated designs where the error amplifier needs to be on the secondary side.

The phase dimmer decoder detects the dimming angle of the rectified AC line, decodes, filters and remaps it to a 500Hz PWM output. The PWM output can then be sent directly, or through optical isolation, to the dimming input of a second stage LED driver. To ensure the decoder properly interprets the dimming angle, dynamic hold is provided which prevents the phase dimmer from misfiring. The input current is sensed and when the current drops below a preset minimum, the system adds more current.

Both the dynamic hold and the decoder are sampled synchronously to reduce the overall efficiency drop due to the additional hold current. When a decoding sample period occurs, the dynamic hold is activated to ensure a proper angle is decoded. Because of this sampling method, non-sampled cycles will potentially cause the phase dimmer to misfire but should not affect the output LED current regulation. Finally, the dynamic filter and variable sampling rate provide fast, smooth dimming transitions.

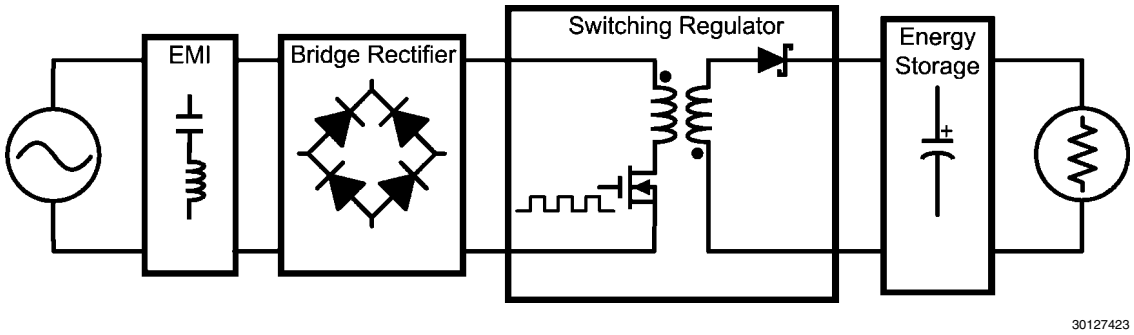


FIGURE 2. PFC System Architecture

PFC BACKGROUND

Power factor (PF) is a number between 0 and 1 that indicates how well energy is transmitted from input to output of a system. It can be described by average power (P_{AVG}), RMS voltage (V_{RMS}), and RMS current (I_{RMS}):

$$PF = \frac{P_{AVG}}{V_{RMS} \times I_{RMS}}$$

Or by distortion factor (K_{DIST}) and displacement factor (K_{DISP}):

$$PF = K_{DIST} \times K_{DISP}$$

With a purely resistive system, PF = 1. The addition of reactive elements necessary in any converter, such as EMI filters and energy storage, will induce some amount of displacement (phase shift between the input voltage and input current). The addition of switching devices will also create distortion (energy present in the harmonics relative to the switching frequencies). These non-idealities decrease the PF towards zero.

Active power factor correction attempts to make the input impedance look as resistive as possible to the power source. Since the output of the converter is usually a regulated voltage or current, there is a need for large energy storage elements to remove the twice line frequency (100Hz or 120Hz) ripple. A power factor control architecture, as shown in *Figure 2*, has very little capacitance at the input. Instead, the twice line frequency content is removed with large energy storage capacitance at the output.

With minimal input capacitance, the converter is able to provide two important functions at the same time:

- Shape the input current
- Regulate the output voltage

The PFC control approach requires two separate control loops to achieve both functions: a fast loop which shapes the input current, and a slow loop that regulates the output voltage.

The fast control loop shapes the input current to have the same sinusoidal shape as the AC input voltage. Assuming both are perfect sinusoids with zero distortion or phase shift, the power factor will be perfect (unity). Unfortunately, distortion is always present in switching converters. An input filter, which is required to comply with EMI standards, helps to attenuate the switching content, thereby reducing distortion. However, the added filter capacitance will increase the phase shift at the same time. Though perfect PF is not achievable within real applications, extremely high PF (>.99) is possible using most active PFCs.

The output voltage has to be regulated slowly to ensure the converter ignores the twice line frequency ripple present on the output. Therefore, the voltage loop containing the error amplifier should have a bandwidth at least an order of magnitude slower (<20Hz is common). Sometimes the bandwidth is increased to improve transient response, which is the case with off-line dimmable LED drivers. Though PF decreases with the increase in bandwidth, high PF (>.95) is still possible.

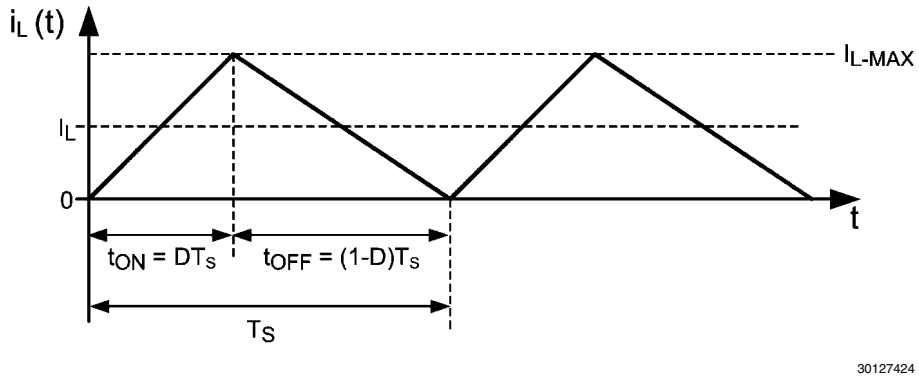


FIGURE 3. Basic CRM Inductor Current Waveform

CRM BACKGROUND

During critical conduction mode (CRM), a converter operates at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). This is usually implemented as follows. The main switching MosFET (Q_{SW}) is turned on and the inductor current rises to a peak threshold. Q_{SW} is then turned off and the current falls until it reaches zero. At this point, Q_{SW} is turned on and the cycle repeats. Near zero voltage switching, enabled by the inductor current return to zero, gives CRM topologies an efficiency improvement compared to CCM topologies. *Figure 3* shows the resulting inductor current waveform, where the average inductor current (I_L) is half of the peak current ($I_{L\text{-}MAX}$).

In a CRM flyback PFC application, the rectified AC input is fed forward to the control loop, creating a sinusoidal primary peak current envelope ($I_{P\text{-}pk}$) as shown in *Figure 4*. The secondary peak current envelope ($I_{S\text{-}pk}$) will simply be a scaled version of the primary according to the turns ratio of the transformer. Assuming good attenuation of the switching ripple via the EMI filter, the average input current (I_{IN}), represented by the red line in *Figure 4*, can also be approximated as a sinusoid proportional to the duty cycle (D(t)):

$$I_{in}(t) = \frac{I_{P\text{-}PK} \times D(t)}{2}$$

Since CRM operation is hysteretic and the input voltage is fedforward, the input current shaping loop is as fast as possible. Only the output voltage needs to be regulated with a narrow bandwidth error amplifier, which greatly simplifies the system dynamics.

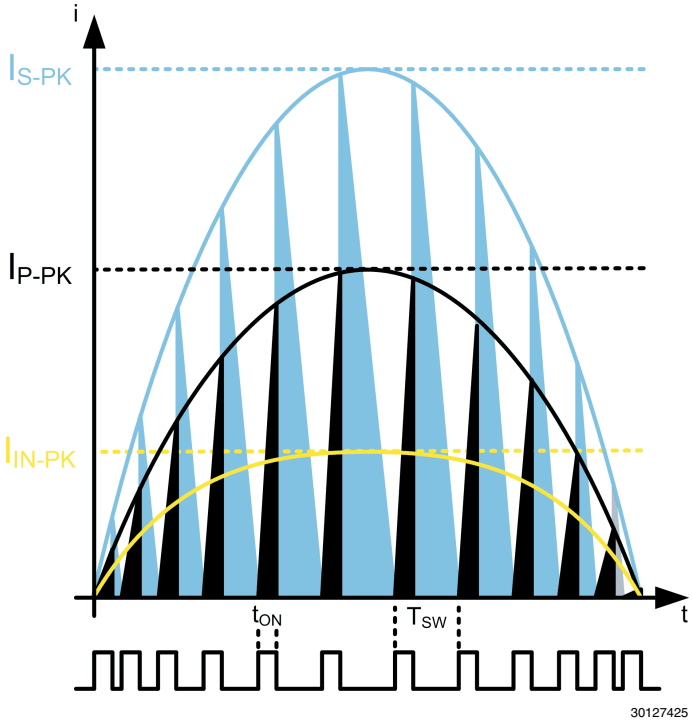


FIGURE 4. CRM Flyback Current Waveforms

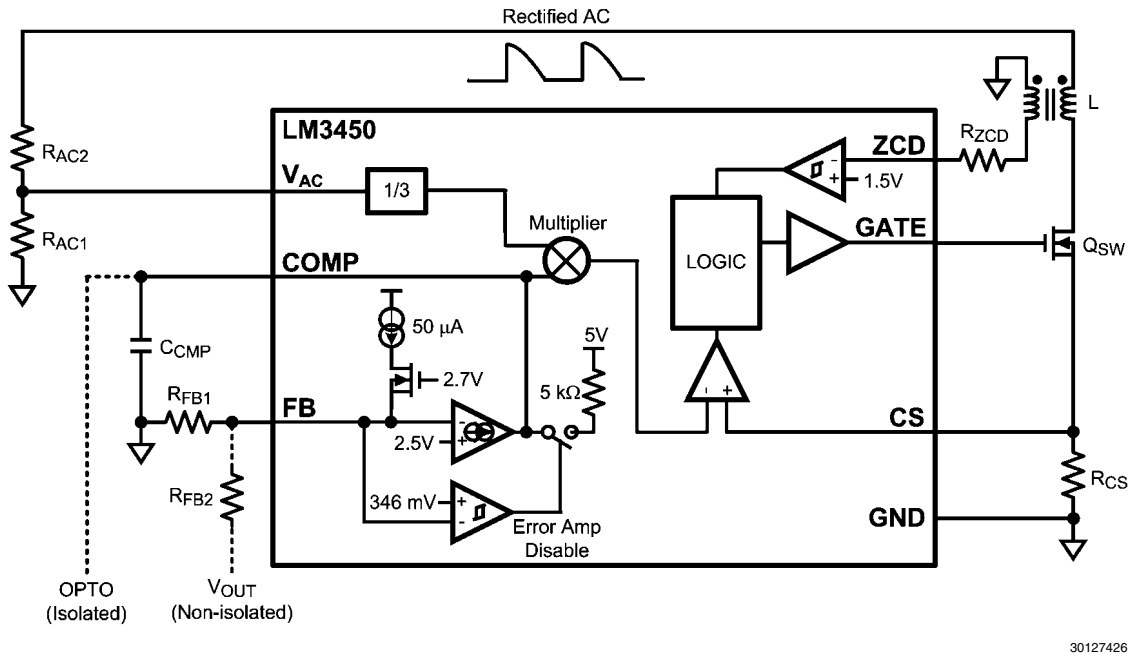


FIGURE 5. PFC Control Circuit

POWER FACTOR CONTROLLER

The LM3450 uses CRM control to regulate the output voltage and provide power factor correction. In a non-isolated boost topology, an external voltage divider (R_{FB1}, R_{FB2}) is used to sense the output voltage, as shown in *Figure 5*. The divider is connected to the inverting input (FB) of the internal error amplifier. The LM3450 regulates the feedback voltage (V_{FB}) to 2.5V in a closed loop fashion.

The FB pin has a shutdown mode to protect against a feedback short which can cause excessive energy transfer to the output. In the same manner, the FB pin also has an OVP mode which terminates switching when output over-voltage is sensed.

With the FB shutdown mode, it is necessary to have a preliminary biasing method for the output of the error amplifier (COMP). Otherwise, the converter would never start. COMP is pre-biased with a 415µA current until the voltage at COMP (V_{CMP}) exceeds the minimum operational voltage (V_{THM}).

For an isolated topology flyback topology, where the error amplifier is on the secondary, the LM3450 internal error amplifier can be bypassed engaging a 5kΩ pull-up resistor at COMP. COMP can then be connected directly to the optical isolation as shown in *Figure 5*.

COMP and the sensed rectified AC input voltage (V_{AC}), provided via a resistor divider (R_{AC1}, RAC2), are inputs to the multiplier. The current through the sense resistor (R_{CS}) produces a voltage (V_{CS}) that is compared to the multiplier output. When V_{CS} exceeds the multiplier output, Q_{SW} is turned off. The peak detect threshold and the current slope during an on-time are proportionally changing which yields a nearly constant on-time, shown in *Figure 4*:

$$t_{ON} = \frac{L \times I_{P\text{-}PK}}{V_{IN\text{-}PK}}$$

Once Q_{SW} is turned off, the LM3450 waits until the inductor (boost) or transformer (flyback) is demagnetized to turn Q_{SW} on again. Demagnetization, sensed at ZCD, occurs when the current through the magnetic component falls to zero. Since the output voltage is regulated, the slope of the current remains relatively constant and, coupled with the variable peak detect, creates a variable off-time.

The sinusoidal peak detection envelope creates an input current that is sinusoidal and in phase with the input voltage providing excellent PF. The PWM comparator 30mV input offset voltage ensures current is also drawn at the zero-crossings of the rectified AC line, reducing distortion and further improving PF.

CURRENT SENSE

The LM3450 senses current through Q_{SW} via a sense resistor (R_{CS}) between the source of Q_{SW} and GND. When V_{CS} exceeds the output of the multiplier (V_{MLT}), Q_{SW} is turned off. V_{MLT} is variable over the line cycle and is a function of the scaled rectified AC voltage (V_{AC}), the COMP voltage referenced from its operational minimum (V_{COMP}-V_{THM}), the multiplier gain (K_M) and the PWM comparator offset (V_{OS}):

$$V_{MLT} = K_M \times V_{AC} \times (V_{COMP} - V_{THM}) + V_{OS}$$

It should be noted that the LM3450 leading edge blanking (LEB) circuit pulls the current sense input to the PWM comparator low for 140µs at the beginning of each on-time. The LEB blanks the current spike and associated ringing due to the turn-on transient of Q_{SW}, limiting the minimum achievable duty cycle.

OVER CURRENT PROTECTION

The LM3450 has a current limit threshold (V_{LIM} = 1.5V) at CS to protect Q_{SW} along with the rest of the system from overcurrent conditions. If V_{CS} exceeds V_{LIM}, Q_{SW} is immediately turned off.

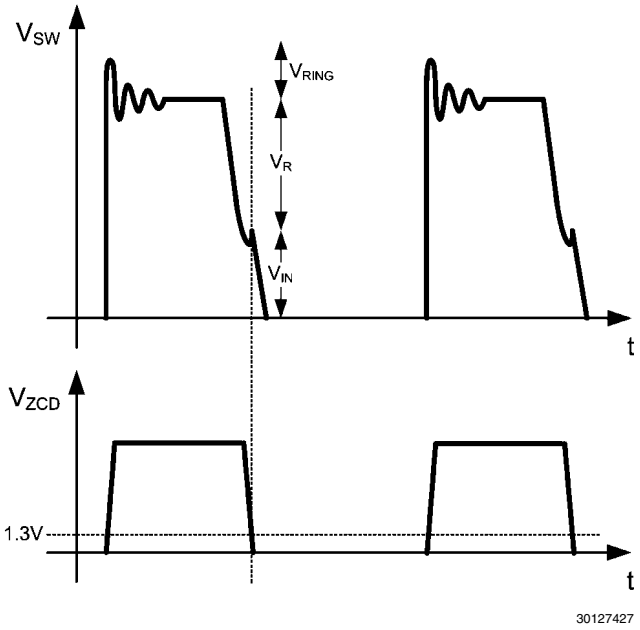


FIGURE 6. ZCD Waveforms for Flyback Design

ZERO CURRENT DETECTION

ZCD is implemented with a 100kΩ resistor from the ZCD pin to a coupled winding on the transformer or inductor as shown in *Figure 5*. This winding is also used to bootstrap V_{CC} after start-up. When Q_{SW} turns off, the voltage at the ZCD pin (V_{ZCD}) increases as energy is transferred through the auxiliary winding. The circuit arms when V_{ZCD} exceeds 1.5V. Then, when the energy is fully transferred, V_{ZCD} decreases towards zero. When V_{ZCD} falls below 1.3V, the transformer is assumed to be fully demagnetized, the circuit disarms, and Q_{SW} is turned back on as shown in *Figure 6*. The ZCD pin will remain low until Q_{SW} is turned off via peak detection and the cycle repeats.

SWITCHING FREQUENCY

With a constant on-time and variable off-time, there is a variable switching frequency:

$$f_{SW} = D(t) \times \left(\frac{V_{IN\text{-}PK}}{L \times I_{P\text{-}PK}} \right)$$

Figure 4 shows that the minimum switching frequency occurs at the peak of the rectified AC waveform, while the maximum switching frequency occurs at the valley.

ERROR AMPLIFIER

The LM3450 internal error amplifier is used for non-isolated designs (boost) where the output voltage can be directly sensed, via a resistor divider, at the FB pin. The FB pin is the inverting input of the trans-conductance amplifier which is regulated to 2.5V. The COMP pin is the output of the amplifier and external compensation is placed from COMP to GND in the form of a single capacitor (C_{CMP}) as shown in *Figure 5*, a series resistor and capacitor, or both. The output of the amplifier sources or sinks current as necessary to force the inputs of the amplifier to be equal. The compensation method depends upon the transient performance desired and requires a loop gain analysis. This analysis can be somewhat complex and cumbersome. To aid the designer, Table 1 in the Appendix gives compensation recommendations for a variety of applications. If a detailed analysis is desired, see Application Note AN-2098.

If the COMP pin voltage (V_{CMP}) falls below 1.4V at any time, the device enters burst mode where the GATE is off for 340µs then is turned on. If V_{CMP} is still below 1.4V at the end of the on-time then another 340µs off-time occurs. However, if V_{CMP} has risen above 1.4V, the converter continues switching until it falls below the threshold again. This feature is necessary to prevent the output of the converter from rising arbitrarily high because the minimum on-time of the device prevents less energy transfer.

The LM3450 also implements both feedback short circuit protection and output over-voltage protection (OVP) functions at the FB pin. If V_{FB} exceeds 3V, then OVP is engaged and the part stops switching until V_{FB} falls below 3V. In the same manner, if V_{FB} falls below 168mV, then shutdown is engaged and switching stops until V_{FB} exceeds 188mV.

The flyback topology is frequently used to provide isolation from input to output. Since, the current transfer ratio (CTR) of standard optical isolation varies over temperature, proper regulation using primary error amplifiers is difficult. An error amplifier is usually placed in the secondary to regulate the output voltage accurately. To accommodate isolated designs, the LM3450 internal error amplifier can be bypassed by placing a 5.11kΩ resistor from FB to GND. This engages a 5kΩ pull-up resistor from COMP to an internal 5V rail.

SECONDARY ERROR AMPLIFIER

For isolated designs, the error amplifier on the secondary should take the form of a proportional integral (PI) compensator. The amplifier is frequently implemented with a LM431 (low cost with internal reference). The output voltage resistor divider (R_{FB1}, R_{FB2}) provides the scaled output voltage to the LM431 inverting input. The PI compensation is achieved by connecting R_{SC} and C_{SC} in between the LM431 input and output, shown in *Figure 7*.

In addition to the basic error amplifier, a soft-start circuit can be implemented using a capacitor, two diodes and a Zener diode as shown in *Figure 7*. C_{CMP} is placed from COMP to GND for high frequency noise attenuation.

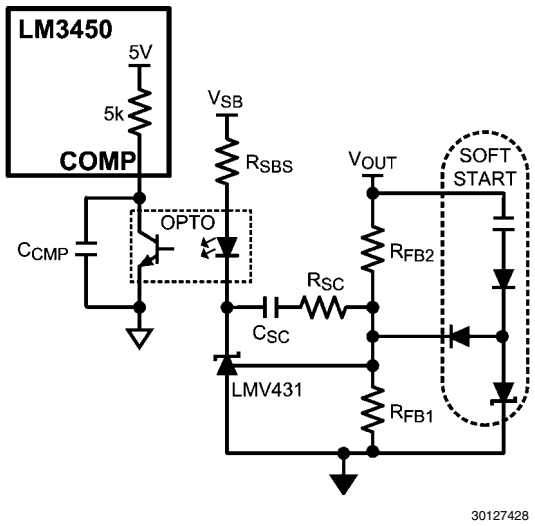


FIGURE 7. Secondary Error Amplifier

PHASE DIMMER OPERATION

A simplified schematic of a phase dimmer is shown in *Figure 8*. An RC network consisting of R1, R2, and C1 delay the turn-on of the triac until the voltage on C1 reaches the trigger voltage of the diac. Increasing the resistance of the potentiometer (wiper moving downward) increases the turn-on delay which decreases the on-time or "conduction angle" of the triac (θ). This reduces the average power delivered to the load.

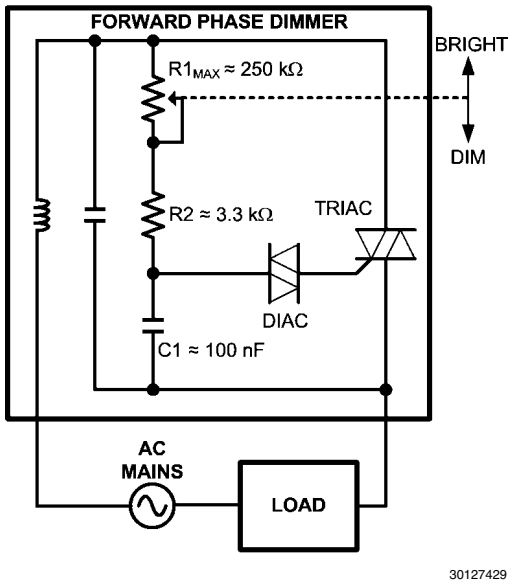


FIGURE 8. Basic Forward Phase Dimmer

Phase dimmer voltage waveforms are shown in *Figure 9*.

Figure 9a shows the full sinusoid of the input voltage. Even when set to full brightness; few dimmers will provide 100% conduction angle.

Figure 9b shows a waveform from a forward phase dimmer. The off-time can be referred to as the firing angle and is simply 180° – θ.

Figure 9c shows the waveform of a reverse phase dimmer (also called an electronic dimmer in the lighting industry). These typically or more expensive, microcontroller based dimmers that use switching devices other than triacs. Note that the conduction angle starts from the zero-crossing, and terminates some time later. This method of control reduces the noise spike at the transition.

Any form of phase dimming modulates the incoming AC waveform by chopping part of the sinusoid, reducing the average power to the load. These dimmers work very well with standard incandescent bulbs, but not with power converters. A converter attempts to regulate the load in with presence of any input, effectively ignoring the phase angle. To implement a dimmable converter, the angle must be sensed at the input, decoded and used to properly control the LED current regulator.

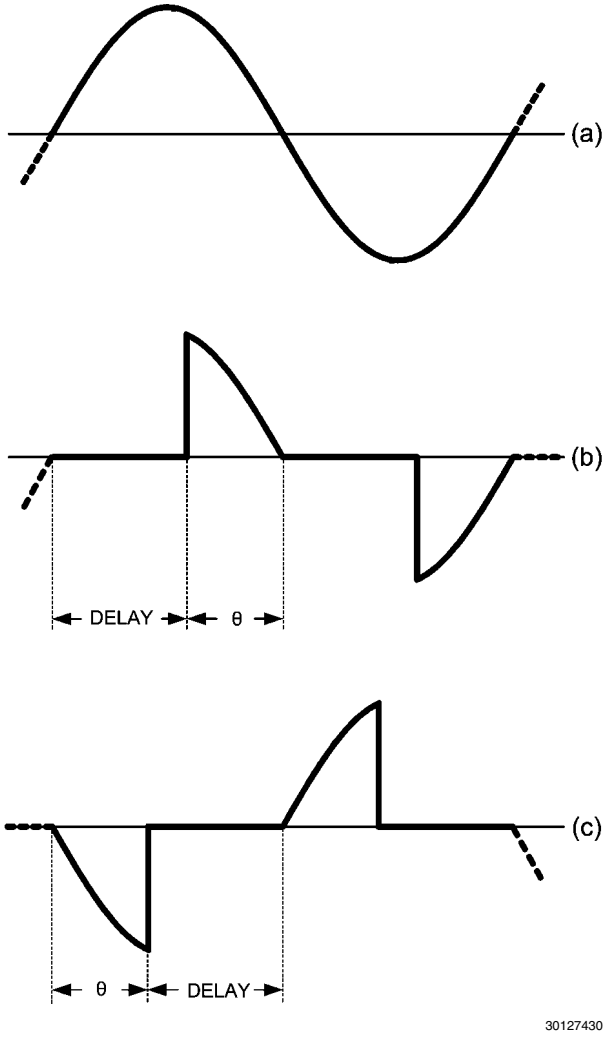


FIGURE 9. Phase Dimming Waveforms

PRECISION VOLTAGE REFERENCE

The LM3450 provides a 3V voltage reference (V_{REF}) for biasing the V_{ADJ} pin as well as any external circuitry. V_{REF} is regulated once V_{CC} exceeds 3V. There is a 2mA current limit for the reference. A 10nF ceramic bypass capacitor should be placed from V_{REF} to GND.

LOW POWER SHUTDOWN

The LM3450 can be placed into a low power shutdown by grounding the V_{ADJ} pin (any voltage below 75mV). During low power shutdown, the device will turn on the GATE for one cycle followed by a fixed off-time of 42µs and the cycle repeats. During shutdown, the DIM output will be high (zero light output) since the buffer rail at FLT1 will be at or near zero. This feature is designed to hold up the PFC output voltage while removing the load (turning the LEDs off).

THERMAL SHUTDOWN

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 160°C with a 20°C hysteresis. During thermal shutdown GATE is disabled.

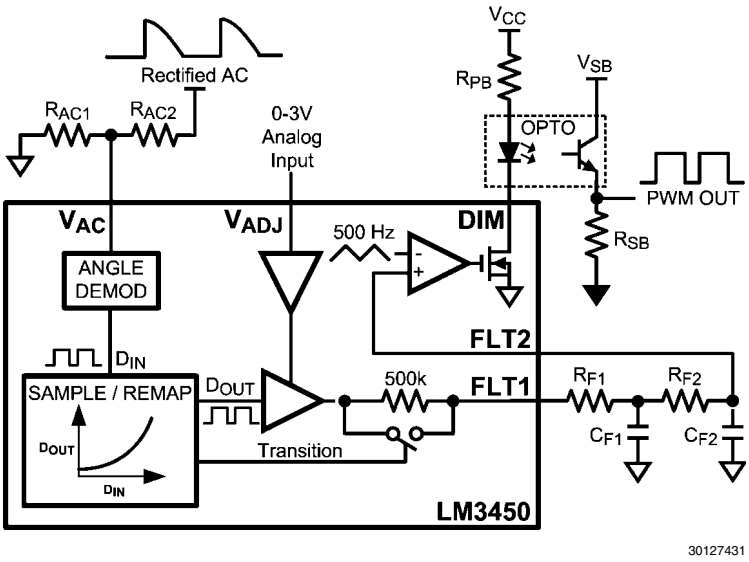


FIGURE 10. Dimming Decoder Circuit

PHASE DIMMING DECODER

The LM3450 uses the rectified AC line voltage to interpret the conduction angle. *Figure 10* shows the LM3450 decoder circuit with associated external circuitry. The rectified AC line voltage is scaled via a resistor divider (R_{AC1}, R_{AC2}) and connected to the V_{AC} pin. V_{AC} is compared to a 356mV reference to generate a twice line frequency PWM signal with corresponding duty cycle as shown in *Figure 11*.

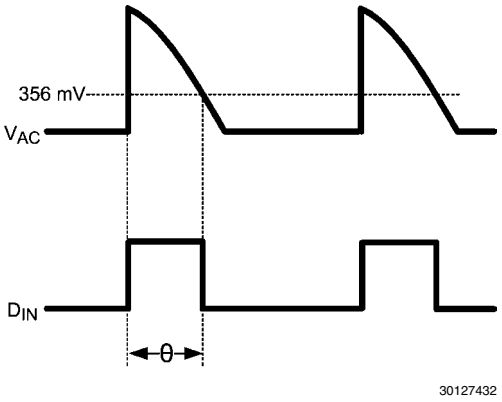


FIGURE 11. Phase Angle Demodulation

For best results, R_{AC1} and R_{AC2} are suggested to be sized so that the V_{AC} voltage crosses the 356mV threshold when the rectified AC line is as follows:

- 120V systems: 20V to 30V
- 230V systems: 40V to 60V

The demodulated duty cycle is sampled and logarithmically remapped to a 300Hz PWM signal improving the resolution of low dimming levels to the human eye. A minimum duty cycle limits the maximum achievable contrast ratio to approximately 70:1. The remapped PWM signal is buffered and output at FLT1 with amplitude equal to V_{ADJ} as shown in *Figure 12*.

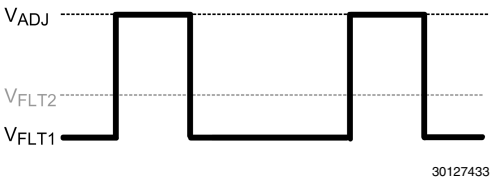


FIGURE 12. FLT1 to FLT2 Mapping

The FLT1 signal is routed through a 2 pole low pass filter (R_{F1}, C_{F1}, R_{F2}, C_{F2}), as shown in *Figure 10*, to remove the twice line frequency ripple. The resulting analog signal at FLT2 is compared to a 500Hz Triangle wave to create the inverted PWM signal at the DIM pin as shown in *Figure 13*:

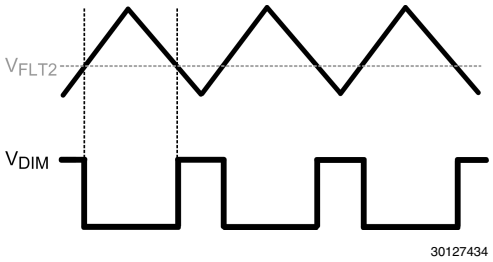


FIGURE 13. FLT2 to DIM Mapping

This PWM signal at the DIM pin can be used as the dim input to a secondary LED driver. DIM is an open drain output designed for isolated solutions. Optical isolation is used to transmit signals across the isolation boundary. With most optoisolators, the edge rate is dependent on the amount of drive current through the photodiode. The open-drain configuration allows the primary bias supply (V_{CC}) to provide the current as shown in *Figure 10*. The choice of resistor (R_{PB}) between V_{CC} and the photodiode anode will set the drive current. This enables the user to trade-off PWM accuracy with system efficiency.

The open drain configuration also ensures that the secondary has a resistor from the phototransistor's emitter to secondary ground (not from collector to secondary bias). During system turn-off, this prevents an undesired LED blink because the secondary stage LED driver is forced off.

A variable sample rate and dynamic filter ensure fast, smooth dimming transitions (movement of the dimmer) while maintaining robust flicker-free behavior when the dimmer is static. The sample rate depends on past and present angle information. The dynamic filter is a dual mode filter. During standby mode, when a transition has not been made and the dimmer is static, a 500kΩ series resistor is connected between the buffered output and FLT1 as shown in *Figure 10*.

The 500kΩ resistor is shorted when the LM3450 senses a large transition of the dimmer. This increases the filter speed while the dimmer is transitioning between levels to improve response time.

The FLT1 and FLT2 poles created by each RC pair (R_{F1} and C_{F1}, R_{F2} and C_{F2}) should be set as follows:

- C_{F1} and C_{F2} can be 1µF ceramic capacitors for all designs.
- R_{F1} and R_{F2} should be set between 15kΩ (~10Hz) and 75kΩ (~2Hz).

2 Hz poles provide a "smooth fade" while 10Hz poles create a "snappy" response.

These component values ensure that the static filter condition in standby mode has 1 pole approximately a decade lower than the nominal in order to provide good noise immunity to the system.

Since the buffered decoder output has amplitude equal to V_{ADJ} and the resulting PWM signal is filtered into an analog voltage at FLT2, the V_{ADJ} pin can be used to change the mapping (extend the usable range of some dimmers). The maximum LED current (DIM = 0) when V_{ADJ} = 3V corresponds to decoded angles of 70% or greater. Some dimmers have a maximum angle greater than this. If V_{ADJ} is reduced to 2.5V, the maximum LED current will correspond to an angle of 80% and at V_{ADJ} = 2V the maximum will occur at a decoded angle of 95%.

The V_{ADJ} pin can also be used to implement a standard analog adjust function. If the demodulated phase angle at V_{AC} is above 85%, then the fast filter is always enabled (500kΩ shorted) and the V_{ADJ} pin can solely be used to scale the DIM pin duty cycle. When V_{ADJ} is pulled below 75mV the part enters low power shutdown so the maximum attainable contrast ratio using V_{ADJ} only is approximately 40:1.

Both FLT1 and FLT2 have pull-down MosFETs that are turned on when V_{CC} UVLO falling threshold is triggered. This provides a quick discharge path for the capacitors and eliminates the possibility of an undesired light level at the next startup.

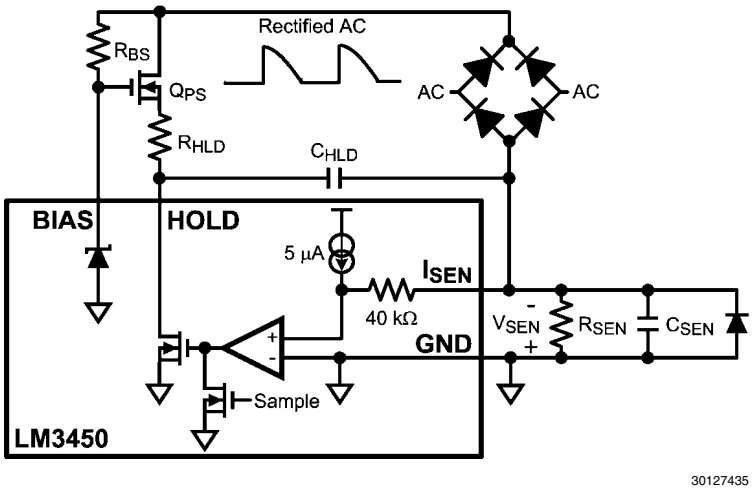


FIGURE 14. Dynamic Hold Circuit

DYNAMIC HOLD

A forward phase "triac" dimmer requires a minimum amount of current to be flowing through it during the entire conduction angle. This is referred to as hold current. If the minimum hold current requirement is not met, the triac will shut off (misfire). During normal operation, the converter will demand some amount of input current. However, at any point during the cycle, the input current can be low enough to cause a misfire.

During an LM3450 sampling period, the triac should not misfire or the decoded angle will be inaccurate as shown in *Figure 15*. Since the triac is asymmetrical phase-to-phase, misfires can occur at different points in the waveform. After the triac misfires, the voltage returns to zero exponentially. This can create a large difference between decoded angles which can be observed as a "fluttering" of the light.

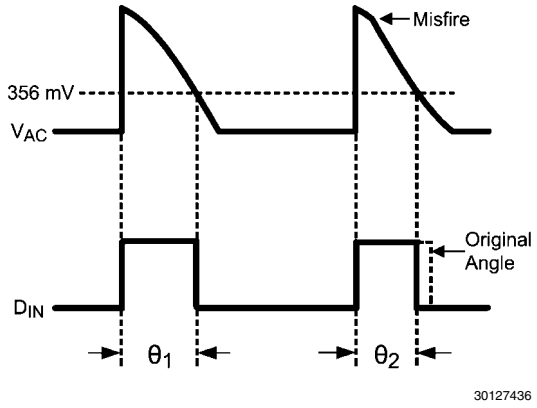


FIGURE 15. Forward Phase Waveform

To ensure the triac does not misfire during a sampling period and the angle is correctly decoded, a dynamic hold function is enabled. The input current is sensed with a resistor (R_{SEN}) from GND to I_{SEN} (the return of the full bridge rectifier). If the voltage across this resistor is less than 200mV, the device adds holding current via the HOLD circuitry to maintain 200mV across R_{SEN}.

The hold current is added by linearly adjusting the gate voltage of Q_{HLD} as shown in *Figure 14*. As the gate voltage of Q_{HLD} is increased, the HOLD pin voltage decreases, forcing a voltage across the resistance (R_{HLD}) from the source of Q_{PS} to HOLD. This extra current is drawn from the input through the triac, but is not processed by the converter. *Figure 16* shows a typical dynamic hold waveform where interval 1 is a non-sampled conduction angle, 2 is the firing angle, and 3 is a sampled conduction angle.

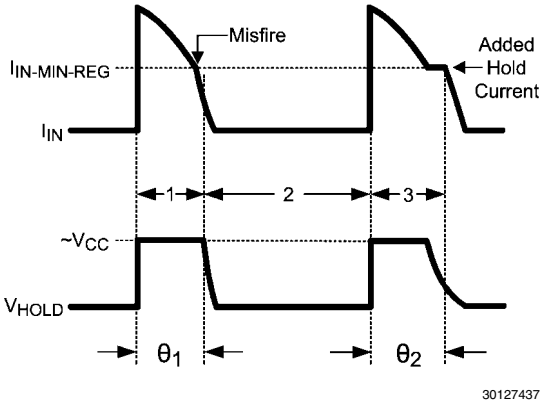


FIGURE 16. Dynamic Hold Waveform

The dynamic hold function is also necessary for reverse phase dimmers, but for a different reason. Reverse phase dimmers do not use triacs, therefore they do not require a minimum "holding" current. Instead, they need what is commonly called bleeder current. When a reverse phase dimmer turns off, the AC voltage is at a high value. There is an RC time constant associated with discharging the total effective input capacitance (EMI capacitors, PFC capacitor, damper capacitance). The decoder does not record the angle until the voltage reaches the 356mV threshold. This can cause the decoded angle to be much larger than it actually is and dependent on the RC time constant as shown in *Figure 17*.

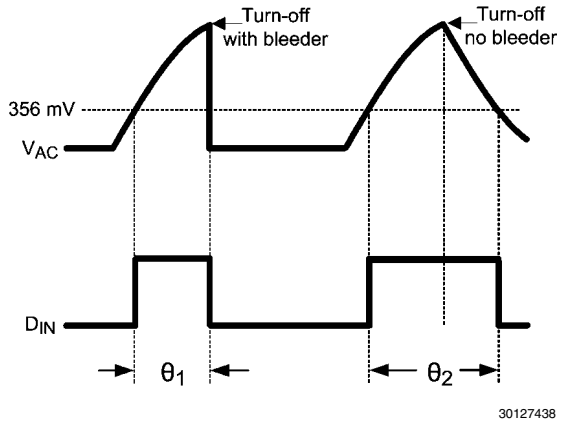


FIGURE 17. Reverse Phase Waveforms

The dynamic hold will quickly bleed off the excess charge in an attempt to regulate the voltage across RSEN. This will preserve the accuracy of the decoded phase angle.

During the conduction angle (θ), dynamic hold is enabled only during a sample period. However, during the firing angle (delay time), dynamic hold is always enabled to ensure the rectified line voltage does not begin to rise due to leakage currents through the phase dimmer.

The minimum regulated input current can be calculated:

$$I_{IN\text{-}MIN\text{-}REG} = \frac{200\ mV}{R_{SEN}}$$

The maximum possible additional holding current (which can occur when HOLD is still transitioning usually at the rising edge of the triac firing) can be approximated:

$$I_{HOLD\text{-}MAX} = \frac{V_{CC}}{R_{HLD} + 30\Omega}$$

It is recommended that the maximum hold current is set 10-15% higher than the minimum regulated input current.

A minimum of 0.1µF capacitance should be placed between I_{SEN} and HOLD to limit the bandwidth of the dynamic hold circuit to well below the switching frequency. However, if too large a capacitor is used, the bandwidth will be too low to respond to line transients. A maximum of 0.47µF should ensure good performance.

Finally, a small Schottky diode should be placed from GND to I_{SEN} to absorb the large current spikes associated with the triac firing edge. This diode should have a VF above 200mV at the worst-case operating temperature so that it won't interfere with dynamic hold regulation.

PRIMARY BIAS SUPPLY

The LM3450 requires a supply voltage at V_{CC}, not to exceed 25V. The device has V_{CC} under-voltage lockout (UVLO) with rising and falling thresholds of 12.9V and 7.9V respectively. A 24V Zener diode should be placed from the V_{CC} pin to GND to protect the device from substantial spikes that could cause damage.

Figure 18 shows how the LM3450 provides a quick way to generate the necessary primary bias supply at start-up. Since the AC line peak voltage is always higher than the rating of the controller, all designs require an N-channel MosFET (passFET). The passFET (Q_{PS}) is connected with its drain attached to the rectified AC. The gate of Q_{PS} is connected to the BIAS pin which has a stack of 2 Zener diodes internal to the device. These diodes are then biased from the rectified AC line through series resistance (R_{BS}). The source of Q_{PS} is held at a V_{GS} below the Zener voltage and current flows through Q_{PS} to charge up whatever capacitance is present. If the capacitance is large enough, the source voltage will remain relatively constant over the line cycle and this becomes the input bias supply at V_{CC}.

This bias circuit enables instant turn-on. However, once the circuit is operational it is desirable to bootstrap V_{CC} to an auxiliary winding of the inductor or transformer (also used for ZCD). The two bias paths are each connected to V_{CC} through a diode to ensure the higher of the two is providing V_{CC} current. This bootstrapping greatly improves efficiency when quick start-up is necessary.

To ensure that the auxiliary winding is powering V_{CC} at all times except start-up, the LM3450 has a dual BIAS mode. The BIAS voltage at startup is 20V through two Zener diodes. When the V_{CC} UVLO rising threshold is exceeded and the device turns on, the BIAS pin voltage is reduced to 14V (bottom 6V Zener is shorted). Once the V_{CC} UVLO falling threshold is reached again, the BIAS pin will return to 20V to attempt to restart the device.

It should be noted that the large hysteresis of V_{CC} UVLO and the dual BIAS mode allow for a large variation of the auxiliary bias circuitry easing the design of the magnetics.

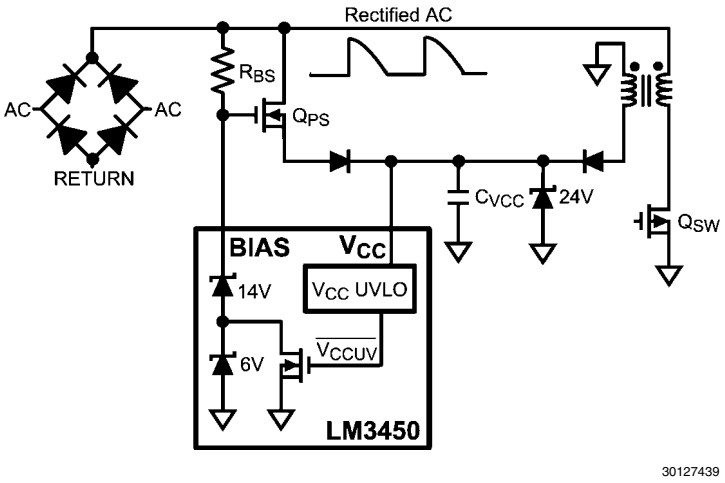
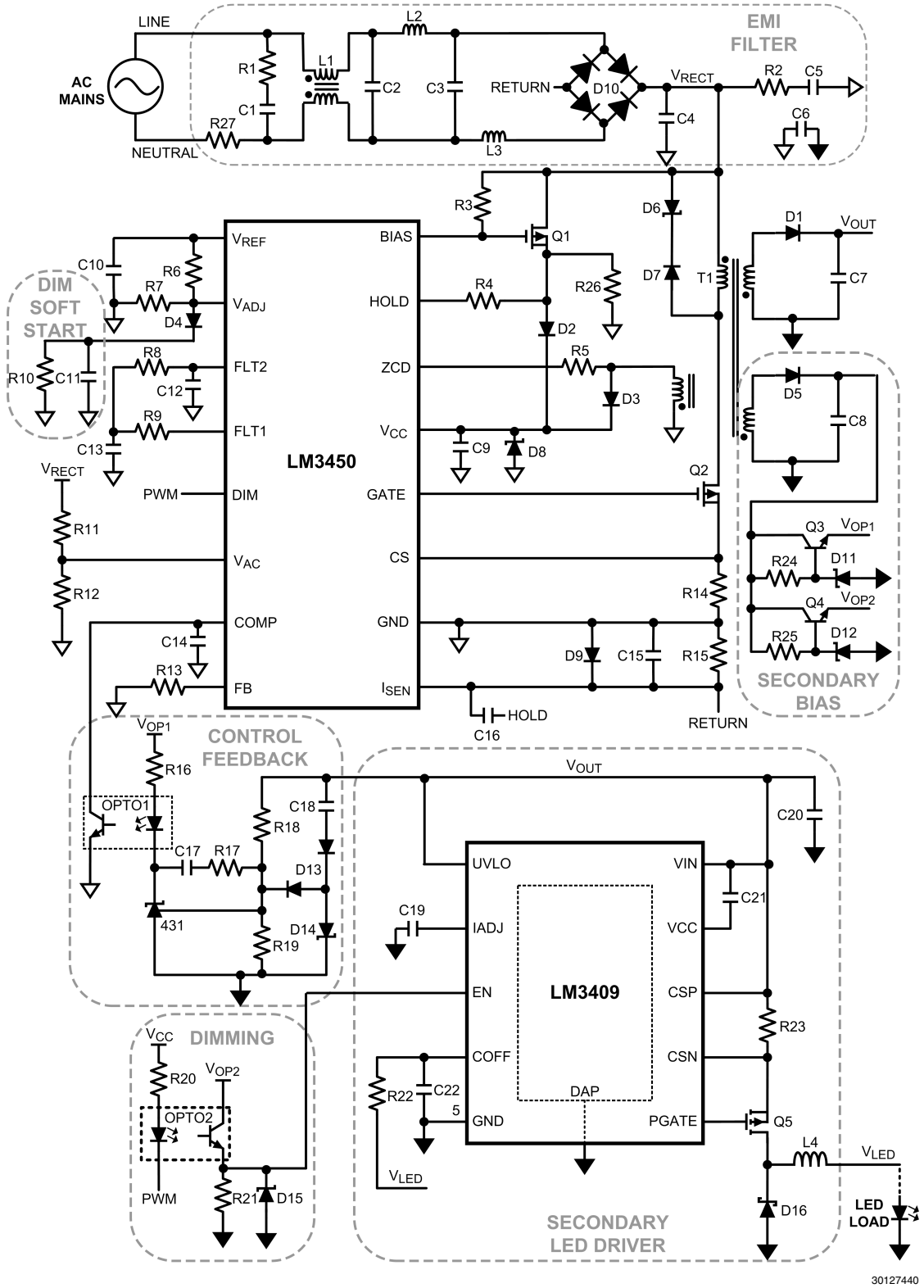


FIGURE 18. Primary Bias Circuitry

Applications Information

See AN-2098 for detailed design and application information.

TWO STAGE LED DRIVER – LM3450 Primary and LM3409 Secondary



15W TWO STAGE DESIGN SPECIFICATIONS

AC Input Voltage: $120V_{AC}$ nominal ($90V_{AC}$ - $135V_{AC}$)

Regulated Flyback Output Voltage: 50V

Regulated LED Current: 350mA

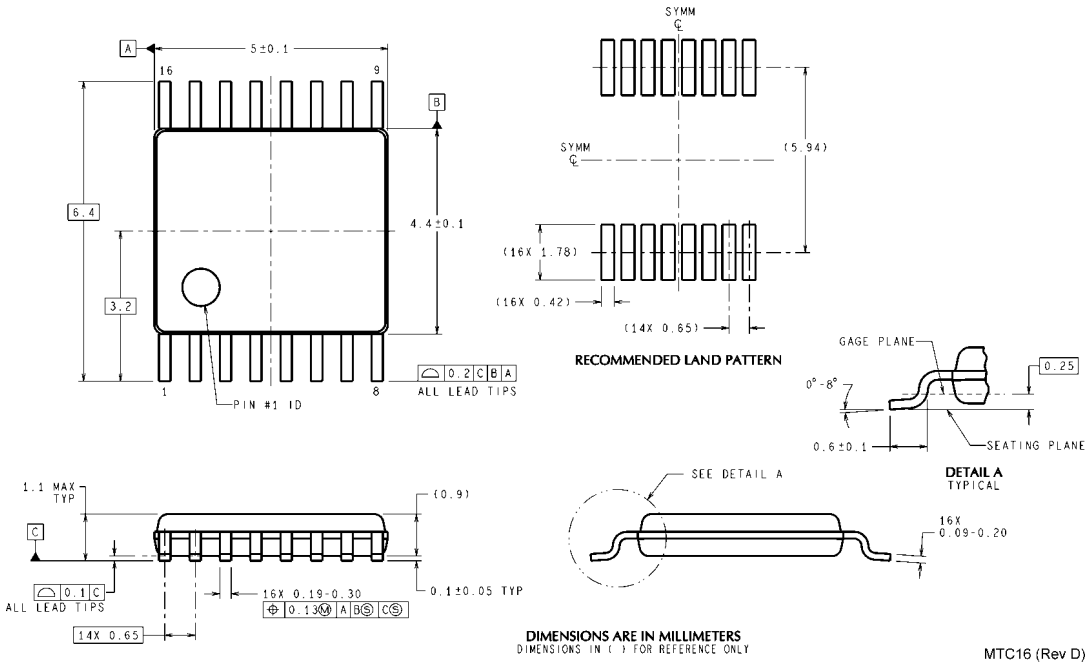
LED Stack Voltage Maximum: 45V

Bill of Materials

Reference Designator	Part Value	Manufacturer	Part Number
LM3450	IC PFC CONT 16-TSSOP	NSC	LM3450
LM3409	IC LED DRIVR 10-eMSOP	NSC	LM3409HVMY
LMV431	IC SHUNT REG SOT-23	NSC	LMV431AIM5
C1a, C1b, C5a, C5b	CAP CER 0.22µF 250V 1210	MURATA	GRM32DR72E224KW01L
C2, C3	CAP MPY 47nF 250VAC X1 RAD	EPCOS	B32912A3333M
C4	CAP MPY 0.1µF 400V RAD	EPCOS	B32612A4104J008
C6	CAP CER 4.7nF 500VAC Y1 RAD	EPCOS	VY1472M63Y5UQ63V0
C7a	CAP ELEC 470µF 63V RAD	NICHICON	UPW1J471MHD3
C7b, C8b, C9b, C15	CAP CER 1µF 50V 1206	TDK	C3216X7R1H105K
C8a, C9a	CAP ELEC 100µF 50V RAD	NICHICON	UHE1H101MPD
C10	CAP CER 10nF 25V 0603	MURATA	GRM188R71E103KA01D
C11	CAP CER 47µF 6.3V 0805	TAIYO YUDEN	JMK212BJ476MG-T
C12, C13 C14, C21	CAP CER 1µF 16V 0603	MURATA	GRM188R71C105KA12D
C16	CAP CER 0.22µF 16V 0603	TDK	C1608X7R1C224K
C17	CAP CER 10µF 16V 1206	MURATA	GRM31CR71C106KAC7L
C18	CAP CER 1µF 100V 1206	TDK	C3216X7R2A105M
C19	CAP CER 2.2µF 6.3V 0603	TDK	C1608X5R0J225M
C20	CAP CER 4.7µF 100V 2220	TDK	C5750X7R2A475K
C22	CAP CER 470pF 100V 0603	TDK	C1608C0G2A471J
D1, D2	DIODE ULTRAFAST 200V 1A SMA	FAIRCHILD	ES1D
D3, D5	DIODE ULTRAFAST 100V 0.2A SOT-23	FAIRCHILD	MMBD914
D4	DIODE SCHOTTKY 20V 0.5A SOT-23	NXP SEMI	PMEG2005ET,215
D6	DIODE TVS 150V 600W UNI SMB	LITTLEFUSE	SMBJ150A
D7	DIODE ULTRAFAST 600V 1A SMA	FAIRCHILD	ES1J
D8	DIODE ZENER 24V 3W SMA	MICRO-SEMI	SMAJ5934B-TP
D9	DIODE SCHOTTKY 20V 3A SMA	FAIRCHILD	ES2AA-13-F
D10	DIODE RECT 600V 0.5A Minidip	COMCHIP	HD06
D11, D12	DIODE ZENER 10V 500mW SOD-123	FAIRCHILD	MMSZ5240B
D13	DIODE ULTRAFAST 70V 0.2A SOT-23	FAIRCHILD	BAV99
D14	DIODE ZENER 3.3V 500mW SOD-123	ON-SEMI	MMSZ3V3T1G
D15	DIODE ZENER 1.8V 500MW SOD-123	ON-SEMI	MMSZ4678T1G
D16	DIODE SCHOTTKY 60V 2A SMB	ON-SEMI	SS26T3G
L1	IND LINE FILTER 6mH 0.3A 11M	PANASONIC	ELF-11M030E
L2, L3	IND SHIELD 1mH 0.46A SMT	COILCRAFT	MSS1038-105KL
L4	IND SHIELD 470µH 1.06A SMT	COILCRAFT	MSS1260-474KLB
Q1	MOSFET N-CH 800V 3A DPAK	ST MICRO	STD3NK80ZT4
Q2	MOSFET N-CH 600V 4.4A DPAK	INFINEON	IPD60R950C6
Q3, Q4	TRANS NPN 40V 0.6A SOT-23	FAIRCHILD	MMBT4401
Q5	MOSFET P-CH 70V 5.7A DPAK	ZETEX	ZXMP7A17K
R1	RES 330Ω 5% 1W 2512	VISHAY	CRCW2512330RJNEG
R2	RES 430Ω 5% 1W 2512	VISHAY	CRCW2512430RJNEG
R3	RES 953kΩ 1% 0.25W 1206	VISHAY	CRCW1206953KFKEA

R4	RES 100Ω 1%1W 2512	VISHAY	WSL2512100RFKEA
R5, R7, R10	RES 100kΩ 1% 0.1W 0603	VISHAY	CRCW0603100KFKEA
R6	RES 3.01kΩ 1% 0.1W 0603	VISHAY	CRCW06033K01FKEA
R8, R9	RES 75.0kΩ 1% 0.1W 0603	VISHAY	CRCW060375K0FKEA
R11	RES 1.00MΩ 1% 0.25W 1206	VISHAY	CRCW12061M00FKEA
R12	RES 14.0kΩ 1% 0.1W 0603	VISHAY	CRCW060314K0FKEA
R13	RES 5.11kΩ 1% 0.1W 0603	VISHAY	CRCW06035K11FKEA
R14a	RES 10Ω 1% 0.25W 1206	VISHAY	CRCW120610R0FKEA
R14b	RES 1.00Ω 1% 0.33W 1210	VISHAY	CRCW12101R00FNEA
R15a, R15b	RES 5.62Ω 1% 0.25W 1206	VISHAY	CRCW12065R62FNEA
R16	RES 2.00kΩ 1% 0.125W 0805	VISHAY	CRCW08052K00FKEA
R17	RES 20.0kΩ 1% 0.1W 0603	VISHAY	CRCW060320K0FKEA
R18	RES 105kΩ 1% 0.125W 0805	VISHAY	CRCW0805105KFKEA
R19	RES 2.67kΩ 1% 0.1W 0603	VISHAY	CRCW06032K67FKEA
R20	RES 6.04kΩ 1% 0.125W 0805	VISHAY	CRCW08056K04FKEA
R21	RES 10.0kΩ 1% 0.125W 0805	VISHAY	CRCW080510K0FKEA
R22	RES 80.6kΩ 1% 0.1W 0603	VISHAY	CRCW060380K6FKEA
R23	RES .62Ω 1% 0.5 2010 SMD	ROHM	MCR50JZHFLR620
R24, R25	RES 10kΩ 1% 0.1W 0603	VISHAY	CRCW060310K0FKEA
R26	RES 2.49kΩ 1% 0.125W 0805	VISHAY	CRCW08052K49FKEA
R27	RES 22Ω 10% 2W FILM	WELWYN	EMC2-22R0
OPTO1, OPTO2	OPTO-ISOLATOR SMD	LITE ON	CNY17F-3S
T1	XFORMER 120V 15W OUTPUT 50V	WURTH	750813550

Physical Dimensions inches (millimeters) unless otherwise noted



TSSOP-16 Pin Package (MTC)
For Ordering, Refer to Ordering Information Table
NS Package Number MTC16

Notes

Notes

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