# Dual USB Port Power Supply Controller

## ISL6185

The ISL6185 USB power controller family provides fully independent overcurrent (OC) fault protection for two or more USB ports.

This product family consists of sixteen individual functional product variants and three package options and is operation rated for a nominal +2.5V to +5V range and specified over the full commercial and industrial temperature ranges.

Each ISL6185 type incorporates in a single package two 71mΩ P-channel MOSFET power switches for power control and features internal current monitoring, accurate current limiting and current limited delay to turn-off for system supply protection along with control and communication I/O.

The ISL6185 family offers product variants with specified continuous output current levels of 0.6A, 1.1A, 1.5A or 1.8A, enable active high or low inputs and latch off or automatic retry after over current turn-off making these devices well suited for many low power applications.

This family of ICs is offered in an industry std. SOIC pinout and also in the 70% smaller 3x3 DFN packages providing similar or enhanced performance in the smallest possible package.

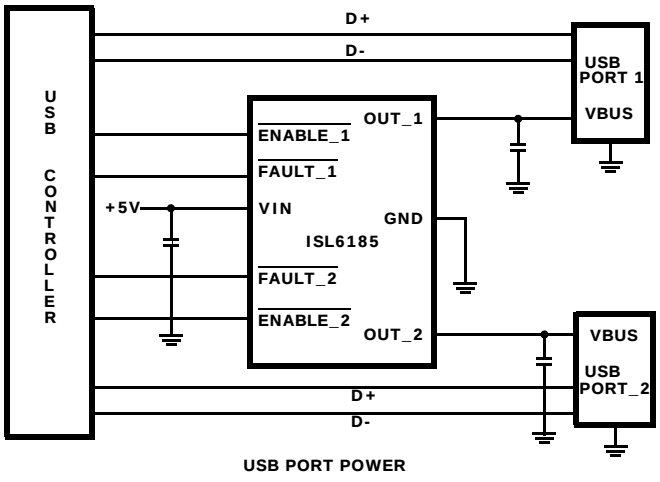
## Features

- 2.5V to 5V Operating Range
- 71mΩ Integrated Power P-channel MOSFET Switches
- Continuous Current Options for 0.6A, 1.1A, 1.5A and 1.8A
- Thermally insensitive 12ms of Current Limiting Prior to Turn-Off
- Output Discharges with Reverse Current Blocking when Disabled
- Latch-off or Auto Restart Options
- 1µA Off-State Supply Current.
- Enable Polarity Options
- Industry Std Pin for Pin SOIC and Smaller DFN Pkgs Available

## Applications

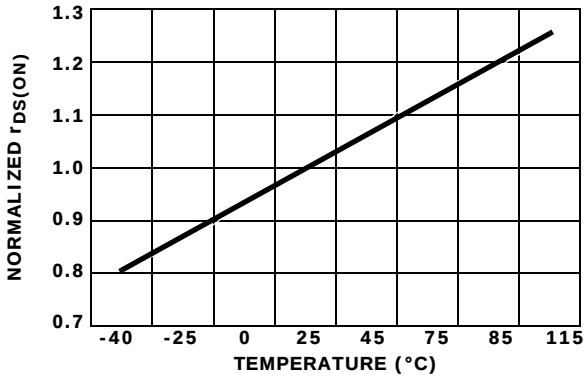
- USB 1, 2, 3 Port Power Management
- Low Power (18W) Electronic Circuit Limiting and Breaker

## Typical Application

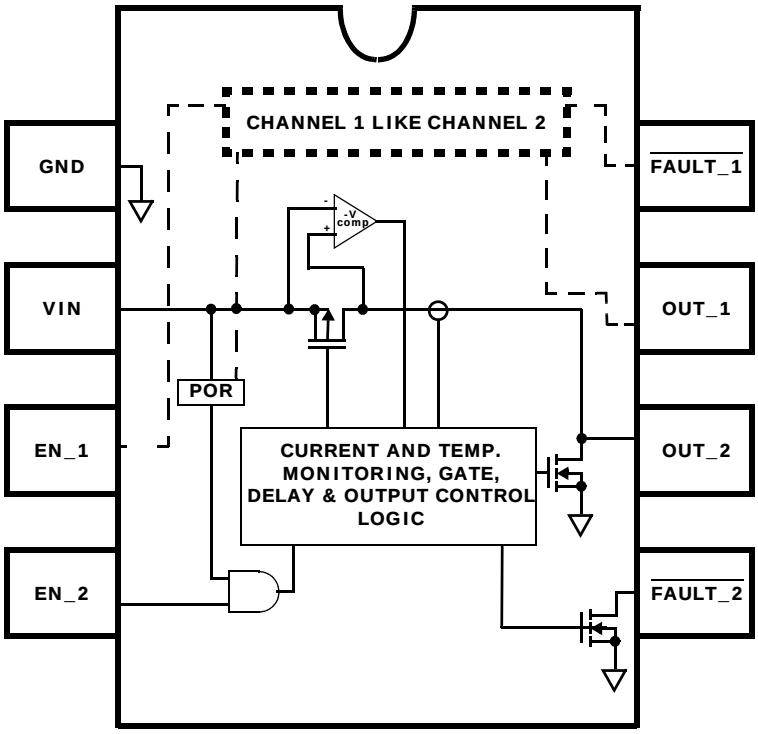



USB PORT POWER

## Normalized $r_{DS(ON)}$ Temperature Characteristic Curve



## Simplified Block Diagram




## Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | EN/$\overline{EN}$ INPUT | $V_{IN}$ = 5V MAXIMUM CONTINUOUS IOUT (A) | LATCH/AUTO RETRY | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|---|---|---|
| ISL61851ACBZ | 61851A CBZ | EN | 0.6 | LATCH | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851BCBZ | 61851B CBZ | EN | 0.6 | RETRY | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851CCBZ | 61851C CBZ | EN | 1.1 | LATCH | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851DCBZ | 61851D CBZ | EN | 1.1 | RETRY | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851ECBZ | 61851E CBZ | $\overline{EN}$ | 0.6 | LATCH | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851FCBZ | 61851F CBZ | $\overline{EN}$ | 0.6 | RETRY | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851GCBZ | 61851G CBZ | $\overline{EN}$ | 1.1 | LATCH | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851HCBZ | 61851H CBZ | $\overline{EN}$ | 1.1 | RETRY | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851ICBZ | 61851I CBZ | EN | 1.5 | LATCH | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851JCBZ | 61851J CBZ | EN | 1.5 | RETRY | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851KCBZ | 61851K CBZ | $\overline{EN}$ | 1.5 | LATCH | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61851LCBZ | 61851L CBZ | $\overline{EN}$ | 1.5 | RETRY | 0 to +70 | 8 Lead SOIC | M8.15 |
| ISL61852ACRZ | 52AC | EN | 0.6 | LATCH | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852BCRZ | 52BC | EN | 0.6 | RETRY | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852CCRZ | 52CC | EN | 1.1 | LATCH | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852DCRZ | 52DC | EN | 1.1 | RETRY | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852ECRZ | 52EC | $\overline{EN}$ | 0.6 | LATCH | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852FCRZ | 52FC | $\overline{EN}$ | 0.6 | RETRY | 0 to +70 | 8 Lead DFN | L8.3x3J |

## Ordering Information (Continued)

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | EN/$\overline{EN}$ INPUT | $V_{IN}$ = 5V MAXIMUM CONTINUOUS IOUT (A) | LATCH/AUTO RETRY | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|---|---|---|
| ISL61852GCRZ | 52GC | $\overline{EN}$ | 1.1 | LATCH | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852HCRZ | 52HC | $\overline{EN}$ | 1.1 | RETRY | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852ICRZ | 52IC | EN | 1.5 | LATCH | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852JCRZ | 52JC | EN | 1.5 | RETRY | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852KCRZ | 52KC | $\overline{EN}$ | 1.5 | LATCH | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61852LCRZ | 52LC | $\overline{EN}$ | 1.5 | RETRY | 0 to +70 | 8 Lead DFN | L8.3x3J |
| ISL61853ACRZ | 53AC | EN | 0.6 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853BCRZ | 53BC | EN | 0.6 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853CCRZ | 53CC | EN | 1.1 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853DCRZ | 53DC | EN | 1.1 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853ECRZ | 53EC | $\overline{EN}$ | 0.6 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853FCRZ | 53FC | $\overline{EN}$ | 0.6 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853GCRZ | 53GC | $\overline{EN}$ | 1.1 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853HCRZ | 53HC | $\overline{EN}$ | 1.1 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853ICRZ | 53IC | EN | 1.5 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853JCRZ | 53JC | EN | 1.5 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853KCRZ | 53KC | $\overline{EN}$ | 1.5 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853LCRZ | 53LC | $\overline{EN}$ | 1.5 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853MCRZ | 53MC | EN | 1.8 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853NCRZ | 53NC | EN | 1.8 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853OCRZ | 53OC | $\overline{EN}$ | 1.8 | LATCH | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61853PCRZ | 53PC | $\overline{EN}$ | 1.8 | RETRY | 0 to +70 | 10 Lead DFN | L10.3x3 |
| ISL61851AIBZ | 61851A IBZ | EN | 0.6 | LATCH | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851BIBZ | 61851B IBZ | EN | 0.6 | RETRY | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851CIBZ | 61851C IBZ | EN | 1.1 | LATCH | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851DIBZ | 61851D IBZ | EN | 1.1 | RETRY | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851EIBZ | 61851E IBZ | $\overline{EN}$ | 0.6 | LATCH | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851FIBZ | 61851F IBZ | $\overline{EN}$ | 0.6 | RETRY | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851GIBZ | 61851G IBZ | $\overline{EN}$ | 1.1 | LATCH | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851HIBZ | 61851H IBZ | $\overline{EN}$ | 1.1 | RETRY | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851IIBZ | 61851I IBZ | EN | 1.5 | LATCH | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851JIBZ | 61851J IBZ | EN | 1.5 | RETRY | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851KIBZ | 61851K IBZ | $\overline{EN}$ | 1.5 | LATCH | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61851LIBZ | 61851L IBZ | $\overline{EN}$ | 1.5 | RETRY | -40 to +85 | 8 Lead SOIC | M8.15 |
| ISL61852AIRZ | 52AI | EN | 0.6 | LATCH | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852BIRZ | 52BI | EN | 0.6 | RETRY | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852CIRZ | 52CI | EN | 1.1 | LATCH | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852DIRZ | 52DI | EN | 1.1 | RETRY | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852EIRZ | 52EI | $\overline{EN}$ | 0.6 | LATCH | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852FIRZ | 52FI | $\overline{EN}$ | 0.6 | RETRY | -40 to +85 | 8 Lead DFN | L8.3x3J |

## Ordering Information (Continued)

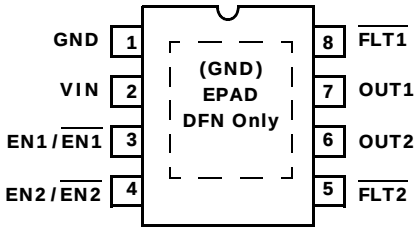
| PART NUMBER (Notes 1, 2, 3) | PART MARKING | EN/$\overline{EN}$ INPUT | $V_{IN}$ = 5V MAXIMUM CONTINUOUS IOUT (A) | LATCH/AUTO RETRY | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|---|---|---|
| ISL61852GIRZ | 52GI | $\overline{EN}$ | 1.1 | LATCH | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852HIRZ | 52HI | $\overline{EN}$ | 1.1 | RETRY | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852IIRZ | 52II | EN | 1.5 | LATCH | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852JIRZ | 52JI | EN | 1.5 | RETRY | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852KIRZ | 52KI | $\overline{EN}$ | 1.5 | LATCH | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61852LIRZ | 52LI | $\overline{EN}$ | 1.5 | RETRY | -40 to +85 | 8 Lead DFN | L8.3x3J |
| ISL61853AIRZ | 53AI | EN | 0.6 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853BIRZ | 53BI | EN | 0.6 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853CIRZ | 53CI | EN | 1.1 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853DIRZ | 53DI | EN | 1.1 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853EIRZ | 53EI | $\overline{EN}$ | 0.6 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853FIRZ | 53FI | $\overline{EN}$ | 0.6 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853GIRZ | 53GI | $\overline{EN}$ | 1.1 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853HIRZ | 53HI | $\overline{EN}$ | 1.1 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853IIRZ | 53II | EN | 1.5 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853JIRZ | 53JI | EN | 1.5 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853KIRZ | 53KI | $\overline{EN}$ | 1.5 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853LIRZ | 53LI | $\overline{EN}$ | 1.5 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853MIRZ | 53MI | EN | 1.8 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853NIRZ | 53NI | EN | 1.8 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853OIRZ | 53OI | $\overline{EN}$ | 1.8 | LATCH | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61853PIRZ | 53PI | $\overline{EN}$ | 1.8 | RETRY | -40 to +85 | 10 Lead DFN | L10.3x3 |
| ISL61851EVAL1Z | 8 Lead SOIC Evaluation Platform | | | | | | |
| ISL61852EVAL1Z | 8 Lead DFN Evaluation Platform | | | | | | |
| ISL61853EVAL1Z | 10 Lead DFN Evaluation Platform | | | | | | |

NOTES:

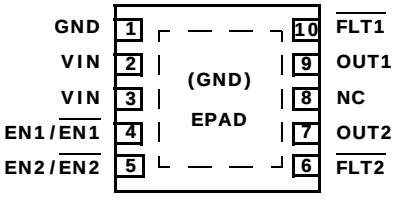
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6185. For more information on MSL please see techbrief TB363.

## Pin Configurations

**ISL6185**
**(8 LD SOIC/DFN)**
TOP VIEW




**ISL6185**
**(10 LD DFN)**
TOP VIEW




## Pin Descriptions

| PIN NUMBER | | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 8 Ld SOIC/DFN | 10 Ld DFN | | |
| 1 | 1 | GND | IC ground reference |
| 2 | 2, 3 | VIN | Chip bias, Controlled Voltage Input, Undervoltage Lock Out (UVLO). VIN provides chip bias voltage. At VIN < 1.7V chip functionality is disabled, $\overline{FLT}$ is active and floating and OUT is held low. Range 0V to 5.5V |
| 3, 4 | 4, 5 | EN1, $\overline{EN1}$/ EN2, $\overline{EN2}$ | Enable/Disable inputs, Active high (EN) and active low ($\overline{EN}$) options enable the power switch. These inputs have internal 1MΩ pull off resistors. Range 0V to VIN |
| 5, 8 | 6, 10 | $\overline{FLT2}$ $\overline{FLT1}$ | Overcurrent Fault Indicator. Overcurrent fault indicator. $\overline{FLT}$ floats and is disabled until VIN >$V_{UVLO}$. This output is pulled low after the current limit time-out period has expired. Fault is not signaled due to over-temperature shut down. Range 0V to VIN |
| 6, 7 | 7, 9 | OUT2, OUT1 | Controlled Supply Output. Upon an OC condition $I_{OUT}$ is current limited. Current limit response time is within 200µs. This output will remain in current limit for a nominal 12ms before being turned off either for the latch or auto retry versions. Range 0V to VIN |
| - | 8 | NC | This pin is not electrically connected internally |
| PD (DFN only) | PD | EPAD | Thermal Dissipation Exposed PAD Range: Connect to GND |

## Absolute Maximum Ratings

Supply Voltage (VIN to GND, Note 7) . . . . . .6.5V
EN, FAULT . . . . . VIN
OUT . . . . . GND - 0.3V to VIN 0.3V
Output Current . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3kV
Machine Model (Per MIL-STD-883 Method 3015.7). . . 300V
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . 100mA

## Thermal Information

| Thermal Resistance (Typical, Note 4) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 8 Lead SOIC Package (Note 4) . . . | 120 | N/A |
| 8 Lead 3x3 DFN Package (Notes 5, 6) | 48 | 6 |
| 10 Lead 3x3 DFN Package (Notes 5, 6) | 53 | 6 |

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Operating Conditions

Commercial Temperature Range. . . . . 0°C to +70°C
Industrial Temperature Range . . . . . -40°C to +85°C
Supply Voltage Range (Typical) . . . . . 2.3V to 5.5V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.
7. All voltages are relative to GND, unless otherwise specified.

## Electrical Specifications

$V_{IN}$ = 5V, $T_A$ = $T_J$, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C.**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 8) | TYP | MAX (Note 8) | UNITS |
|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | |
| $r_{DS(ON)\_50}$ | ON-Resistance at 5.0V (Pulse Tested) | $V_{IN}$ = 5V, $I_{OUT}$ = 0.1A, $T_A$ = $T_J$ = +25°C | - | 71 | 87 | mΩ |
| | | $T_A$ = $T_J$ = +85°C | - | | **110** | mΩ |
| $r_{DS(ON)\_33}$ | ON-Resistance at 3.3V (Pulse Tested) | $V_{IN}$ = 3.3V, $I_{OUT}$ = 0.1A, $T_A$ = $T_J$ = +25°C | - | 90 | 105 | mΩ |
| | | $T_A$ = $T_J$ = +85°C | - | | **130** | mΩ |
| $r_{DS(ON)\_25}$ | On Resistance at 2.5V (Pulse Tested) | $V_{IN}$ = 2.5V, $I_{OUT}$ = 0.1A, $T_A$ = $T_J$ = +25°C | - | 114 | 127 | mΩ |
| | | $T_A$ = $T_J$ = +85°C | - | | **150** | mΩ |
| $V_{OUT\_DIS}$ | Disabled Output Voltage | $V_{IN}$ = 5V, Switch Disabled, 50µA Load | - | 50 | **70** | mV |
| $R_{OUT\_PU}$ | Output Pull-Down Resistor | $V_{IN}$ = 5V, Switch Disabled | **8** | 9.6 | **12** | kΩ |
| $t_R$ | $V_{OUT}$ Rise Time | $R_L$ = 10Ω, $C_L$=10µF, 10% to 90% | - | 100 | - | µs |
| $t_F$ | Slow $V_{OUT}$ Turn-off Fall Time | $R_L$ = 10Ω, $C_L$=10µF, 90% to 10% | - | 200 | - | µs |
| $t_{F\_fast}$ | Fast $V_{OUT}$ Turn-off Fall Time | $R_L$ = 1Ω, $C_L$=10µF, 80% to 20% | - | 23 | - | µs |
| **CURRENT CONTROL** | | | | | | |
| $I_{OUT\_CONT\_5}$ | Maximum Continuous Current, $V_{IN}$ = 5V. Guaranteed by Itrip minimum specification. | ISL6185xA,B,E,F | - | | **0.6** | A |
| $I_{OUT\_CONT\_5}$ | | ISL6185xC,D,G,H | - | | **1.1** | A |
| $I_{OUT\_CONT\_5}$ | | ISL6185xI,J,K,L | - | | **1.5** | A |
| $I_{OUT\_CONT\_5}$ | | ISL61853M,N,O,P (10 Ld DFN) | - | | **1.8** | A |
| $I_{OUT\_CONT\_3}$ | Maximum Continuous Current, $V_{IN}$ = 3.3V. Guaranteed by Itrip minimum specification. | ISL6185xA,B,E,F | - | | **0.6** | A |
| $I_{OUT\_CONT\_3}$ | | ISL6185xC,D,G,H | - | | **0.9** | A |
| $I_{OUT\_CONT\_3}$ | | ISL61851I,J,K,L (SOIC) | - | | **1.3** | A |
| $I_{OUT\_CONT\_3}$ | | ISL61852, ISL61853 (DFN) | - | | **1.5** | A |

**Electrical Specifications** $V_{IN}$ = 5V, $T_A$ = $T_J$, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C. (Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 8) | TYP | MAX (Note 8) | UNITS |
|---|---|---|---|---|---|---|
| $I_{OUT\_CONT\_2}$ | Maximum Continuous Current, $V_{IN}$ = 2.5V | ISL6185xA,B,E,F | - | 0.6 | - | A |
| $I_{OUT\_CONT\_2}$ | | ISL61851C,D,G,H (SOIC) | - | 0.9 | - | A |
| $I_{OUT\_CONT\_2}$ | | ISL61852, ISL61853 C,D,G,H (DFN) | - | 1 | - | A |
| $I_{OUT\_CONT\_2}$ | | ISL61853I,J,K,L (10 Ld DFN) | - | 1 | - | A |
| $I_{OUT\_CONT\_2}$ | | ISL61853M,N,O,P (10 Ld DFN) | - | 1 | - | A |
| $I_{TRIP\_5}$ | Trip Current, $V_{IN}$ = 5V | ISL6185xA,B,E,F | **0.70** | 1.02 | **1.52** | A |
| $I_{TRIP\_5}$ | | ISL6185xC,D,G,H | **1.15** | 1.45 | **1.95** | A |
| $I_{TRIP\_5}$ | | ISL61853I,J,K,L | **1.55** | 1.82 | **2.25** | A |
| $I_{TRIP\_5}$ | | ISL61853M.N,O,P | **1.85** | 1.99 | **2.15** | A |
| $I_{TRIP\_3}$ | Trip Current, $V_{IN}$ = 3.3V | ISL6185xA,B,E,F | **0.65** | 0.86 | **1.20** | A |
| $I_{TRIP\_3}$ | | ISL6185xC,D,G,H | **0.95** | 1.25 | **1.60** | A |
| $I_{TRIP\_3}$ | | ISL61853I,J,K,L | **1.35** | 1.60 | **1.85** | A |
| $I_{TRIP\_3}$ | | ISL61853M.N,O,P | **1.55** | 1.89 | **2.25** | A |
| $I_{TRIP\_2}$ | Trip Current, $V_{IN}$ = 2.5V | ISL6185xA,B,E,F | **-** | 0.65 | - | A |
| $I_{TRIP\_2}$ | | ISL6185xC,D,G,H | **-** | 1 | - | A |
| $I_{TRIP\_2}$ | | ISL61853I,J,K,L | **-** | 1.2 | - | A |
| $I_{TRIP\_2}$ | | ISL61853M.N,O,P | **-** | 1.6 | **-** | A |
| $I_{LIM\_5}$ | Current Limit, $V_{IN}$ = 5V | ISL6185xA,B,E,F, $V_{IN}$ - $V_{OUT}$ = 1V | **0.50** | 0.65 | **0.78** | A |
| $I_{LIM\_5}$ | | ISL6185xC,D,G,H, $V_{IN}$ - $V_{OUT}$ = 1V | **0.98** | 1.14 | **1.28** | A |
| $I_{LIM\_5}$ | | ISL61853I,J,K,L, $V_{IN}$ - $V_{OUT}$ = 1V | **1.30** | 1.55 | **1.72** | A |
| $I_{LIM\_5}$ | | ISL61853M,N,O,P, $V_{IN}$ - $V_{OUT}$ = 1V | **1.52** | 1.83 | **2.20** | A |
| $I_{LIM\_3}$ | Current Limit, $V_{IN}$ = 3.3V | ISL6185xA,B,E,F, $V_{IN}$ - $V_{OUT}$ = 1V | **0.45** | 0.63 | **0.75** | A |
| $I_{LIM\_3}$ | | ISL6185xC,D,G,H, $V_{IN}$ - $V_{OUT}$ = 1V | **0.90** | 1.10 | **1.26** | A |
| $I_{LIM\_3}$ | | ISL61853I,J,K,L, $V_{IN}$ - $V_{OUT}$ = 1V | **1.25** | 1.50 | **1.68** | A |
| $I_{LIM\_3}$ | | ISL61853M,N,O,P, $V_{IN}$ - $V_{OUT}$ = 1V | **1.48** | 1.78 | **2.05** | A |
| $I_{LIM\_2}$ | Current Limit, $V_{IN}$ = 2.5V | ISL6185xA,B,E,F, $V_{IN}$ - $V_{OUT}$ = 1V | **0.47** | 0.61 | **0.74** | A |
| $I_{LIM\_2}$ | | ISL6185xC,D,G,H, $V_{IN}$ - $V_{OUT}$ = 1V | **0.90** | 1.05 | **1.17** | A |
| $I_{LIM\_2}$ | | ISL61853I,J,K,L, $V_{IN}$ - $V_{OUT}$ = 1V | **1.15** | 1.37 | **1.58** | A |
| $I_{LIM\_2}$ | | ISL61853M,N,O,P, $V_{IN}$ - $V_{OUT}$ = 1V | **1.3** | 1.63 | **1.90** | A |
| $I_{sc\_5}$ | Short Circuit Current, $V_{IN}$ = 5V | ISL6185xA,B,E,F, $V_{OUT}$ = 0V | **0.60** | 0.80 | **1.00** | A |
| $I_{sc\_5}$ | | ISL6185xC,D,G,H, $V_{OUT}$ = 0V | **1.00** | 1.27 | **1.55** | A |
| $I_{sc\_5}$ | | ISL61853I,J,K,L, $V_{OUT}$ = 0V | **1.15** | 1.61 | **1.85** | A |
| $I_{sc\_5}$ | | ISL61853M,N,O,P, $V_{OUT}$ = 0V | **1.20** | 1.70 | **2.5** | A |
| $I_{sc\_3}$ | Short Circuit Current, $V_{IN}$ = 3.3V | ISL6185XA,B,E,F, $V_{OUT}$ = 0V | **0.35** | 0.48 | **0.60** | A |
| $I_{sc\_3}$ | | ISL6185XC,D,G,H, $V_{OUT}$ = 0V | **0.65** | 0.80 | **0.95** | A |
| $I_{sc\_3}$ | | ISL61853I,J,K,L, $V_{OUT}$ = 0V | **0.70** | 1.06 | **1.25** | A |
| $I_{sc\_3}$ | | ISL61853M,N,O,P, $V_{OUT}$ = 0V | **0.90** | 1.24 | **1.50** | A |
| $I_{sc\_2}$ | Short Circuit Current, $V_{IN}$ = 2.5V | ISL6185xA,B,E,F, $V_{OUT}$ = 0V | **-** | 0.61 | | A |
| $I_{sc\_2}$ | | ISL6185xC,D,G,H, $V_{OUT}$ = 0V | **-** | 1.06 | **-** | A |
| $I_{sc\_2}$ | | ISL61853I,J,K,L, $V_{OUT}$ = 0V | **-** | 1.30 | **-** | A |
| $I_{sc\_2}$ | | ISL61853M,N,O,P, $V_{OUT}$ = 0V | **-** | 1.39 | **-** | A |

**Electrical Specifications** $V_{IN}$ = 5V, $T_A$ = $T_J$, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, 0°C to +75°C or -40°C to +85°C. (Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 8) | TYP | MAX (Note 8) | UNITS |
|---|---|---|---|---|---|---|
| $tsett_{Ilim}$ | OC to Limit Settling Time | $V_{IN}/R_L$ = $2I_{LIM}$, $C_L$ = 10µF to within 10% of $I_{LIM}$ | - | 200 | - | µs |
| $tsett_{Ilim\_sev}$ | Severe OC to Limit Settling Time | $V_{IN}/R_L$ = $4I_{LIM}$, $C_L$ = 10µF to within 10% of $I_{LIM}$ | - | 30 | - | µs |
| $t_{CL}$ | Current Limit Duration | $I_{OUT}$ = $I_{LIM}$ | **9.2** | 12 | **15** | ms |
| $t_{RTY}$ | Automatic Retry Period | | **0.80** | 1 | **1.35** | s |
| **I/O PARAMETERS** | | | | | | |
| Vfault_lo | Fault Output Voltage | Fault $I_{OUT}$ = 10mA | - | - | **0.4** | V |
| Ifault | Fault Leakage | | - | 5 | **-** | µA |
| Venr_5 | ENABLE Rising Threshold | $V_{IN}$ = 5V | **1.5** | 1.8 | **2** | V |
| Hys_Venr_5 | ENABLE Rising Threshold Hysteresis | $V_{IN}$ = 5V | **80** | 140 | **175** | mV |
| Venr_3 | ENABLE Rising Threshold | $V_{IN}$ = 3.3V | **1.0** | 1.3 | **1.6** | V |
| Hys_Venr_3 | ENABLE Rising Threshold Hysteresis | $V_{IN}$ = 3.3V | **58** | 80 | **120** | mV |
| Venr_2 | ENABLE Rising Threshold | $V_{IN}$ = 2.5V | **0.95** | 1.1 | **1.3** | V |
| Hys_Venr_2 | ENABLE Rising Threshold Hysteresis | $V_{IN}$ = 2.5V | **30** | 70 | **110** | mV |
| Ren_h | ENABLE Pull-Down Resistor | Enable asserted high options | **0.6** | 1 | **1.55** | MΩ |
| Ren_l | $\overline{\text{ENABLE}}$ Pull-Up Resistor | Enable asserted low options | **0.6** | 1 | **1.55** | MΩ |
| $t_{ON}$ | Enable to Output Turn-on Time | $R_L$ = 10Ω, $C_L$ = 10µF, Enable 50% to Output 90% | - | 0.1 | - | ms |
| $t_{OFF}$ | Enable to Output Turn-off Time | $R_L$ = 10Ω, $C_L$ = 10µF, Enable 50% to Output 10% | - | 0.25 | - | ms |
| **BIAS PARAMETERS** | | | | | | |
| $I_{VDD}$ | Enabled $V_{IN}$ Current | Switches Closed, OUTPUT = OPEN | | 50 | **75** | µA |
| $I_{VDD}$ | Disabled $V_{IN}$ Current | Switches Open, OUTPUT = OPEN | - | 2 | **5** | µA |
| $V_{UVLO}$ | Rising POR Threshold | $V_{IN}$ Rising to functional operation | **1.7** | 2.1 | **2.3** | V |
| $UV_{HYS}$ | POR Hysteresis | | **200** | 360 | **580** | mV |
| $I_{VR}$ | Reverse Blocking Leakage Current | $V_{IN}$ = 0V, $V_{OUT}$ = 5V | - | | **2** | µA |
| Temp_dis | Over-Temperature Disable | | - | 150 | - | °C |
| Temp_hys | Over-Temperature Hysteresis | | - | 20 | - | °C |

NOTE:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

# Introduction

The ISL6185 is a dual channel fully independent overcurrent (OC) fault protection IC for the +2.5V to +5V environment. Each ISL6185 incorporates in a single package two 85mΩ P-channel MOSFET power switches for power control. Independent enabling inputs and fault reporting outputs compatible with 2.5V to 5V logic allows for external control and reporting. This device features integrated power switches with current monitoring, accurate current limiting, reverse bias protection and current limited timed delay to turn-off for system reliability. See Figures 11 through 26 for typical operational waveforms including both under and overcurrent situations.

The ISL6185 offers current sense and limiting with $V_{IN}$ = 5V guaranteed continuous current product variants of 0.6A, 1.1A, 1.5A and 1.8A making these devices well suited for a myriad of USB and other low power (9W max) port power management applications and configurations.

The ISL6185 also provides a thermally insensitive timed OC turn-off and fault notification, isolating and protecting the voltage bus in the event of a peripheral OC event or short circuit event independent of the adjoining switch's electrical or the ambient thermal condition.

The ISL6185 undervoltage lockout feature prevents turn-on of the outputs unless the correct ENABLE state and $V_{IN} > V_{UVLO}$ are present. During initial turn-on the ISL6185 prevents fault reporting by blanking the fault signal.

During operation, once an OC condition is detected the output is current limited for $t_{CL}$ to allow transient OC conditions to pass. If still in current limit after the current limit period has elapsed, the output is then turned off and the fault is reported by pulling the corresponding $\overline{\text{FAULT}}$ output low. On the latch off options, after turn-off both the output and the $\overline{\text{FAULT}}$ signal are latched low until reset by the enable signal being de-asserted or a POR occurs at which time the $\overline{\text{FAULT}}$ signal will clear and the switch is ready to be turned back on. On the auto restart options the ISL6185 will attempt to periodically turn-on the output as long as the enable is asserted.

When disabled the ISL6185 has a low quiescent supply current and output to input reverse current flow blocking capability.

The ISL6185 family is provided with enable polarity options and an industry standard 8 lead SOIC pinout along with two versions in the 70% smaller 3x3 DFN. The 8 Ld DFN package offers the same performance as the 8 Ld SOIC whereas the 10 Ld DFN offers higher current capability in the smallest possible package because of lower package electrical and thermal resistance.

# Functional Description

## Power On Preset (POR)

The ISL6185 POR feature inhibits device functionality when VIN $< V_{UVLO}$.

## Reverse Polarity Protection

In any event where the power switch is disabled and $V_{OUT} > V_{IN}$ there will be no output to input current flow nor will the output voltage appear on the input.

## Soft-Start

Upon enable, the switch passes a constant current to the load. The voltage on the VOUT pin will ramp up according the equation: $I_{LIM}/C_{OUT}$ (V/s). Resistive or active load will slow the $V_{OUT}$ ramp up toward the top of its curve.

## Fault Blanking On Start-Up

During initial turn-on, the ISL6185 prevents nuisance faults being reported to the system controller by blanking the fault signal until the internal FET is fully enhanced.

## Current Trip and Limiting Levels

The ISL6185 provides integrated current sensing in the MOSFET that allows for rapid control of OC events. Once an OC condition is detected the ISL6185 goes into its current limiting (CL) control mode. The ISL6185 is variant specified to allow a continuous current ($I_{CONT}$) operation of 0.6A, 1.1A, 1.5A or 1.8A. As the current increases past its continuous current rating it will reach a level that causes the device to enter its current limit mode, that is the current trip level. The current trip level is in all cases adequately above the $I_{CONT}$ rating as to not cause unintended false faults. The current limit is specified at $V_{OUT} = V_{IN}$ - 1V to test a known representative condition and is featured at a nominal value slightly higher than the continuous current rating. The speed of this current limiting control is inversely related to the magnitude of the OC fault. Thus a hard overcurrent is more quickly pulled to its limiting value than a marginal OC condition.

## Over-Temperature Shutdown

Although the ISL6185 has an over-temperature shutdown and lockout feature, because of the 12ms timed shutdown the thermal shutdown is likely only to be invoked in extremely high ambient temperatures.

The over- temperature protection invokes and disables the switch turn-on operation once the die temperature is ~+140°C, it will turn off an already on switch at ~+150°C and releases the part to operation once the die temperature falls to ~+120°C.

### Turn-off Time Delay

During operation, once an OC condition is detected the output is current limited for ~12ms to allow transient OC conditions to pass. If still in current limit and after the current limit period has elapsed, the output is then turned off and the fault is reported by pulling the corresponding $\overline{\text{FAULT}}$ low. The internal 12ms timer starts upon current limiting and is independent of ambient or IC thermal conditions providing more consistent operation over the entire temp range.

### Latchoff Restart / Auto-Restart Start

After turn-off, with the latch off options both the output and the $\overline{\text{FAULT}}$ signal are latched low until reset by the enable signal being de-asserted at which time the $\overline{\text{FAULT}}$ signal will clear and the IC is ready for enable to assert. On the auto restart options the ISL6185 will attempt to periodically turn-on the output at approximately 1s intervals as long as the enable is asserted. If the OC condition remains indefinitely so will the fault indication and the restart attempts until such time that the thermal protection feature is invoked increasing the restart period.

### Active Output Pull-down

Another ISL6185 feature is the 10kΩ active pull-down on the outputs to <60mV above GND when the device is disabled ensuring discharge of the load.

## Typical Performance Curves

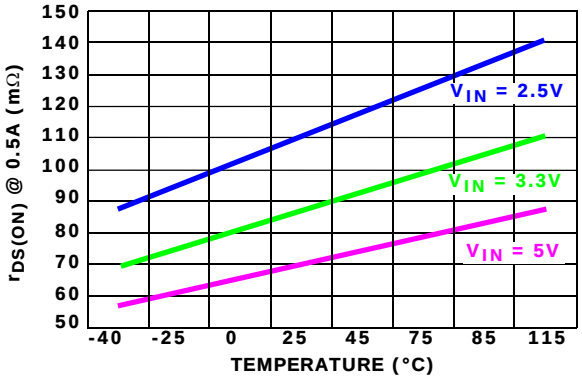



FIGURE 1. SWITCH ON-RESISTANCE AT 0.5A

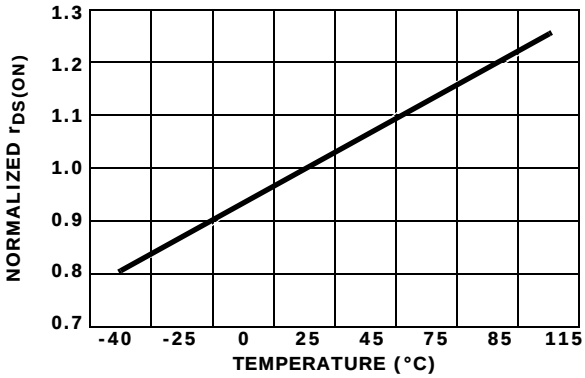



FIGURE 2. NORMALIZED SWITCH RESISTANCE

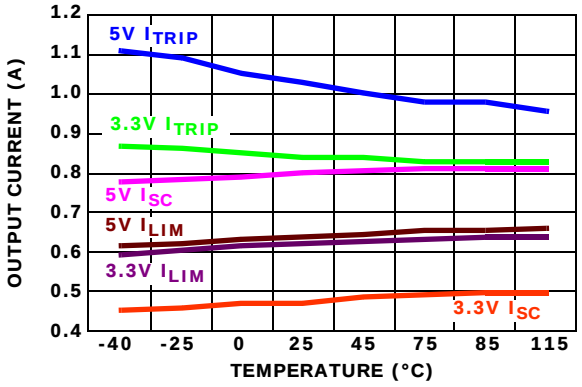



FIGURE 3. 0.6A CONTINUOUS CURRENT CHARACTERISTICS

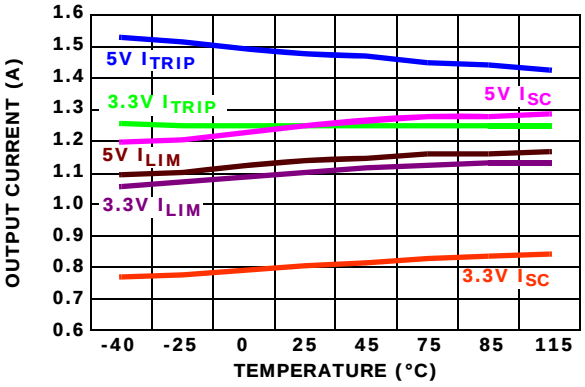



FIGURE 4. 1.1A CONTINUOUS CURRENT CHARACTERISTICS

## Typical Performance Curves (Continued)

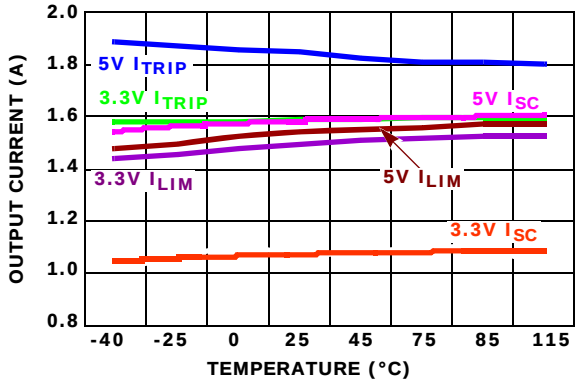



FIGURE 5. 1.5A CONTINUOUS CURRENT CHARACTERISTICS

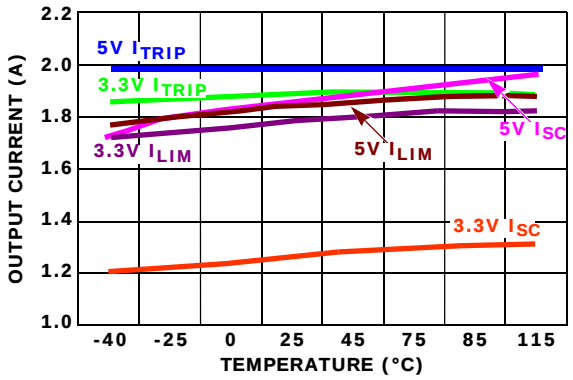



FIGURE 6. 1.8A CONTINUOUS CURRENT CHARACTERISTICS

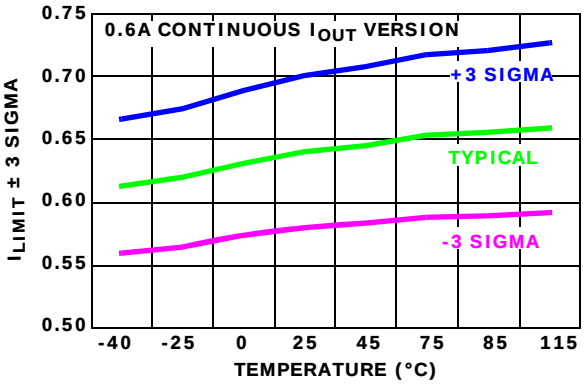



FIGURE 7. LIMITING CURRENT ±3 SIGMA, $V_{IN}$ = 5V

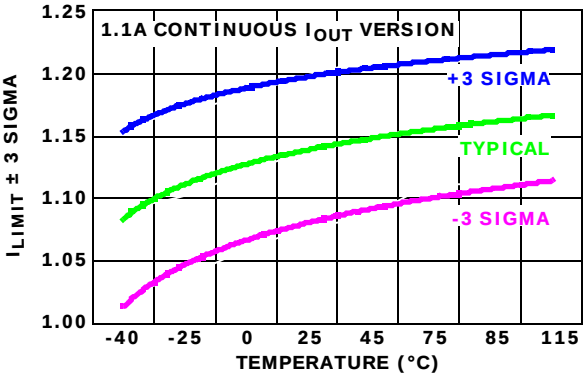



FIGURE 8. LIMITING CURRENT ±3 SIGMA, $V_{IN}$ = 5V

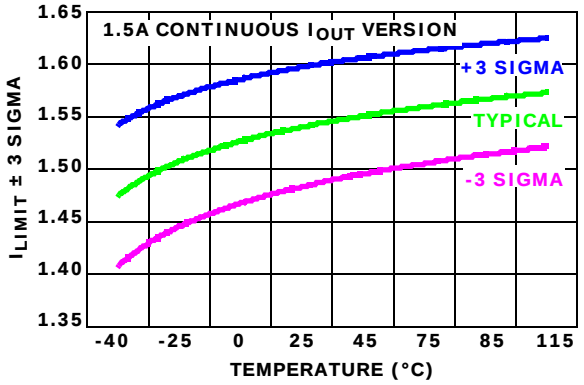



FIGURE 9. LIMITING CURRENT ±3 SIGMA, $V_{IN}$ = 5V

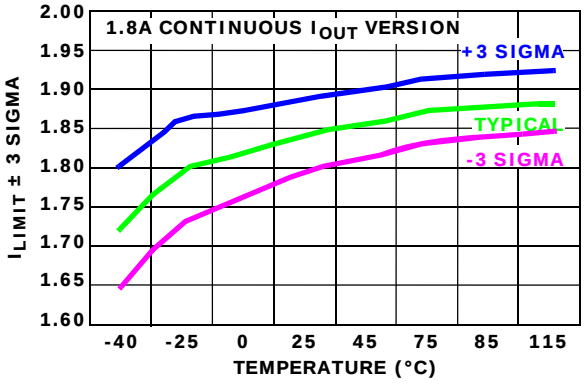



FIGURE 10. LIMITING CURRENT ±3 SIGMA, $V_{IN}$=5V

## Typical Performance Curves (Continued)

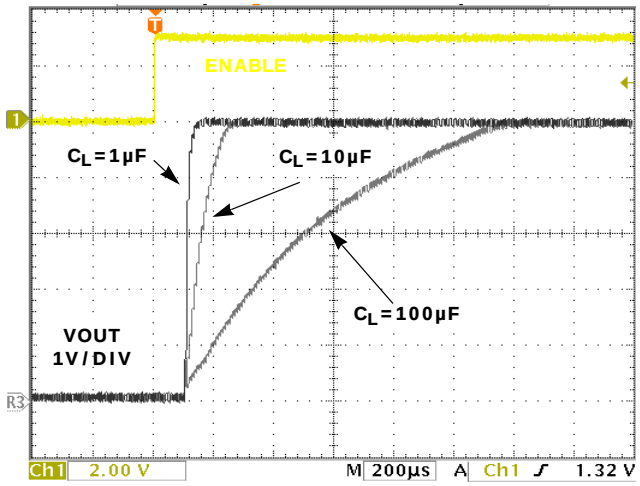



FIGURE 11. $V_{OUT}$ TURN-ON/RISE TIME vs $C_{LOAD}$. $V_{IN}$ = 5V, $R_L$ = 10Ω

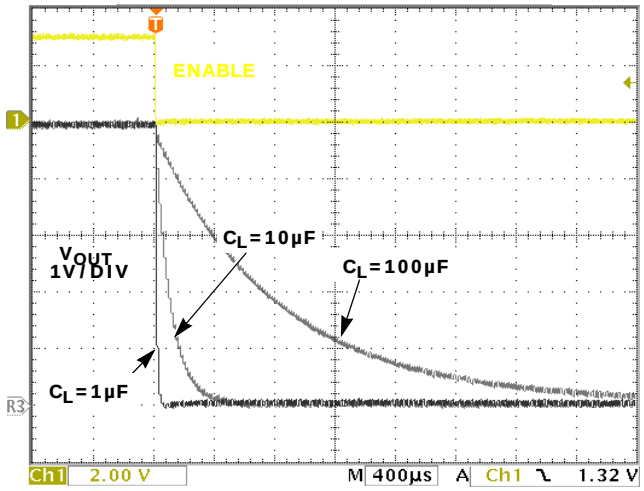



FIGURE 12. $V_{OUT}$ TURN-OFF/FALL TIME vs $C_{LOAD}$. $V_{IN}$ = 5V, $R_L$ = 10Ω

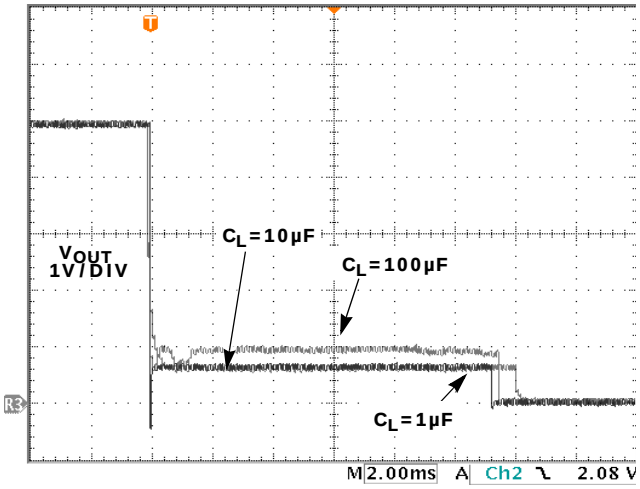



FIGURE 13. LATCH-OFF vs $C_{LOAD}$

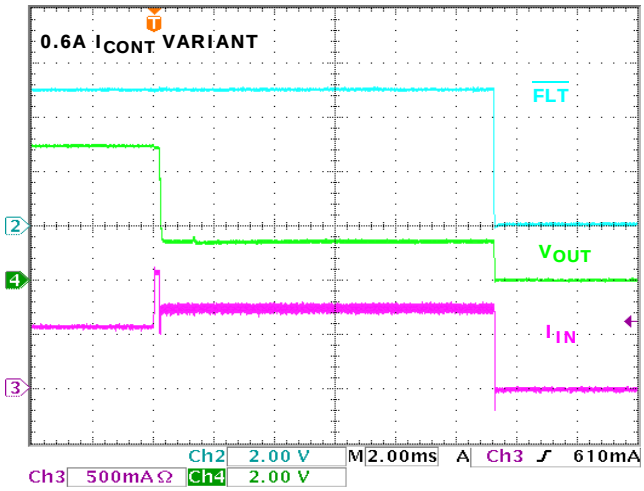



FIGURE 14. $I_{LIM}$ WAVEFORM

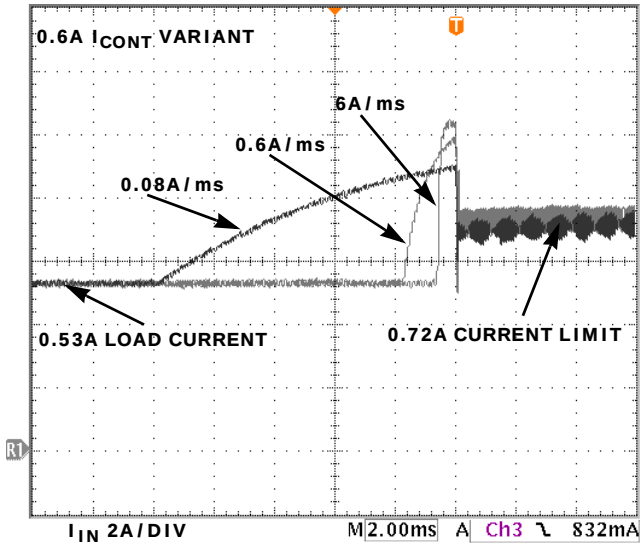



FIGURE 15. OC RAMP RATE $I_{LIM}$ WAVEFORMS

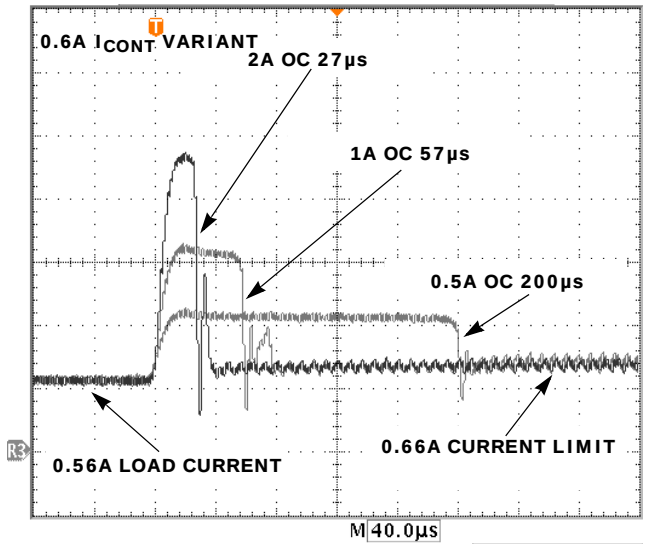



FIGURE 16. PEAK CURRENT SETTLING TIMES

## Typical Performance Curves (Continued)

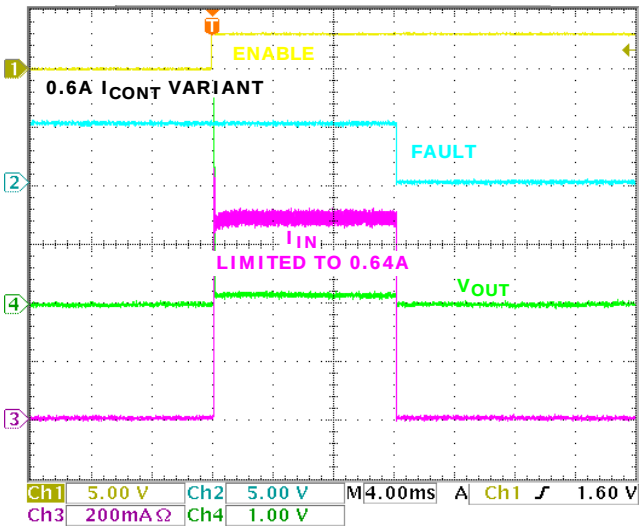



FIGURE 17. TURN-ON INTO A SHORT

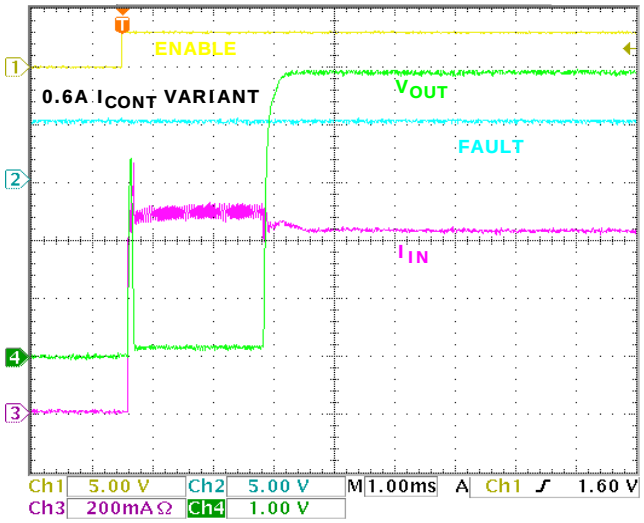



FIGURE 18. TURN-ON INTO MOMENTARY OC

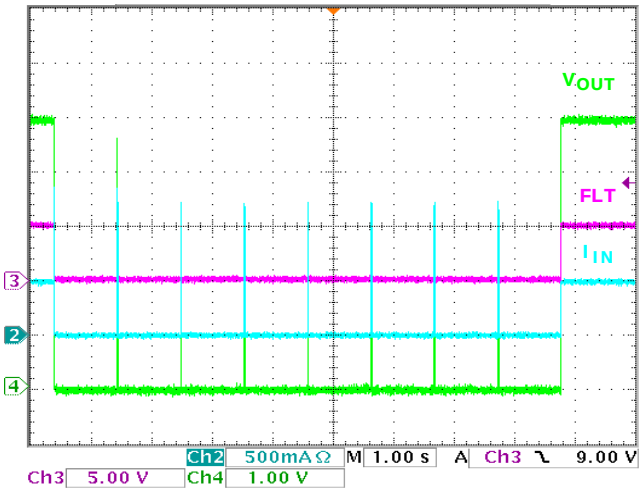



FIGURE 19. ISL6185 RETRY FUNCTION

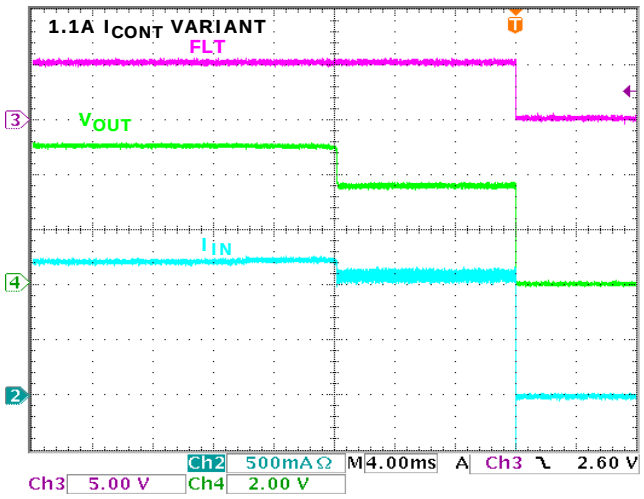



FIGURE 20. $I_{LIM}$ WAVEFORM

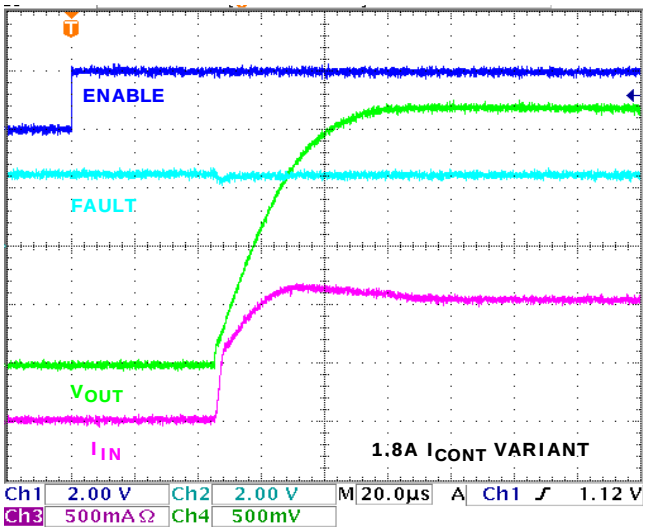



FIGURE 21. $V_{IN}$ = 2.5V TURN-ON INTO 2.2Ω

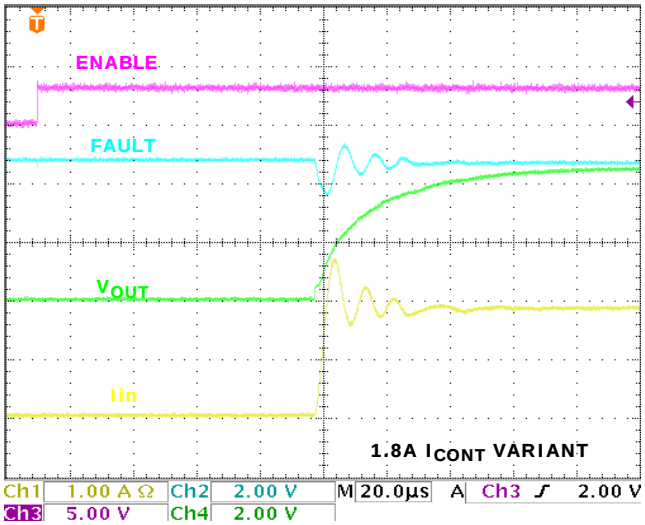



FIGURE 22. $V_{IN}$ = 5V TURN-ON INTO 2.7Ω

## Typical Performance Curves (Continued)

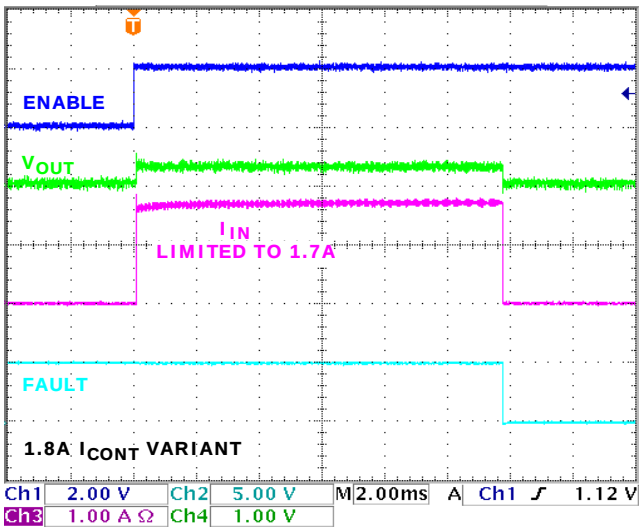



FIGURE 23. TURN-ON INTO A SHORT

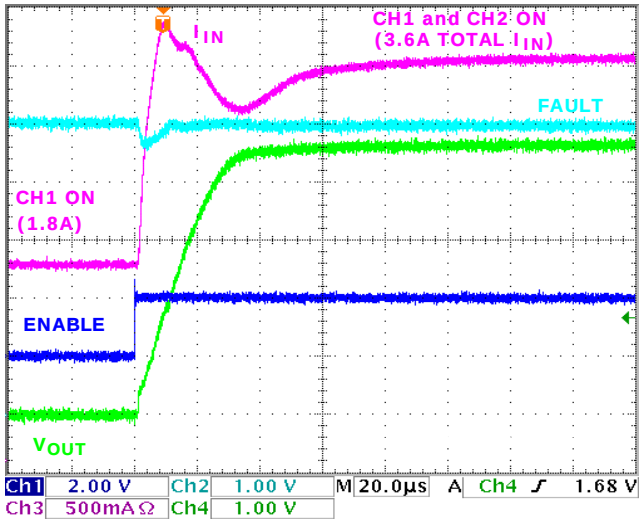



FIGURE 24. TURN-ON 2ND OUTPUT TO FULL LOAD

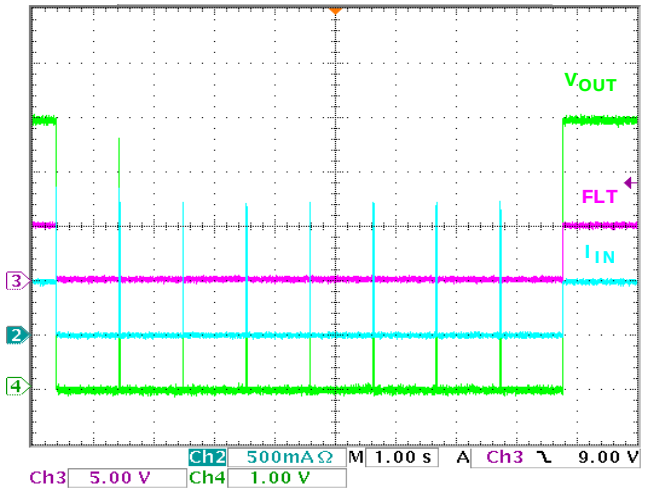



FIGURE 25. ISL6185 RETRY FUNCTION

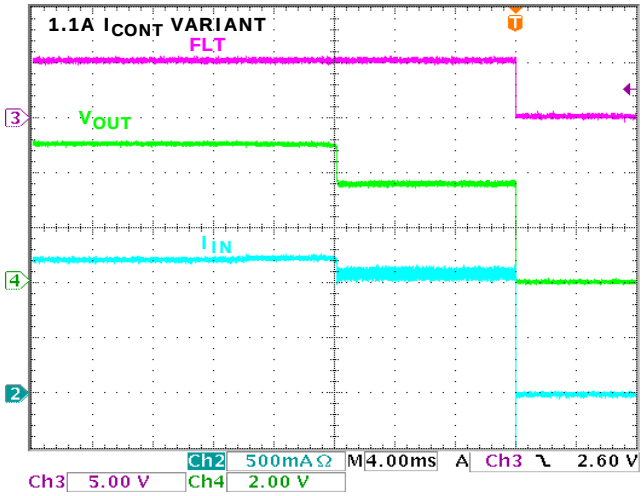
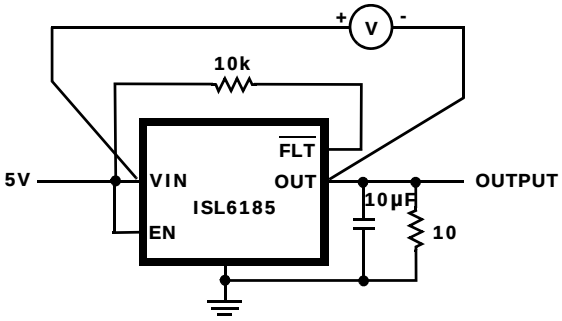



FIGURE 26. $I_{LIM}$ WAVEFORM

FIGURE 26. PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

## Test Circuits




$r_{DS(ON)} = V/(VOUT/10\Omega)$

FIGURE 27A. $r_{DS(ON)}$

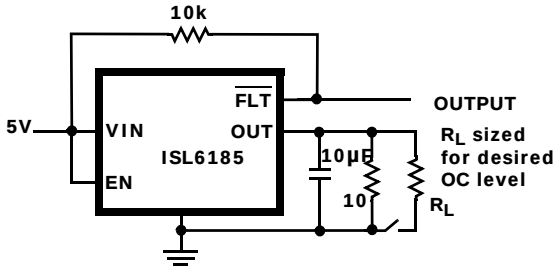



FIGURE 27B. CURRENT LIMITING

FIGURE 27. DC TEST CIRCUIT

## Test Circuits (Continued)

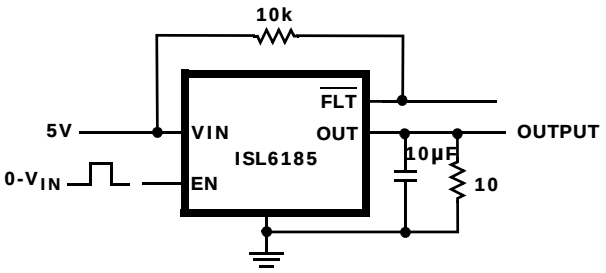



FIGURE 28A. TRANSIENT TEST CIRCUIT

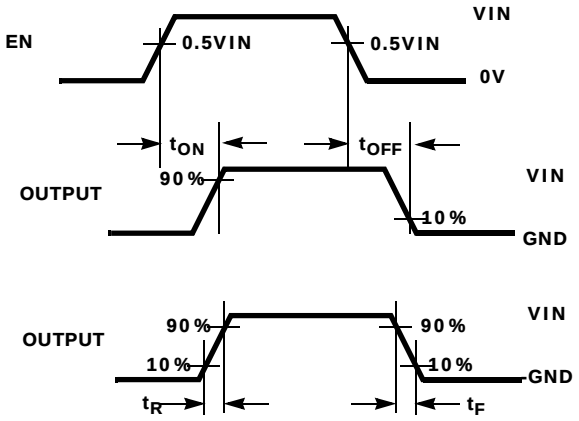
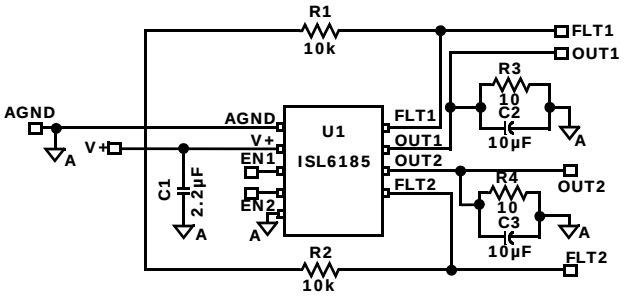



FIGURE 29. TRANSIENT WAVEFORM MEASUREMENT POINTS

## ISL6185xEVAL1Z Schematic and Photo




NOTE: EXPOSED PAD only on DFN packages

FIGURE 30A. ISL6185xEVAL SCHEMATIC

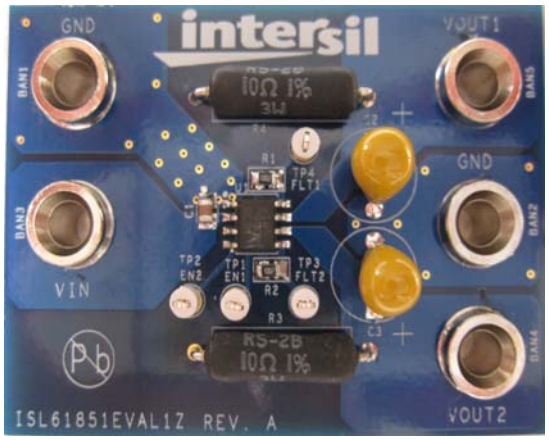



FIGURE 30B. ISL61851EVAL1Z BOARD PHOTO

FIGURE 30. ISL6185xEVAL1Z SCHEMATIC and ISL61851EVAL1Z PHOTOGRAPH

# Application Information

## Using the ISL6185xEVAL1Z Platform General and Biasing Information

There are three (3) evaluation platforms for the ISL6185 family. There is one (1) for each package style, each with a different continuous output current level and a mix of enable polarity and output retry or latch options. See the bottom of Table 1 for standard available evaluation board options. Figure 30A, illustrates the common schematic for all of the evaluation boards, consult the individual package pinouts for those differences.

The evaluation platform is biased and monitored through numerous labeled test points. See Table 1 for test point assignments and descriptions.

**TABLE 1. ISL61851EVAL1Z TEST POINT ASSIGNMENTS**

| TP NAME | DESCRIPTION |
|---|---|
| GND | Eval Board and IC Gnd |
| V+ | Eval Board and IC Bias |
| EN1 | Enable Switch 1 |
| EN2 | Enable Switch 2 |
| FLT2 | Switch 2 Fault |
| OUT2 | Switch Out 2 |
| OUT1 | Switch Out 1 |
| FLT1 | Switch 1 Fault |

Upon proper bias and of the evaluation platform and correct enabling of the IC the ISL6185 will have a nominal $V_{IN}/10\Omega$ load current passing through each enabled switch which is below the continuous current rating. See Figures 11 and 12 for typical ISL6185 turn-on and off waveforms.

External current loading in excess of the trip current level for the particular part being evaluated will result in the ISL6185 entering the current limiting mode. Figure 14 illustrates the current limiting mode for the ISL6185 product variants with 0.6A of continuous load current rating. The scope shot shows current limiting for ~12ms before it is turned off and the fault signal is asserted.

## Application Considerations

The application considerations for the ISL6185 family are widely accepted best industry practices. Good decoupling practices on the VIN pin must be followed with placement close to the IC with at least 2.2µF being recommended. Work to reduce the input and output inductance to the ISL6185 with good PCB layout practices.

When designing with the 1.5A and 1.8A versions in an implementation where the output may be unloaded (open) while the ISL6185 is turned on, a minimum of 4.7µF of capacitive output load is recommended to prevent high dv/dt from unnecessarily activating the surge/ESD control circuit.

The ISL6185 provides several continuous current rated devices specified at $V_{IN}$ = 5V, these are 0.6A, 1.1A, 1.5A and 1.8A options capable over the entire temperature extreme. At $V_{IN}$ = 3.3V the current capability is degraded and the ISL6185 is specified at 0.6A, 1.1A, 1.3A and 1.5A respectively. At $V_{IN}$ = 2.5V there are no min specifications but a typical value is provided for +25°C operation in the specification table. This degraded capability is due to the higher $r_{DS(ON)}$ of the FET switch at the lower bias voltage.

The enhanced thermal characteristics and increased number of bond wires allows the 10 Ld DFN to have a higher current capability than either the 8 Ld SOIC or DFN.

**TABLE 2. ISL6185XEVAL1Z BOARD COMPONENT LISTING**

| COMPONENT DESIGNATOR | COMPONENT FUNCTION | COMPONENT DESCRIPTION |
|---|---|---|
| U1 | ISL6185 | Intersil, ISL6185 |
| R3 - R4 | Output Load Resistors | 10Ω, 5%, 3W |
| R1 - R2 | FLT Output pull up resistor | 10kΩ, 0805 |
| C1 | Decoupling Capacitor | 2.2µF, 0805 |
| C2 - C3 | Load Capacitor | 10µF 16V Electrolytic, Radial Lead |

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| 10/22/10 | FN6937.0 | Initial release. |

## Products

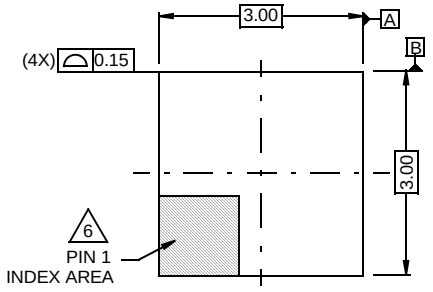
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL6185

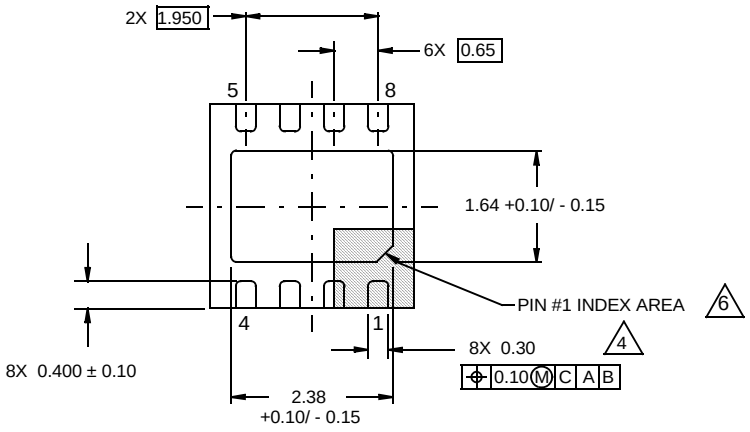
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

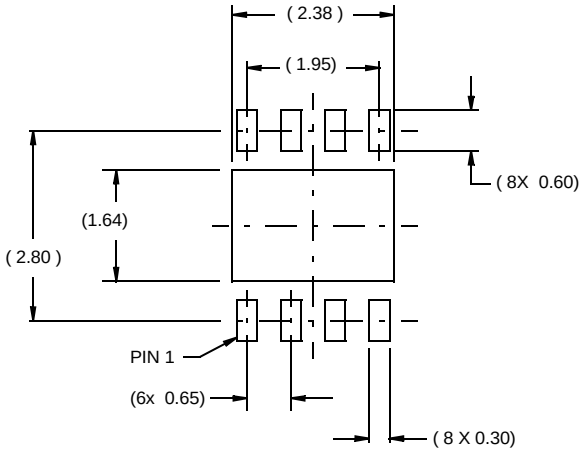
# Package Outline Drawing
## L8.3x3J
**8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 0 9/09**



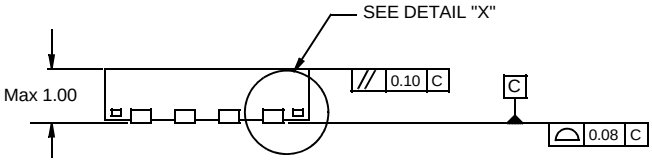

**TOP VIEW**



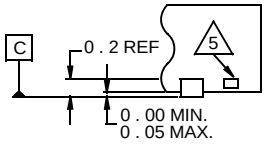

**BOTTOM VIEW**




**TYPICAL RECOMMENDED LAND PATTERN**




**SIDE VIEW**




**DETAIL "X"**

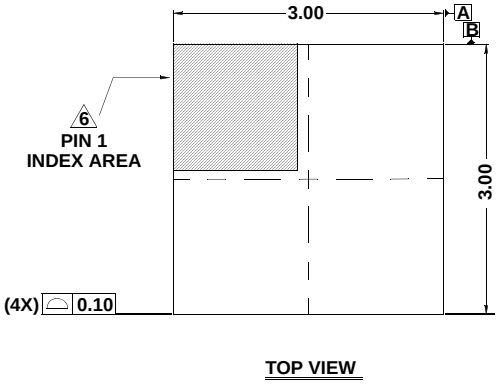
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

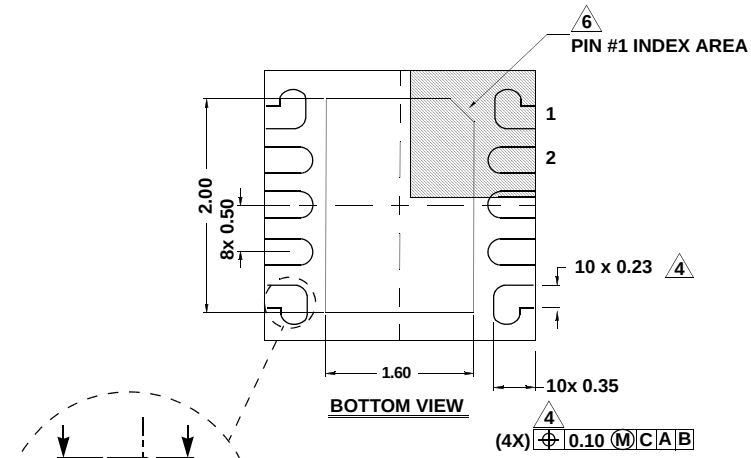
# Package Outline Drawing

## L10.3x3

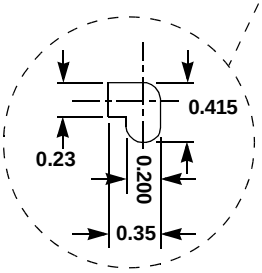
**10 LEAD DUAL FLAT PACKAGE (DFN)**
**Rev 6, 09/09**

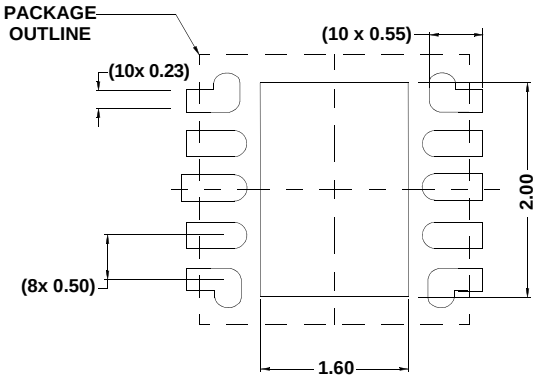



TOP VIEW

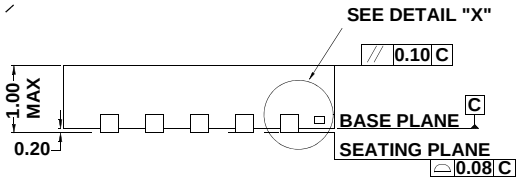



BOTTOM VIEW

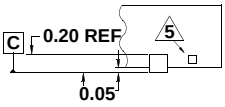



TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW

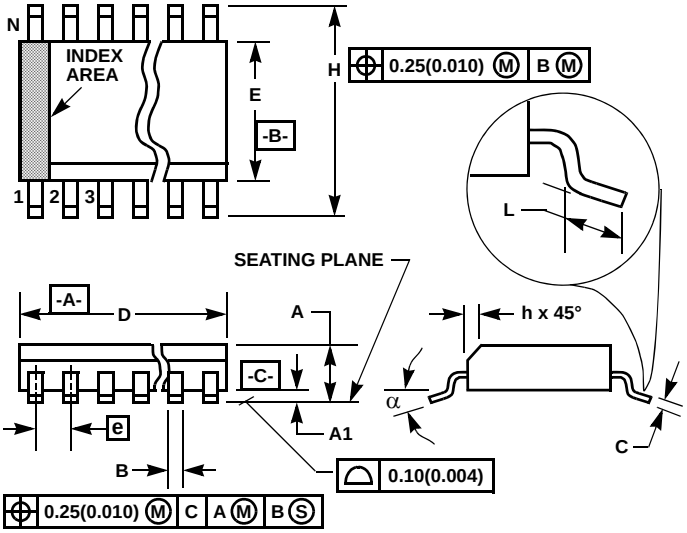



DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

## *Small Outline Plastic Packages (SOIC)*




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 1 6/05