Freescale Semiconductor
Product Brief

Document Number: MC56F825XPB
Rev. 2, 06/2010

MC56F825x/MC56F824x Product Brief

The MC56F825x/MC56F824x is a member of Freescale's family of digital signal controllers (DSCs) based on the 56800E core. It combines, on a single chip, DSP processing power and microcontroller functionality with a flexible set of peripherals, creating a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, it is well-suited for many consumer and industrial applications, including:

- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Solar inverters
- Battery chargers and management
- Switched-mode power supplies and management
- Power metering
- Motor control (ACIM, BLDC, PMSM, SR, and stepper)
- Handheld power tools
- Arc detection

Contents

freescale™ semiconductor

Preliminary

- Medical devices/equipment
- Instrumentation
- Lighting ballast

The 56800E core is based on a dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The MC56F825x/MC56F824x supports program execution from internal memories. Two data operands per instruction cycle can be accessed from the on-chip data RAM. A full set of programmable peripherals supports various applications. Each peripheral can be independently shut down to save power. Any pin except power pins can also be configured as General Purpose Input/Output (GPIO).

1 Application examples

The MC56F825x/MC56F824x includes many peripherals that are especially useful for industrial control, motion control, home appliances, general-purpose inverters, smart sensors, fire and security systems, switched-mode power supplies, power management, UPSs, and medical monitoring applications.

1.1 Digital power supply

Figure 1 shows the MC56F825x/MC56F824x used in controlling a secondary DC-DC phase shifting converter in a typical industrial isolated AC/DC power supply. This topology is being widely used in telecom power supplies, server power supplies, and other industrial equipment.

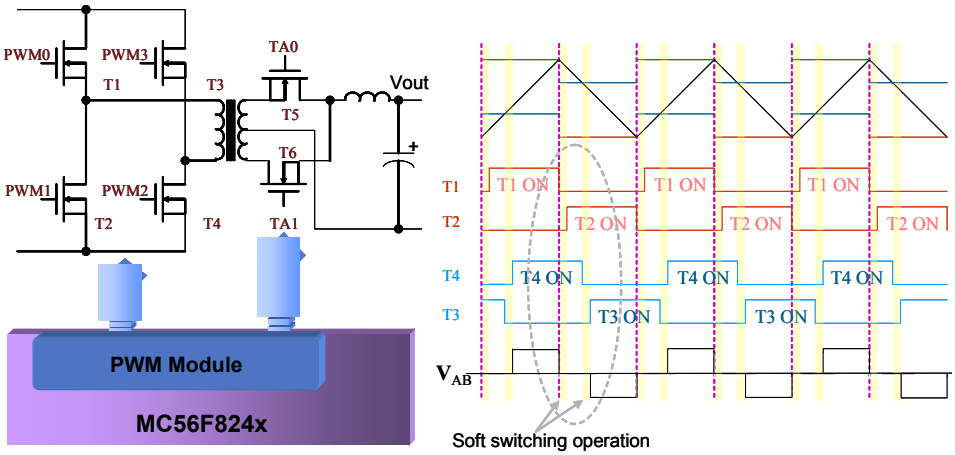

Figure 1. Phase shift power converter

1.2 Servo motor

Figure 2 shows a high precision servo motor control system that is controlled by an MC56F825x device.

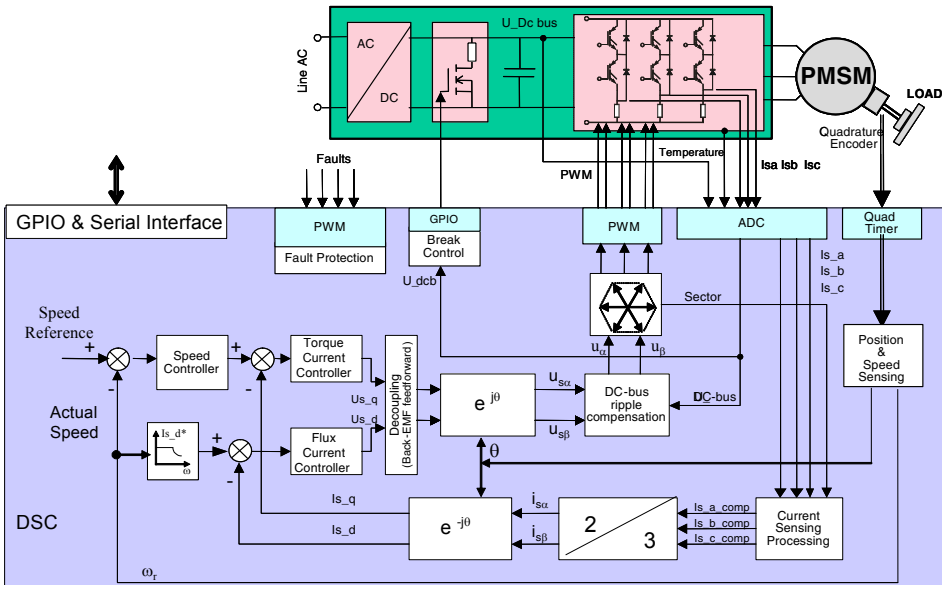

Figure 2. High-performance PMSM servo system

2 Features

A full set of programmable peripherals—eFlexPWM, ADCs, QSCIs, QSPI, I^{2}Cs, MSCAN, inter-module crossbar, quad timers, CRC block, DACs, analog comparators, and on-chip/off-chip clock sources—supports various applications.

2.1 MC56F825x/MC56F824x family comparison

Table 1 compares the MC56F825x/MC56F824x devices.

Table 1. MC56F825x/MC56F824x device comparison

Feature		56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Operation frequency (MHz)		60					
High speed peripheral clock (MHz)		120					
Flash memory size (KB) with 1024 words per page		48	48	48	64	64	64
RAM size (KB)		6	6	8	8	8	8
Enhanced Flex PWM (eFlexPWM)	High resolution NanoEdge PWM (520 ps res.)	6	6	6	6	6	6
	Enhanced Flex PWM with input capture	0	0	3	0	0	3
	PWM fault inputs (from crossbar input)	4	4	4	4	4	4
12-bit ADC with ×1, ×2, ×4 programmable gain		2 × 4 Ch	2 × 5 Ch	2 × 8 Ch	2 × 4 Ch	2 × 5 Ch	2 × 8 Ch
Analog comparators (CMP), each with integrated 5-bit DAC		3					
12-bit DAC		1					
Cyclic redundancy check (CRC)		Yes					
Inter-integrated circuit (I^{2}C) / SMBus		2					

Table 1. MC56F825x/MC56F824x device comparison (continued)

Feature		56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Queued serial peripheral interface (QSPI)		1					
High-speed queued serial communications interface (QSCI)[1]		2					
Controller area network (MSCAN)		0			1		
High-speed 16-bit multi-purpose timers (TMR)[2]		8					
Computer operating properly (COP) watchdog timer		Yes					
Integrated power-on reset and low voltage detection		Yes					
Phase-locked loop (PLL)		Yes					
8 MHz (400 kHz at standby mode) on-chip ROSC		Yes					
Crystal/resonator oscillator		Yes					
Crossbar	Input pins	6	6	6	6	6	6
	Output pins	2	2	6	2	2	6
General purpose I/O (GPIO)[3]		35	39	54	35	39	54
IEEE 1149.1 Joint Test Action Group (JTAG) interface		Yes					
Enhanced on-chip emulator (EOnCE)		Yes					
Operating temperature range		–40 °C to 105 °C					
Package		44LQFP	48LQFP	64LQFP	44LQFP	48LQFP	64LQFP

NOTES:
1 Can be clocked by high-speed peripheral clock up to 120 MHz.
2 Can be clocked by high-speed peripheral clock up to 120 MHz.
3 Shared with other function pins.

2.2 Block diagram

Figure 3 is a simplified block diagram of the MC56F825x.

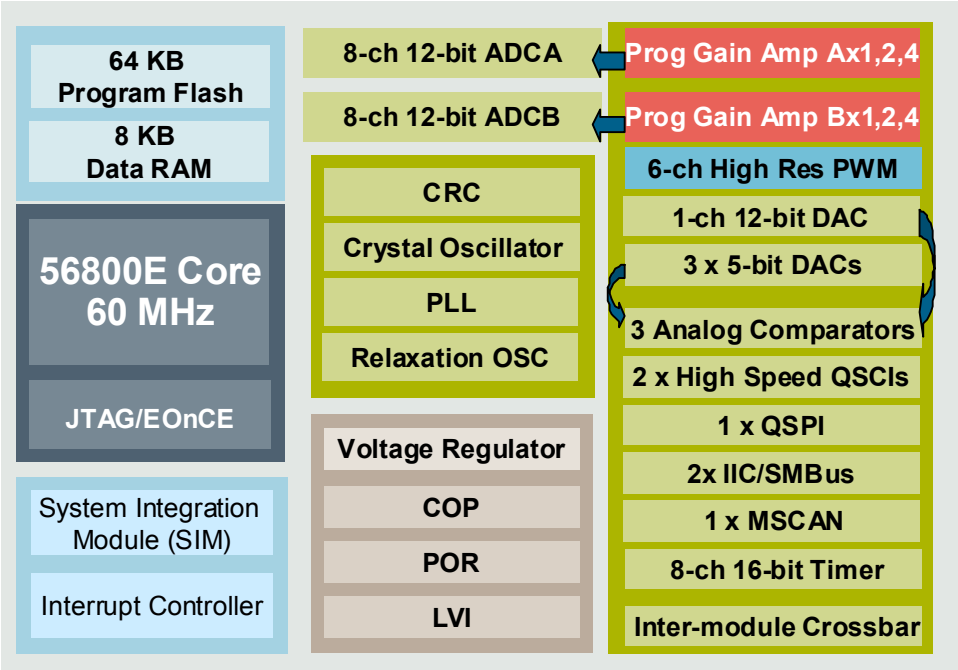

Figure 3. MC56F825x block diagram

2.3 Operation parameters

- 3.0 V to 3.6 V operation (power supplies and I/O)
- From power-on reset: approximately 2.7 V to 3.6 V
- Ambient temperature operating range: –40 °C to +105 °C

2.4 Chip-level features

On-chip features include:

- 60 MHz operation frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - 56F8245/46: 48 KB (24K × 16) flash memory; 6 KB (3K × 16) unified data/program RAM
  - 56F8247: 48 KB (24K × 16) flash memory; 8 KB (4K × 16) unified data/program RAM
  - 56F8255/56/57: 64 KB (32K × 16) flash memory; 8 KB (4K × 16) unified data/program RAM
- eFlexPWM with up to 9 channels, including 6 channels with high (520 ps) resolution NanoEdge placement
- Two 8-channel, 12-bit analog-to-digital converters (ADCs)
  - Dynamic ×2 and ×4 programmable amplifier
  - Conversion time as short as 600 ns
  - Input current-injection protection
- Three analog comparators with integrated 5-bit DAC references

- Cyclic redundancy check (CRC) generator
- Two high-speed queued serial communication interface (QSCI) modules with LIN slave functionality
- Queued serial peripheral interface (QSPI) module
- Two SMBus-compatible inter-integrated circuit (I^2C) ports
- Freescale's scalable controller area network (MSCAN) 2.0 A/B module
- Two 16-bit quad timers (2 × 4 16-bit timers)
- Computer operating properly (COP) watchdog module
- On-chip relaxation oscillator: 8 MHz (400 kHz at standby mode)
- Crystal/resonator oscillator
- Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
- Inter-module crossbar connection
- Up to 54 GPIOs
- 44-pin LQFP, 48-pin LQFP, and 64-pin LQFP packages
- Single supply: 3.0 V to 3.6 V

2.4.1 Core

- Efficient 56800E digital signal processor (DSP) engine with dual Harvard architecture
  - Three internal address buses
  - Four internal data buses
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Instruction set supporting DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

2.4.2 Memory

- Dual Harvard architecture that permits as many as three simultaneous accesses to program and data memory
- 48 KB (24K × 16) to 64 KB (32K × 16) on-chip flash memory with 2048 bytes (1024 × 16) page size
- 6 KB (3K × 16) to 8 KB (4K × 16) on-chip RAM that is byte-addressable
- EEPROM emulation capability using flash
- Support for 60 MHz program execution from both internal flash and RAM memories
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash

2.4.3 Interrupt controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source:
    - Level 0
    - Level 1
    - Level 2
  - Unmaskable level 3 interrupts include:
    - Illegal instruction
    - Hardware stack overflow
    - Misaligned data access
    - SWI3 instruction
  - Maskable level 3 interrupts include:
    - EOnCE step counter
    - EOnCE breakpoint unit
    - EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Nested interrupts: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

The masking of interrupt priority level is managed by the 56800E core.

2.4.4 Power-saving features

- Low-speed run, wait, and stop modes: as low as 781 Hz clock provided by OCCS and internal ROSC

- Large regulator standby mode available for reducing power consumption at low-speed mode
- Less than 30 µs typical wakeup time from stop modes
- Each peripheral can be individually disabled to save power

2.5 Module features

The following is a brief summary of the peripheral modules.

2.5.1 eFlexPWM

- One enhanced Flex pulse width modulator (eFlexPWM) module
  - — Up to nine output channels
  - — Sixteen bits of resolution for center, edge aligned, and asymmetrical PWMs
  - — Each complementary pair can operate with its own PWM frequency-based and deadtime values
    - – 4 Time base
    - – Independent top and bottom deadtime insertion
  - — PWM outputs can operate as complementary pairs or independent channels
  - — Independent control of both edges of each PWM output
  - — 6-channel NanoEdge high resolution PWM
    - – Fractional delay for enhanced resolution of the PWM period and edge placement
    - – Arbitrary eFlexPWM edge placement—PWM phase shifting
    - – NanoEdge implementation: 520 ps PWM frequency resolution
  - — 3-channel PWM with full input capture features
    - – Three PWM channels: PWMA, PWMB, and PWMX
    - – Enhanced input capture functionality
  - — Support for synchronization to external hardware or other PWM
  - — Double buffered PWM registers
    - – Integral reload rates from one to sixteen
    - – Half cycle reload capability
  - — Multiple output trigger events can be generated per PWM cycle via hardware
  - — Support for double switching PWM outputs
  - — Up to four fault inputs can be assigned to control multiple PWM outputs
    - – Programmable filters for fault inputs
  - — Independently programmable PWM output polarity
  - — Individual software control for each PWM output
  - — All outputs can be programmed to change simultaneously via a FORCE_OUT event
  - — PWMX pin can optionally output a third PWM signal from each submodule
  - — Channels not used for PWM generation can be used for buffered output compare functions
  - — Channels not used for PWM generation can be used for input capture functions

- Enhanced dual edge capture functionality
- The option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

2.5.2 ADC

- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 × 8 channel external inputs
  - Built-in ×1, ×2, ×4 programmable gain pre-amplifier
  - Maximum ADC clock frequency up to 10 MHz
    - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
    - Additional conversion time of six ADC clock cycles (6 × 100 ns = 600 ns)
  - Sequential, parallel, and independent scan mode
  - First eight samples have offset, limit, and zero-crossing calculation supported
  - ADC conversions can be synchronized by eFlexPWM and timer modules via internal crossbar module
  - Support for simultaneous and software triggering conversions
  - Support for multi-triggering mode with a programmable number of conversions on each trigger

2.5.3 XBAR

- Inter-module crossbar switch (XBAR)
  - Programmable internal module connections between and among the eFlexPWM, ADCs, quad timers, 12-bit DAC, CMPs, and package pins
  - User-defined input/output pins for PWM fault inputs, timer input/output, ADC triggers, and comparator outputs

2.5.4 CMP

- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, eFlexPWM fault input, eFlexPWM source, and external pin output as well as trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
  - 32-tap programmable voltage reference per comparator

2.5.5 DAC

- One 12-bit digital-to-analog converter (12-bit DAC)
  - 12-bit resolution
  - Power-down mode
  - Output can be routed to internal comparator or off chip

2.5.6 TMR

- Two four-channel 16-bit multi-purpose timer (TMR) modules
  - Four independent 16-bit counter/timers with cascading capability per module
  - Up to 120 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to twelve operating modes
  - Four external inputs and two external outputs

2.5.7 QSCI

- Two queued serial communication interface (QSCI) modules with LIN slave functionality
  - Up to 120 MHz operating clock
  - Four-byte-deep FIFOs available on both transmit and receive buffers
  - Full-duplex or single-wire operation
  - Programmable 8- or 9-bit data format
  - 13-bit integer and 3-bit fractional baud rate selection
  - Two receiver wakeup methods:
    - Idle line
    - Address mark
  - 1/16 bit-time noise detection
  - LIN slave operation

2.5.8 QSPI

- One queued serial peripheral interface (QSPI) module
  - Full-duplex operation
  - Four-word deep FIFOs available on both transmit and receive buffers
  - Master and slave modes
  - Programmable length transactions (2–16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
  - Maximum slave module frequency = module clock frequency divided by two
  - 13-bit baud rate divider for low-speed communication

2.5.9 I^2C

- Two inter-integrated circuit (I^2C) ports
  - Operation at up to 400 kbps
  - Support for master and slave operation
  - Support for 10-bit address mode and broadcasting mode
  - Support for SMBus, version 2

2.5.10 MSCAN

- One Freescale Scalable Controller Area Network (MSCAN) module
  - Fully compliant with CAN protocol version 2.0 A/B
  - Support for standard and extended data frames
  - Support for data rate up to 1 Mbps
  - Five receive buffers and three transmit buffers

2.5.11 COP

- Computer operating properly (COP) watchdog timer capable of selecting different clock sources
  - Programmable prescaler and time-out period
  - Programmable wait, stop, and partial power-down mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of three clock sources:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IP bus to 60 MHz)

2.5.12 PS

- Power supervisor (PS)
  - On-chip linear regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated low-voltage detection to generate warning interrupt if V_{DD} is below low-voltage detection (LVI) threshold
  - Integrated power-on reset (POR)
    - Reliable reset process during power-on procedure
    - POR is released after V_{DD} passes low voltage detection (LVI) threshold
  - Integrated brown-out reset
  - Run, wait, and stop modes

2.5.13 PLL

- Phase-locked loop (PLL) providing a high-speed clock to the core and peripherals
  - 2× system clock provided to quad timers and SCIs
  - Loss of lock interrupt
  - Loss of reference clock interrupt

2.5.14 Clock source

- Clock sources
  - On-chip relaxation oscillator with two user-selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - External clock: crystal oscillator, ceramic resonator, and external clock source

2.5.15 CRC

- Cyclic redundancy check (CRC) generator
  - Hardware CRC generator circuit using 16-bit shift register
  - CRC16-CCITT compliance with ×16 + ×12 + ×5 + 1 polynomial
  - Error detection for all single, double, odd, and most multi-bit errors
  - Programmable initial seed value
  - High-speed hardware CRC calculation
  - Optional feature to transpose input data and CRC result via transpose register—required on applications where bytes are in LSB (least significant bit) format

2.5.16 GPIO

- Up to 54 general-purpose I/O (GPIO) pins
  - 5 V tolerant I/O
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Individual control for each output pin to be in push-pull mode or open-drain mode
  - Hysteresis and configurable pullup device on all input pins
  - Ability to generate interrupt with programmable rising or falling edge and software interrupt
  - Configurable drive strength: 4 mA / 8 mA sink/source current

2.5.17 JTAG/EOnCE

- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

3 Award-winning development environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards can support concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

4 Document revision history

Table 2 summarizes changes to this document since the release of the previous version.

Table 2. Revision History

Revision	Location(s)	Substantive change(s)
2	Section 2.4.4, “Power-saving features,” on page 7	Corrected feature descriptions
	Section 2.5.2, “ADC,” on page 9	Corrected unit symbol for single conversion time value
	Section 2.5.7, “QSCI,” on page 10	Added summary of baud rate selection features
	Section 2.5.12, “PS,” on page 11	Corrected name of power supervisor (PS) module

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MC56F825XPB
Rev. 2
06/2010

Preliminary

freescale™
semiconductor