



STL7NM60N

N-channel 600 V, 0.805 Ω , 5.8 A PowerFLAT™ (5x5)
MDmesh™ II Power MOSFET

Features

Order code	V _{DSS} @ T _{JMAX}	R _{DS(on)} max.	I _D
STL7NM60N	650 V	< 0.90 Ω	5.8 A ⁽¹⁾

1. The value is rated according Rthj-case

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

Switching applications

Description

These devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

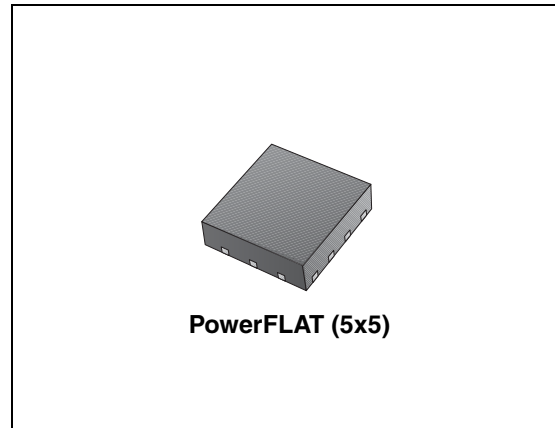


Figure 1. Internal schematic diagram

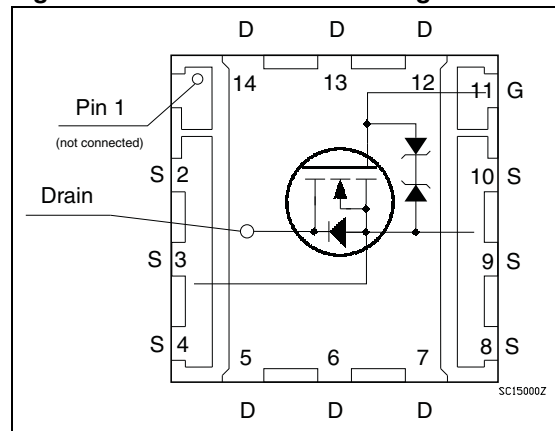


Table 1. Device summary

Order code	Marking	Package	Packaging
STL7NM60N	7NM60N	PowerFLAT™ (5x5)	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	5.8	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.7	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	1.4	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	0.9	A
$I_{DM}^{(2), (5)}$	Drain current (pulsed)	5.6	A
$P_{TOT}^{(5)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	4	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	68	W
I_{AS}	Avalanche current, repetitive or not-repetitive ⁽³⁾	2	A
E_{AS}	Single pulse avalanche energy ⁽⁴⁾	119	mJ
	Derating factor ⁽⁵⁾	0.02	W/ $^\circ\text{C}$
dv/dt ⁽⁶⁾	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according Rthj-case.
2. Pulse width limited by safe operating area.
3. Pulse width limited by T_{jmax}
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$
5. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$
6. $I_{SD} \leq 17\text{ A}$, $dv/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\%V_{(BR)DSS}$.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max.	1.85	$^\circ\text{C}/\text{W}$
$R_{thj\text{-amb}}^{(1)}$	Thermal resistance junction-amb max.	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2.5 \text{ A}$		0.805	0.90	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	363	-	pF
C_{oss}	Output capacitance			24.6		pF
C_{rss}	Reverse transfer capacitance			1.1		pF
$C_{oss \text{ eq.}}^{(1)}$	Output equivalent capacitance	$V_{GS} = 0$, $V_{DS} = 0$ to 480 V	-	130	-	pF
R_g	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 test signal level = 20 mV open drain	-	5.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480 \text{ V}$, $I_D = 5 \text{ A}$	-	14	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10 \text{ V}$		2.7		nC
Q_{gd}	Gate-drain charge (see Figure 15)			2.7		nC

1. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14)		7		ns
t_r	Rise time			10		ns
$t_{d(off)}$	Turn-off delay time				26	ns
t_f	Fall time				12	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		5.8	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)				23	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16)	-	213		ns
Q_{rr}	Reverse recovery charge			1.5		nC
I_{RRM}	Reverse recovery current			14		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	265		ns
Q_{rr}	Reverse recovery charge			1.8		nC
I_{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area
2. When mounted on FR-4 board of 1inch², 2 oz Cu
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

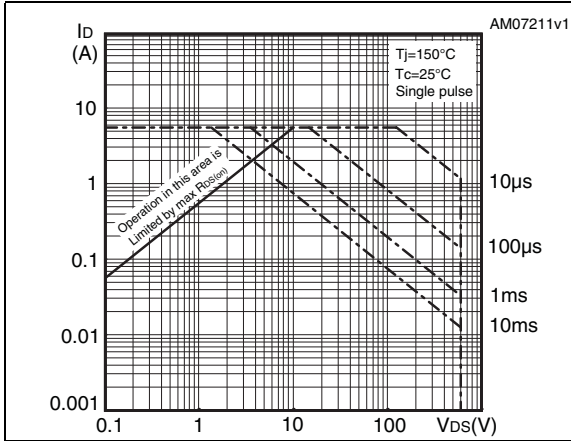


Figure 3. Thermal impedance

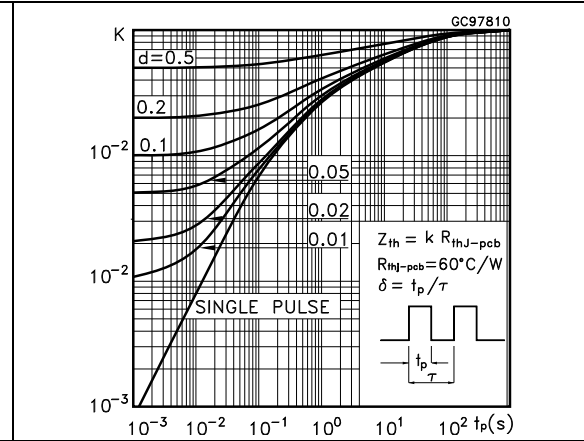


Figure 4. Output characteristics

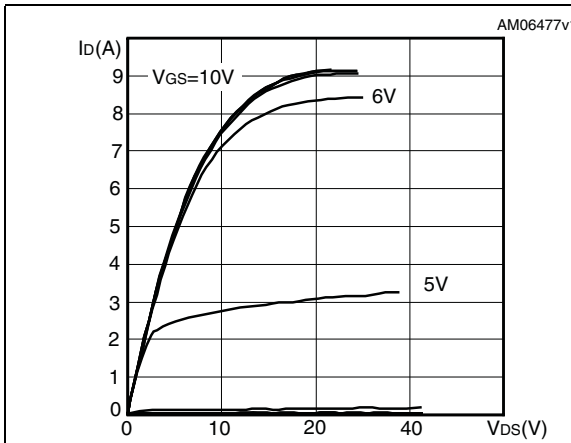


Figure 5. Transfer characteristics

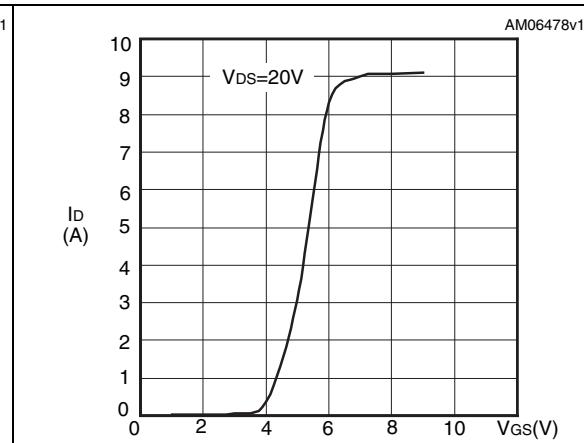


Figure 6. Gate charge vs gate-source voltage Figure 7. Static drain-source on resistance

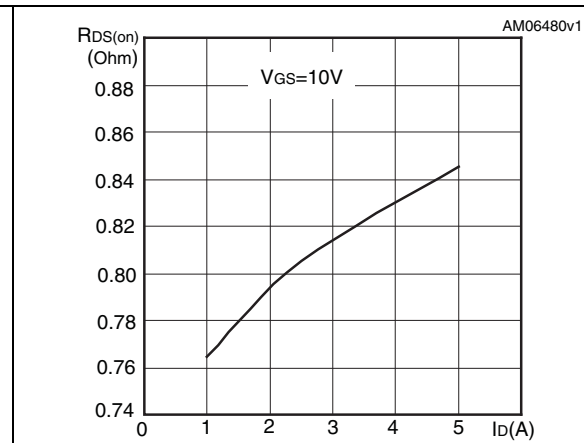
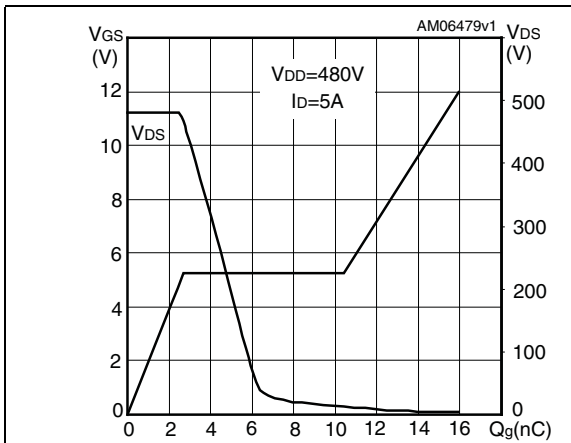


Figure 8. Capacitance variations

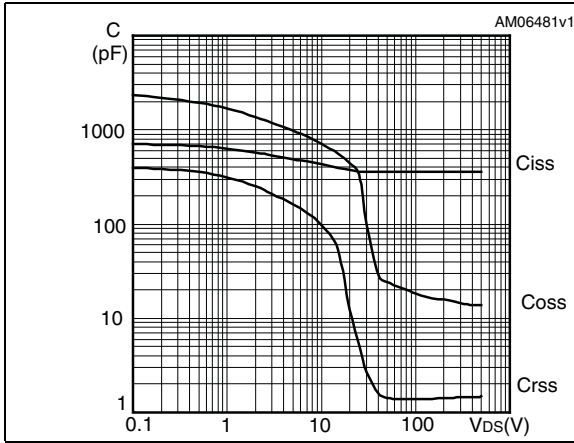


Figure 9. Output capacitance stored energy

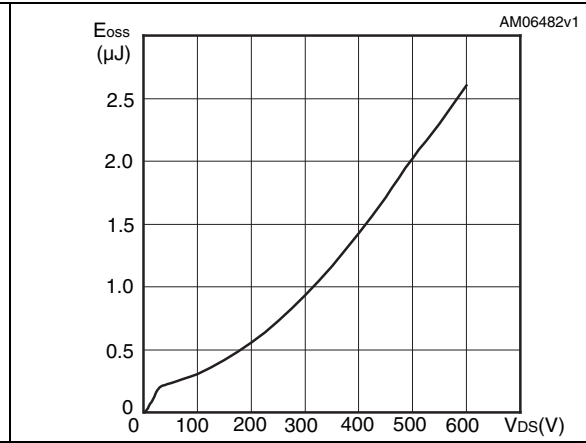


Figure 10. Normalized gate threshold voltage vs temperature

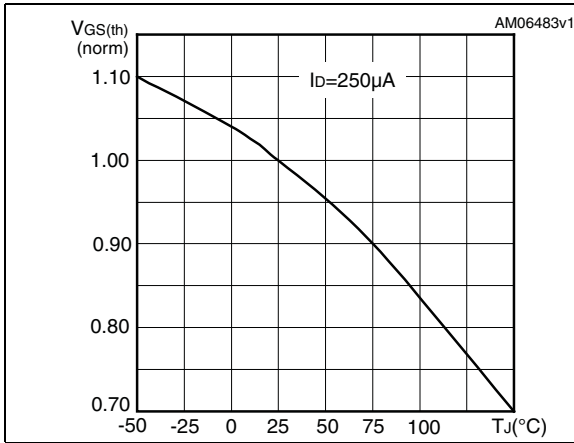


Figure 11. Normalized on resistance vs temperature

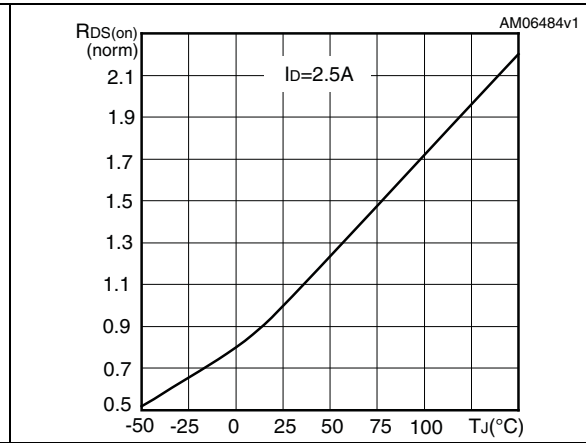


Figure 12. Normalized BV_{DSS} vs temperature

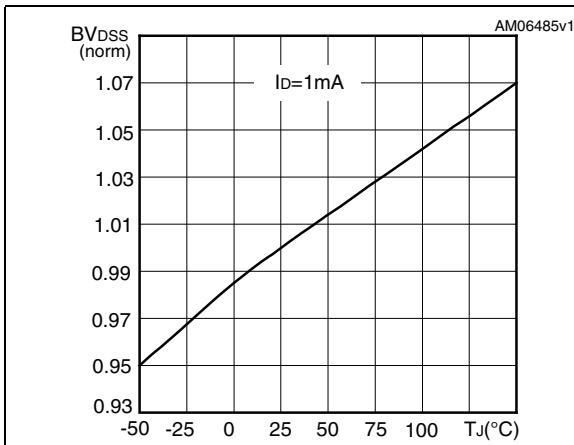
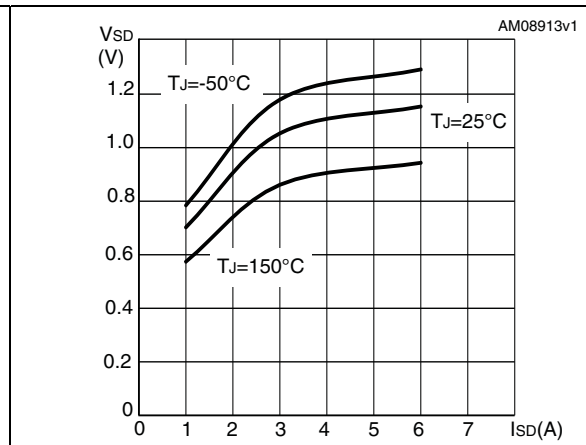


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

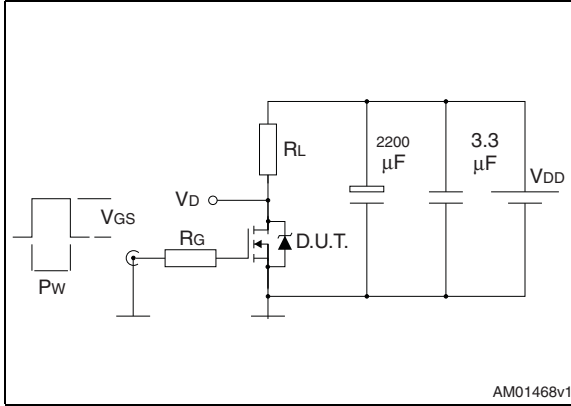


Figure 15. Gate charge test circuit

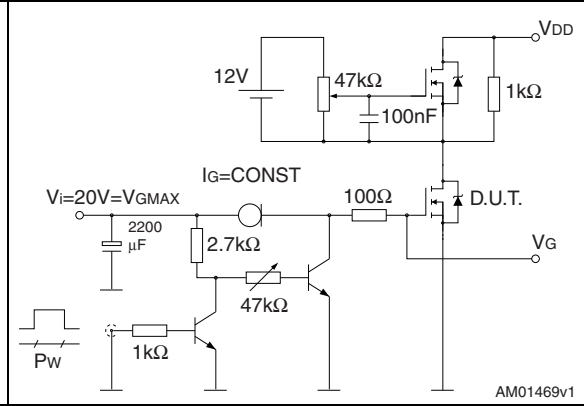


Figure 16. Test circuit for inductive load switching and diode recovery times

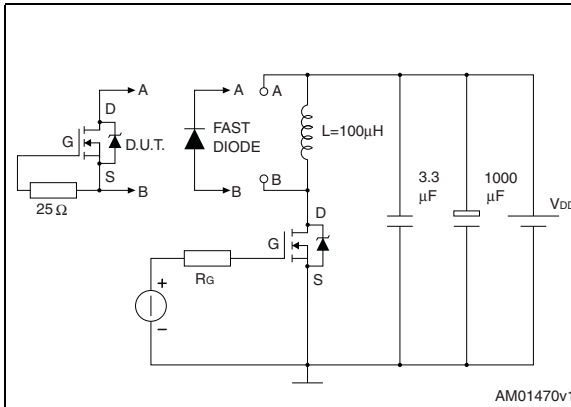


Figure 17. Unclamped inductive load test circuit

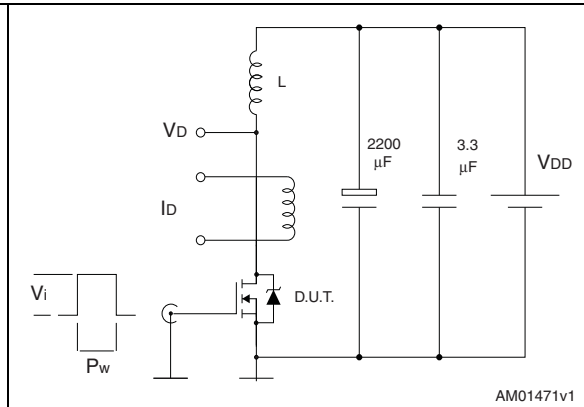


Figure 18. Unclamped inductive waveform

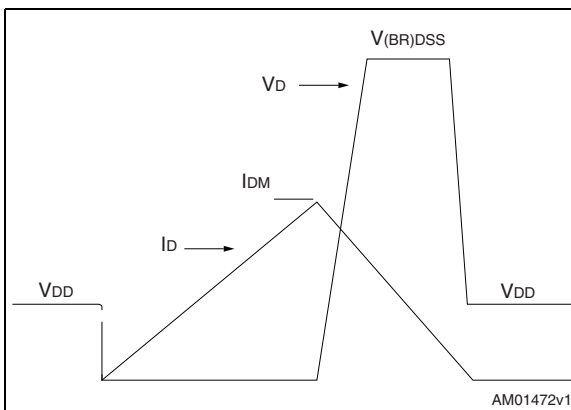
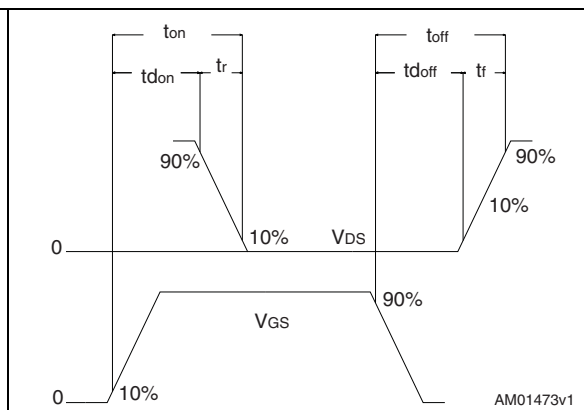


Figure 19. Switching time waveform



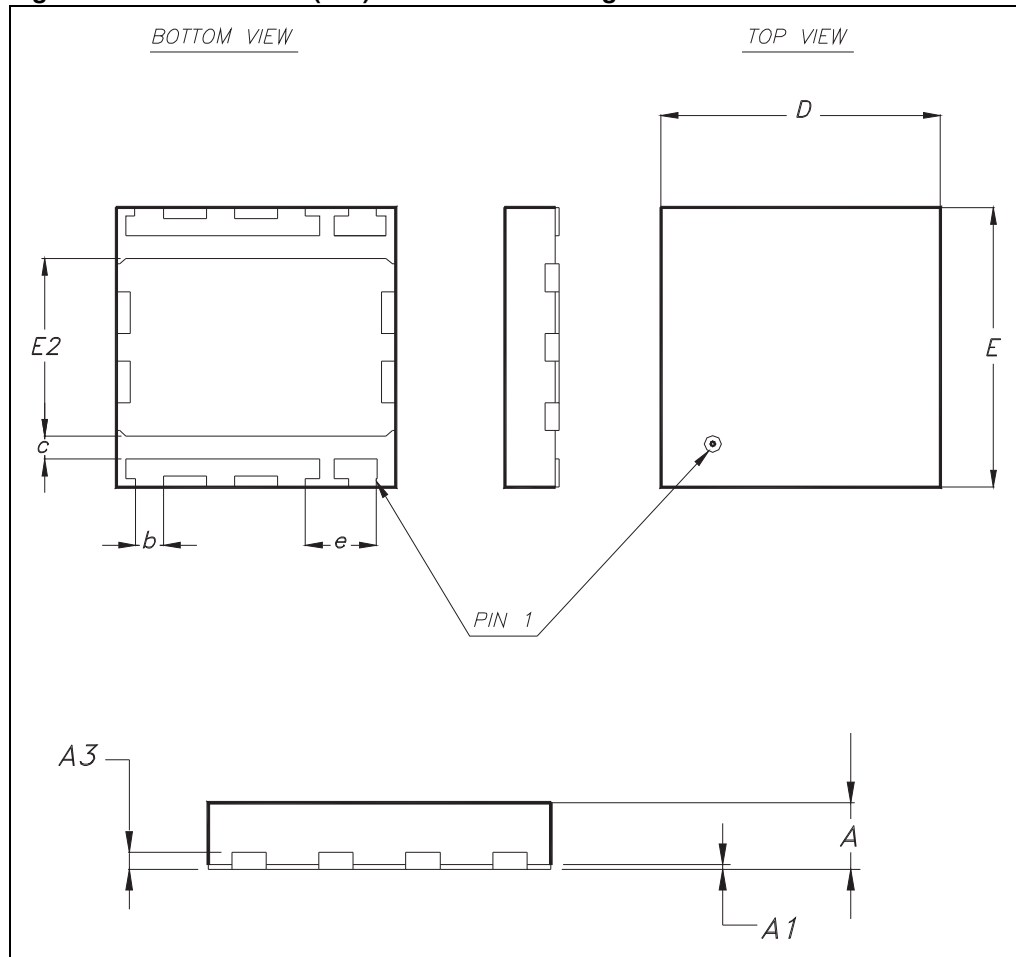
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. PowerFLAT™(5x5) mechanical dimensions

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.0
A1	0	0.02	0.05
A3		0.24	0.90
D	4.90	5.0	5.10
E	4.90	5.0	5.10
E2	2.49	2.57	2.64
e	1.22	1.27	1.32
b	0.43	0.51	0.58
c	0.64	0.71	0.79

Figure 20. PowerFLAT™(5x5) mechanical drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Jan-2011	1	First release

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