STD44N4LF6

N-channel 40 V, 8.9 mΩ, 44 A DPAK STripFET™ VI DeepGATE™ Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STD44N4LF6	40 V	12.5 mΩ	44 A

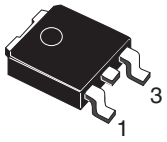
- 100% avalanche tested
- Logic level drive

Application

- Switching applications
- Automotive

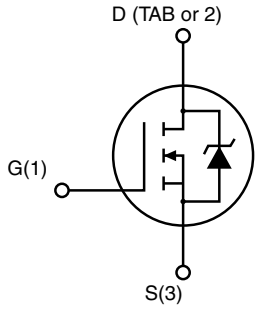
Description

This product utilizes the 6th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure.The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in a standard package.



DPAK

Figure 1. Internal schematic diagram



AM01474v1

Table 1. Device summary

Order code	Marking	Package	Packaging
STD44N4LF6	44N4LF6	DPAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	44	A
I_D	Drain current (continuous) at T_C = 100 °C	31	A
I_{DM} (1)	Drain current (pulsed)	176	A
P_{TOT}	Total dissipation at T_C = 25 °C	50	W
	Derating factor	0.33	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Operating junction temperature		

1. Pulse is rated according SOA

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max (1)	50	°C/W

1. When mounted on 1 inch^2, 2 oz Cu.

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current	20	A
E_{AS} (1)	Single pulse avalanche energy	150	mJ

1. Starting Tj = 25 °C, $I_D = I_{AV}$, V_{DD} = 24 V

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250 µA, V_{GS}= 0	40	-		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 20 V V_{DS} = 20 V,Tc = 125 °C		-	1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	-	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 5 V, I_D = 20 A V_{GS} = 10 V, I_D = 20 A		11.3 8.9	18 12.5	mΩ

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS} = 0 V	-	1190 200 110	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 20 V, I_D = 40 A V_{GS} = 10 V *(see Figure 14)*	-	22 5 4.3	-	nC nC nC
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.1	-	Ω

Table 7. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 20 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 15)*	-	15 65	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time		-	150 110	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		44 176	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 32 V, T_J = 150 °C *(see Figure 17)*	-	27 256 2		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

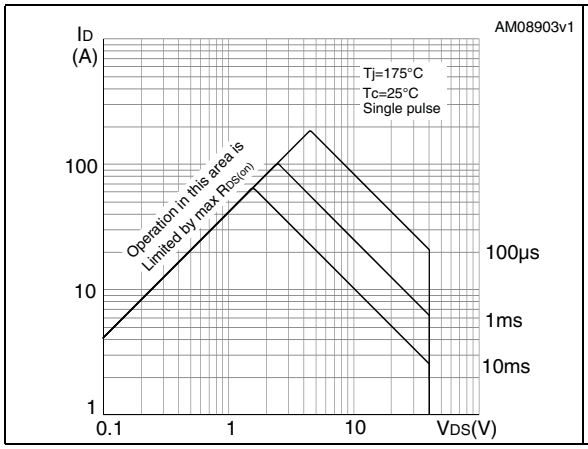


Figure 3. Thermal impedance

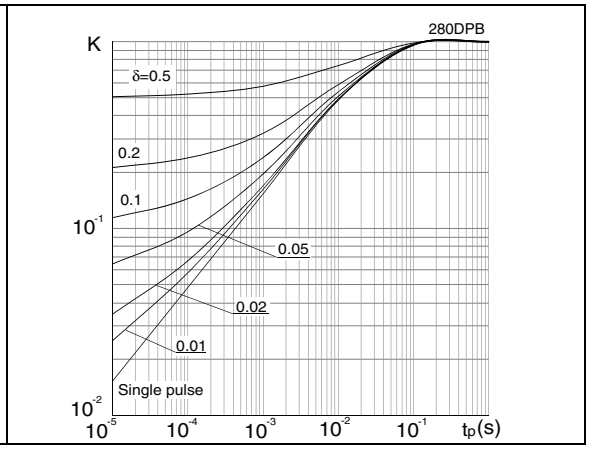


Figure 4. Output characteristics

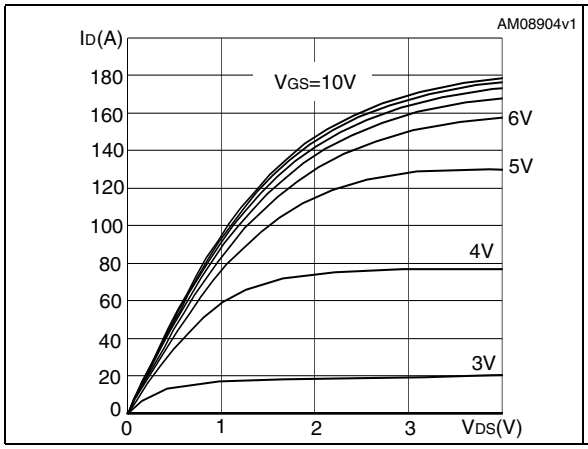


Figure 5. Transfer characteristics

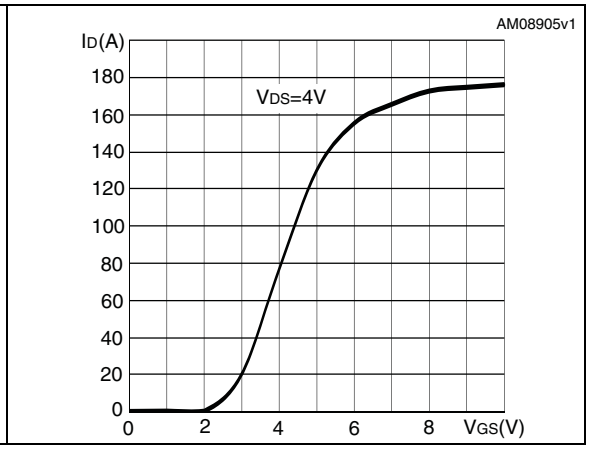


Figure 6. Normalized B_{VDSS} vs temperature

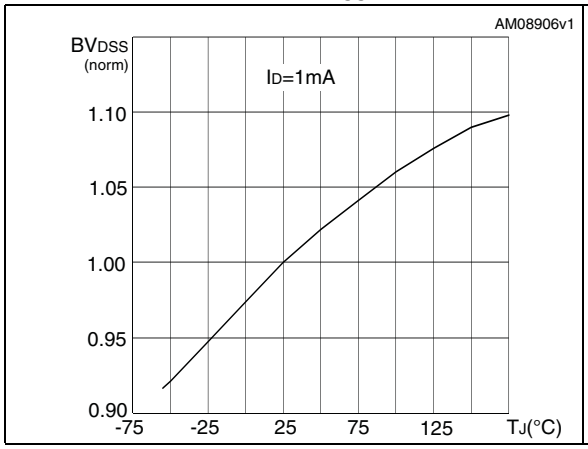


Figure 7. Static drain-source on resistance

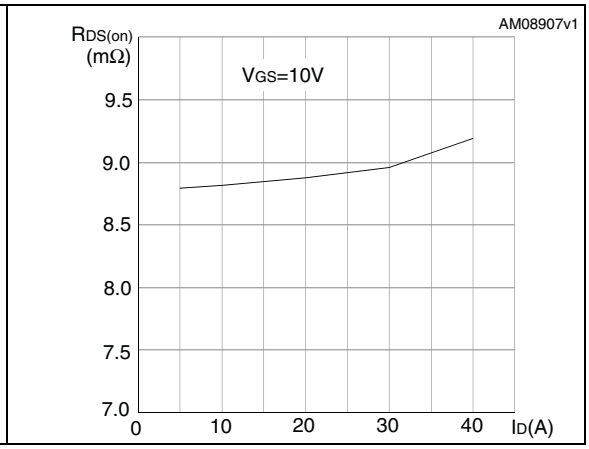


Figure 8. Gate charge vs gate-source voltage

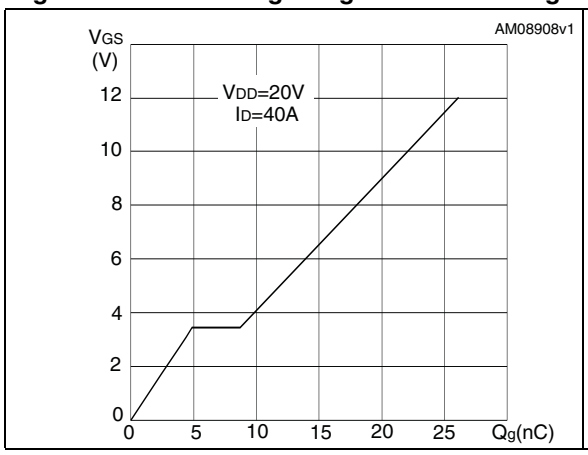


Figure 9. Capacitance variations

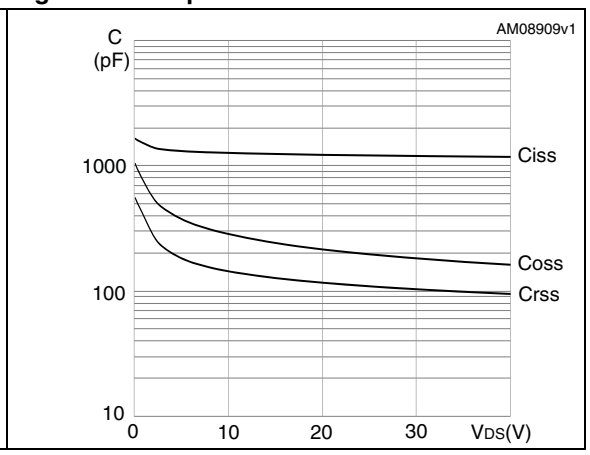


Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on resistance vs temperature

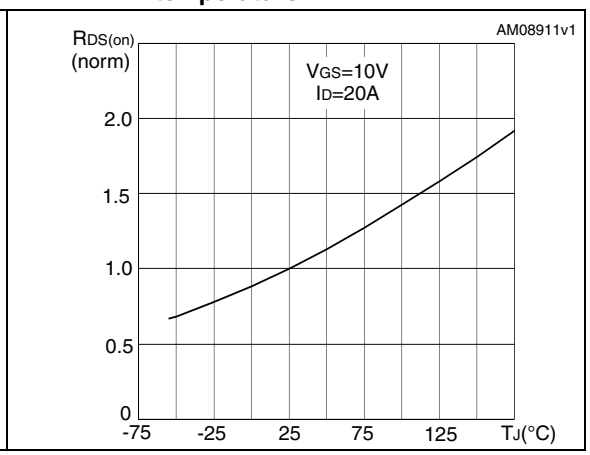
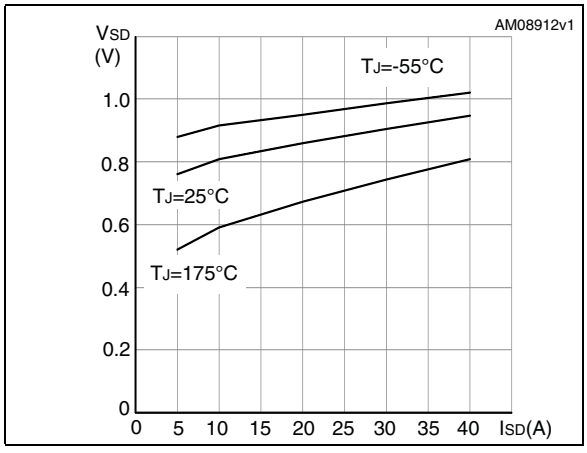


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

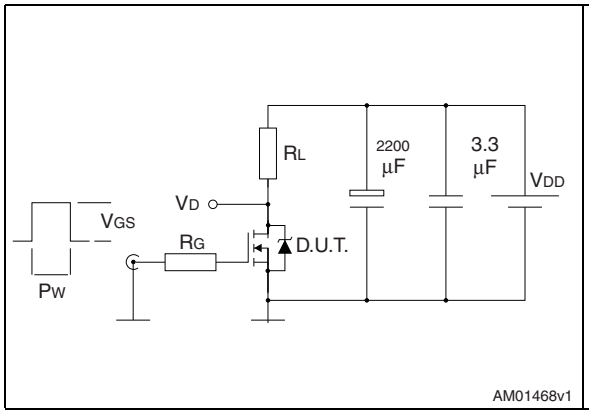


Figure 14. Gate charge test circuit

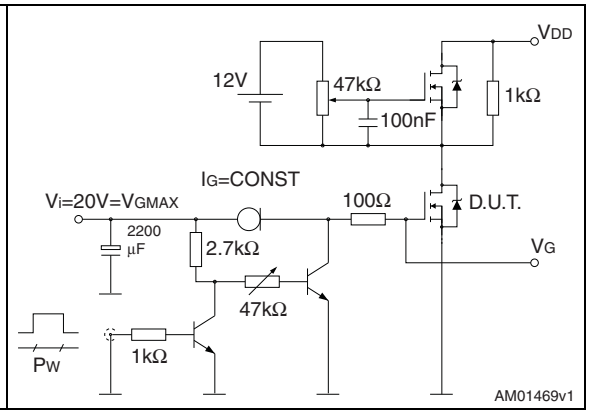


Figure 15. Test circuit for inductive load switching and diode recovery times

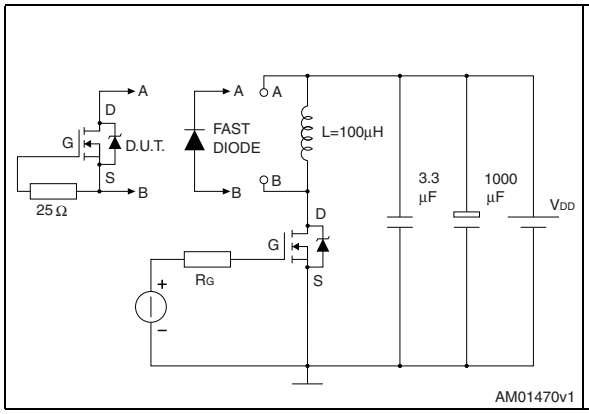


Figure 16. Unclamped inductive load test circuit

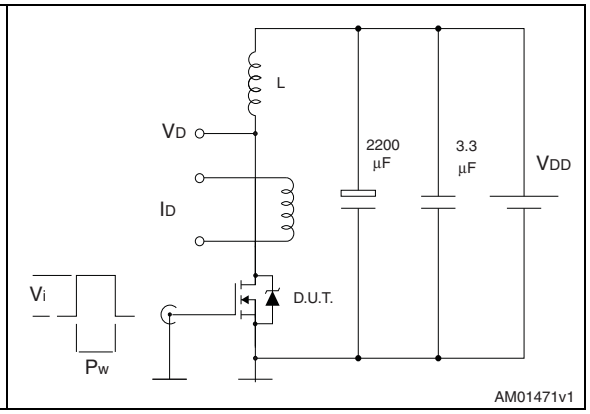


Figure 17. Unclamped inductive waveform

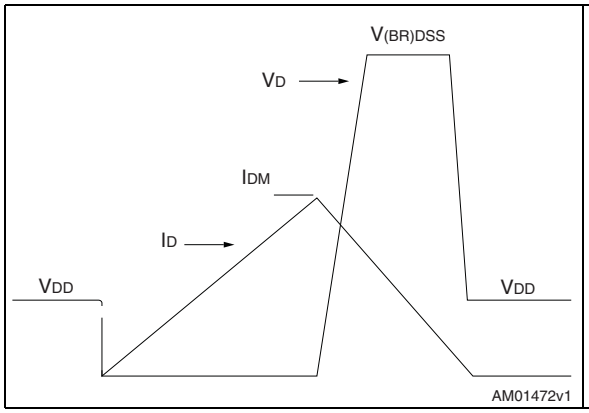
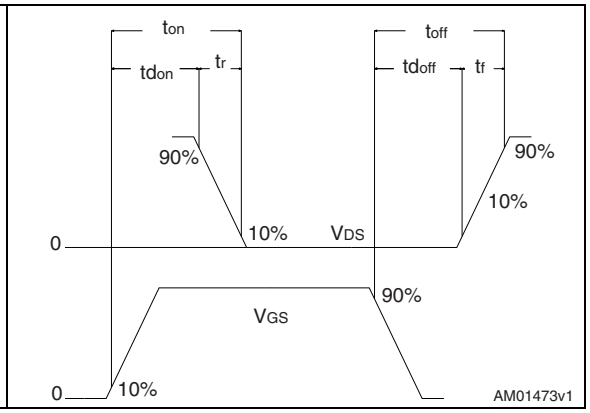


Figure 18. Switching time waveform



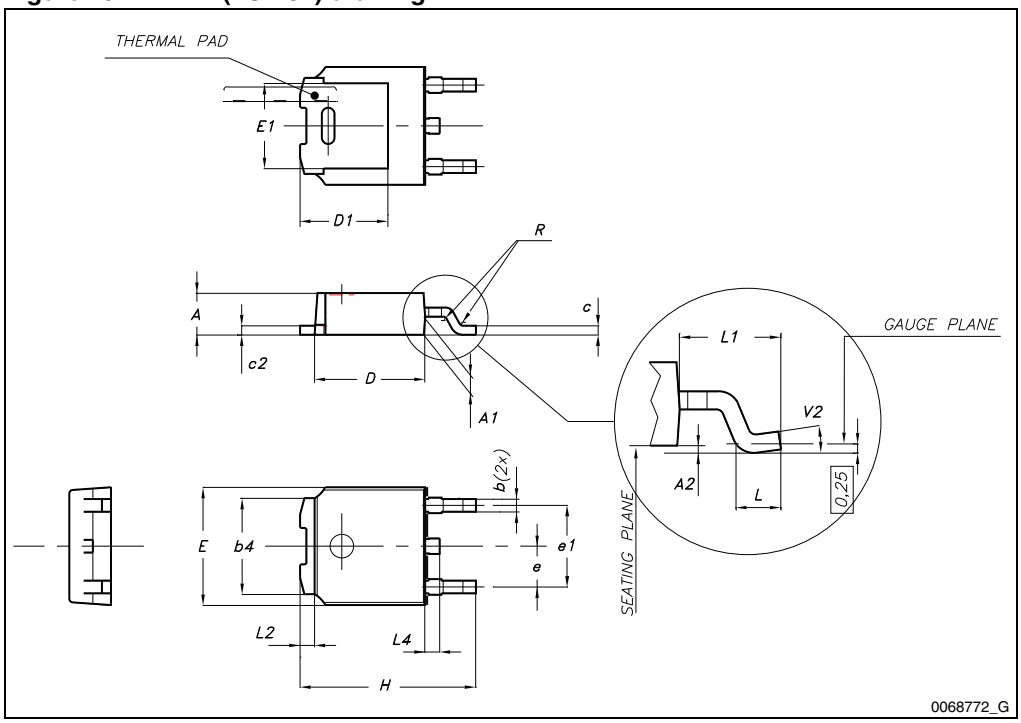
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and products status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 19. DPAK (TO-252) drawing

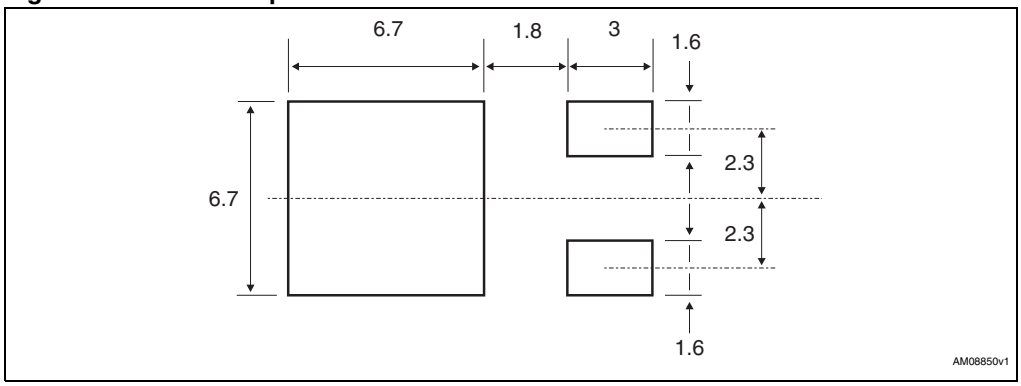


5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 20. DPAK footprint[a]



a. All dimension are in millimeters

Figure 21. Tape for DPAK (TO-252)

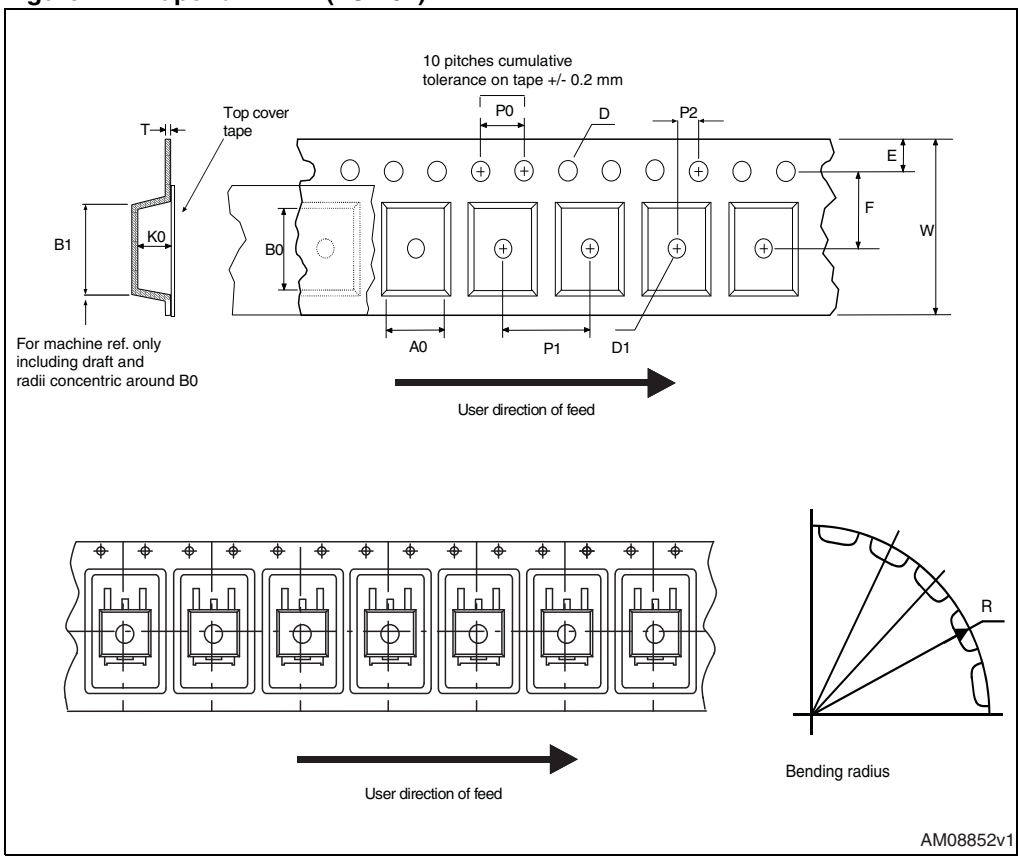
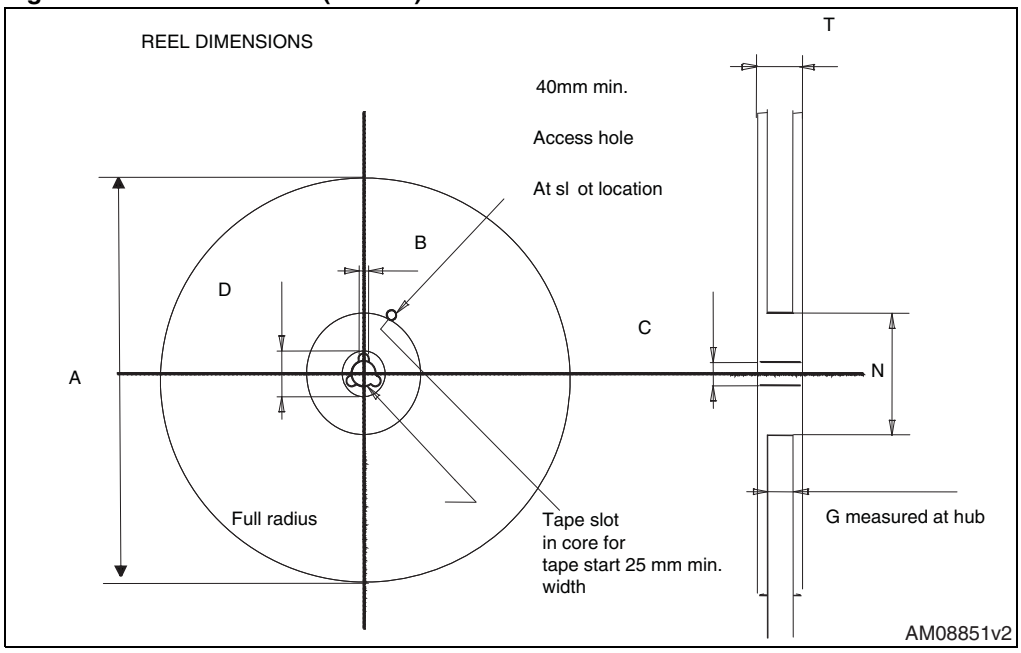


Figure 22. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
23-Feb-2010	1	First release.
03-Feb-2011	2	Document status promoted from preliminary data to datasheet.

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