



BUK661R8-30C

N-channel TrenchMOS intermediate level FET

Rev. 02 — 28 December 2010

Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	263	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 13	-	1.6	1.9	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; see Figure 14	-	11.1	13	mΩ



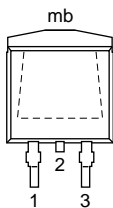
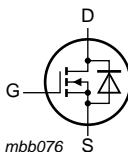
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^\circ\text{C}$; unclamped	-	-	0.87	J
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 24\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 17 ; see Figure 18	-	45	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK661R8-30C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	30	V
V_{GS}	gate-source voltage	DC [1]	-16	16	V
		Pulsed [2]	-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 [3]	-	120	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1 [3]	-	120	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ see Figure 3	-	1080	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	263	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$ [3]	-	120	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	1080	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 120\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped	-	0.87	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[4] [5] [6]	-	J

[1] -16V accumulated duration not to exceed 168 hrs.

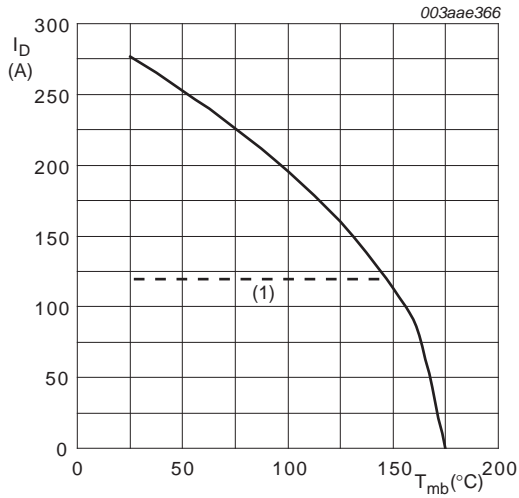
[2] Accumulated pulse duration not to exceed 5mins.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

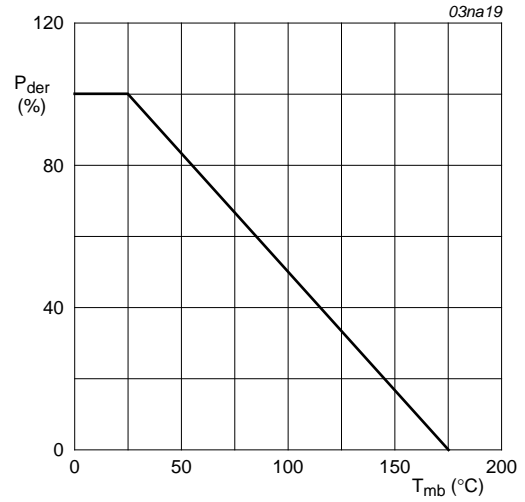
[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[6] Refer to application note AN10273 for further information.



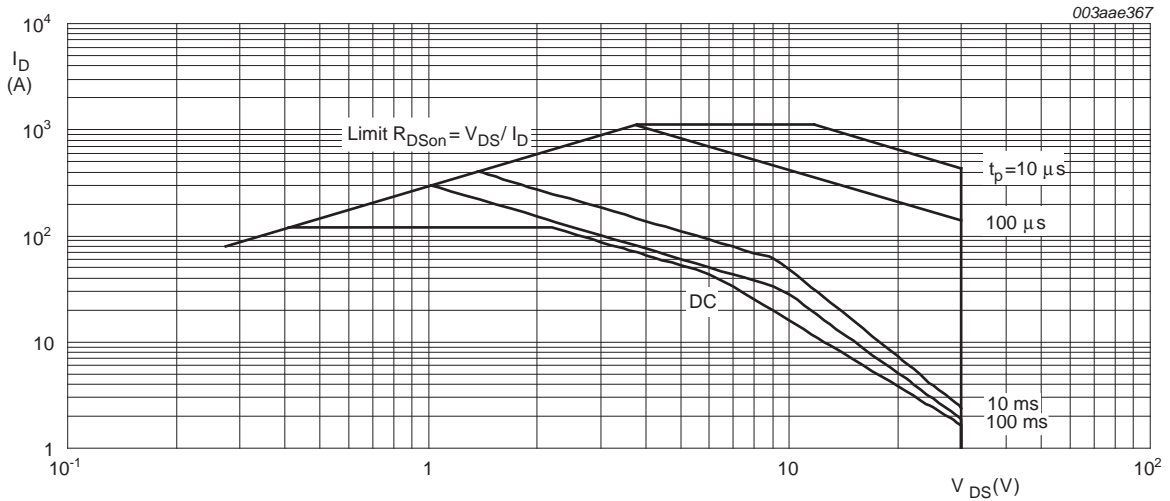
$V_{GS} \geq 10V$
 (1) Capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.57	K/W

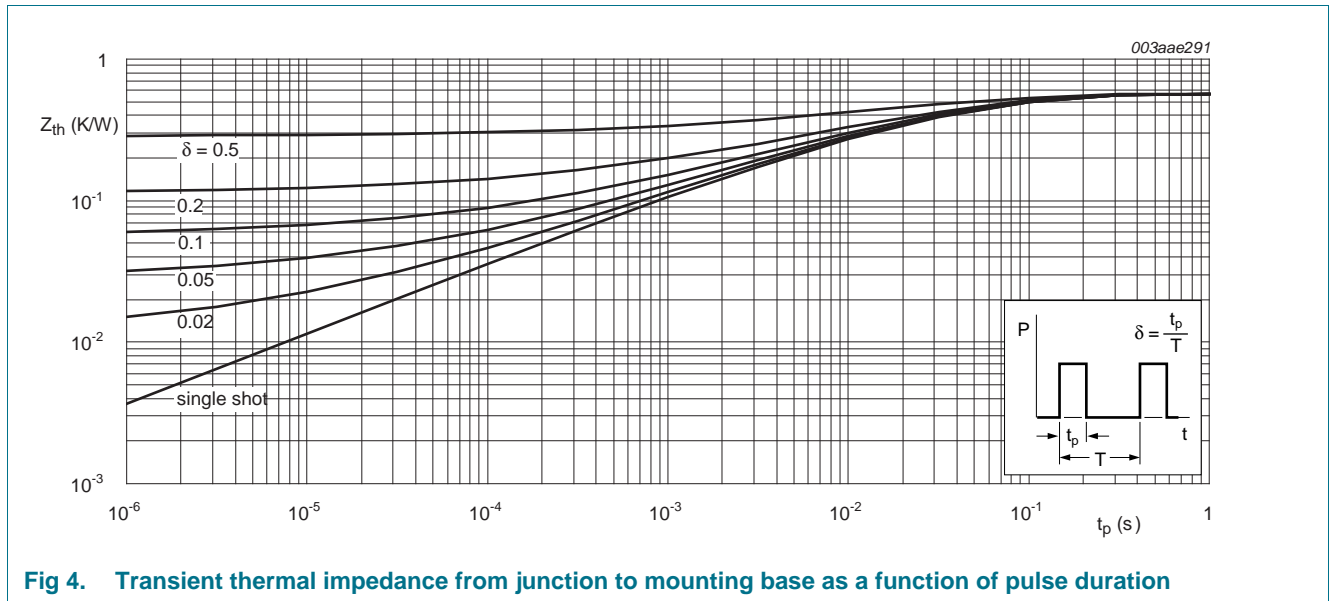


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

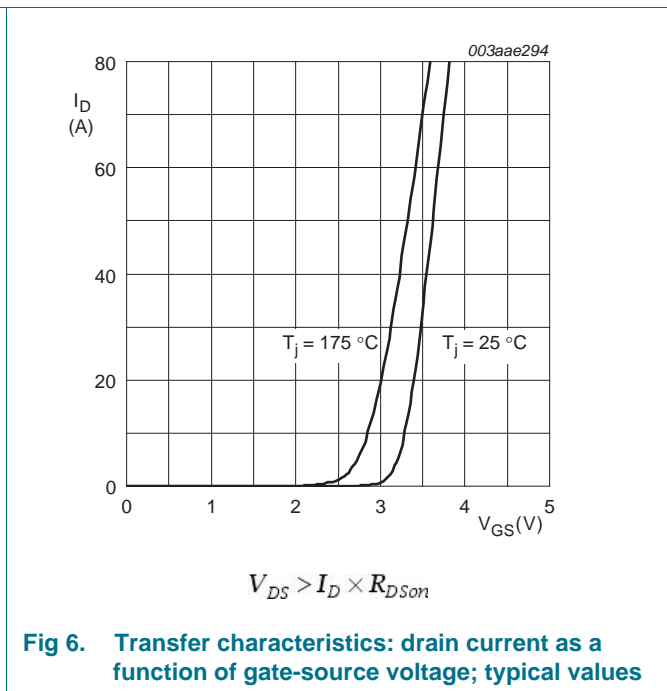
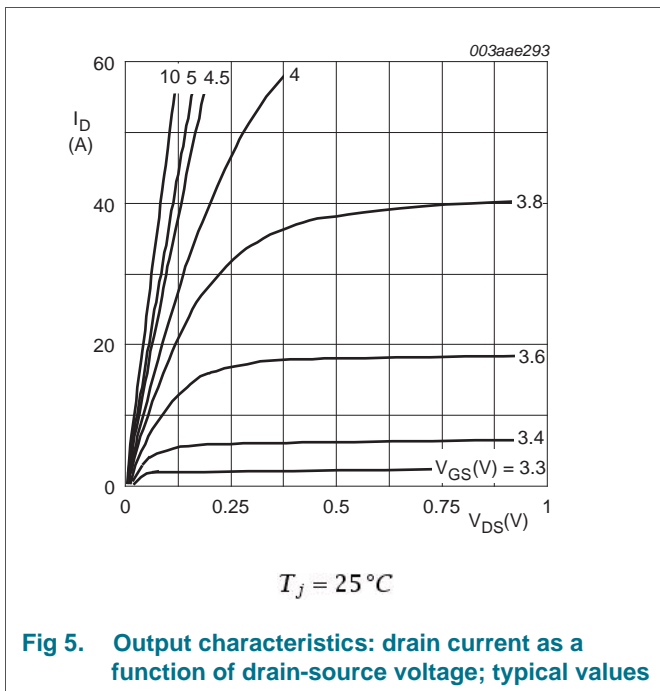
6. Characteristics

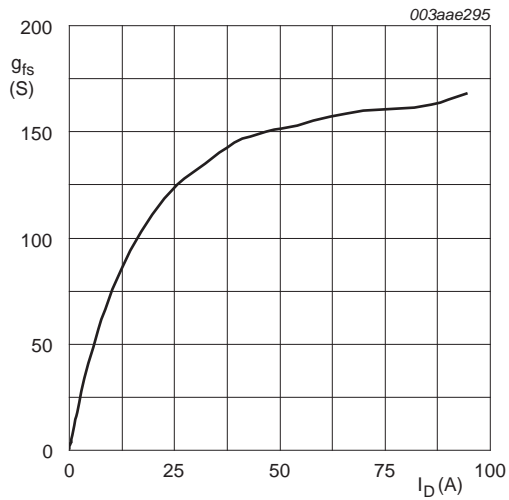
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
			27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10	1.8	2.3	2.8	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 10	-	-	3.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 11 ; see Figure 12	1.1	1.5	2	V
		$I_D = 2.5 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 10	0.8	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 13	-	1.6	1.9	m Ω
		$V_{GS} = 5 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$; see Figure 14	-	11.1	13	m Ω
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 13	-	2.48	3.3	m Ω
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$; see Figure 14	-	11.4	12	m Ω
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$; see Figure 14	-	10	11.7	m Ω
		$V_{GS} = 5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 13	-	2.24	2.8	m Ω
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C$; see Figure 13 ; see Figure 15	-	-	3.6	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 45 A; V_{DS} = 15 V; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$; see Figure 16 ; see Figure 17	-	5.9	-	C
		$I_D = 25 A; V_{DS} = 24 V; V_{GS} = 5 V$; see Figure 17 ; see Figure 18	-	95	-	nC
		$I_D = 25 A; V_{DS} = 24 V; V_{GS} = 10 V$; see Figure 18 ; see Figure 17	-	168	-	nC
Q_{GS}	gate-source charge		-	27	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 A; V_{DS} = 24 V; V_{GS} = 10 V$; see Figure 17 ; see Figure 18	-	45	-	nC

Table 6. Characteristics ...continued

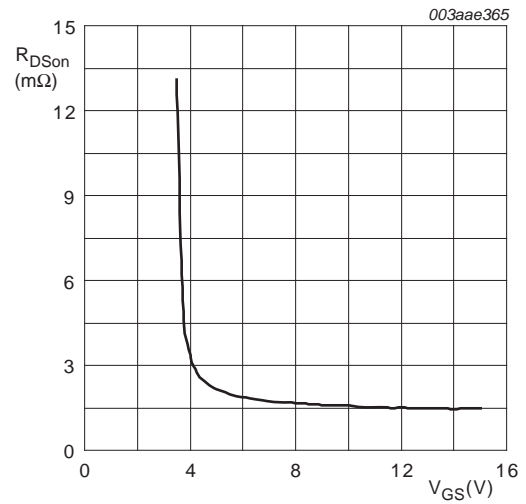
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ see Figure 19	-	8188	10918	pF
C_{oss}	output capacitance		-	1327	1592	pF
C_{rss}	reverse transfer capacitance		-	761	1042	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25\text{ V}; R_L = 1\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 10\ \Omega$	-	43	-	ns
t_r	rise time		-	93	-	ns
$t_{d(off)}$	turn-off delay time		-	272	-	ns
t_f	fall time		-	142	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die ; $T_j = 25\text{ }^\circ\text{C}$	-	3.5	-	nH
L_S	internal source inductance	from source lead to source bond pad ; $T_j = 25\text{ }^\circ\text{C}$	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 20	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 25\text{ V}$	-	62.7	-	ns
Q_r	recovered charge		-	115	-	nC





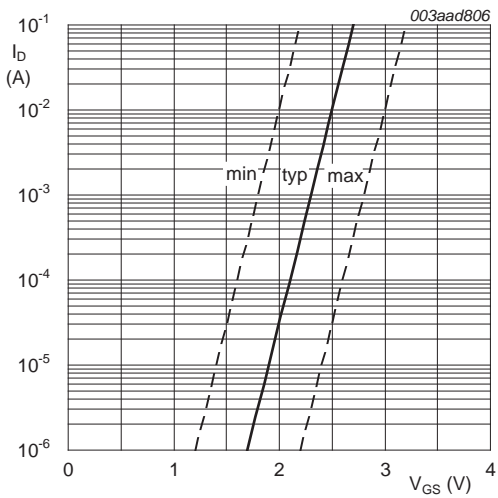
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 7. Forward transconductance as a function of drain current; typical values



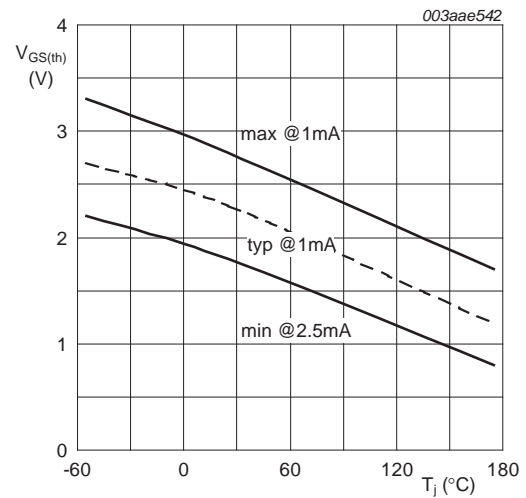
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values.



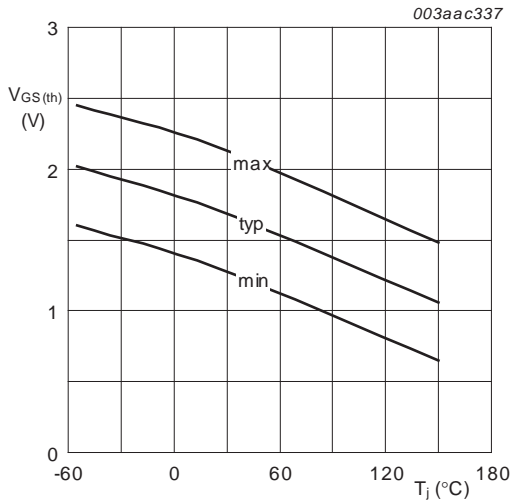
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



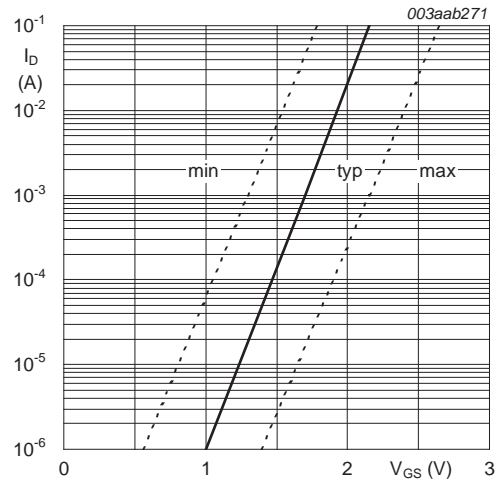
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



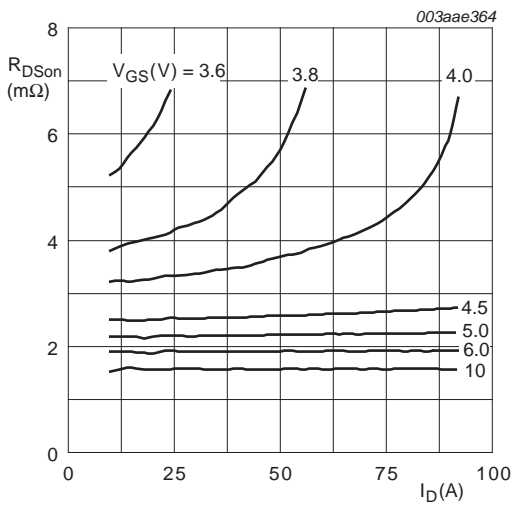
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



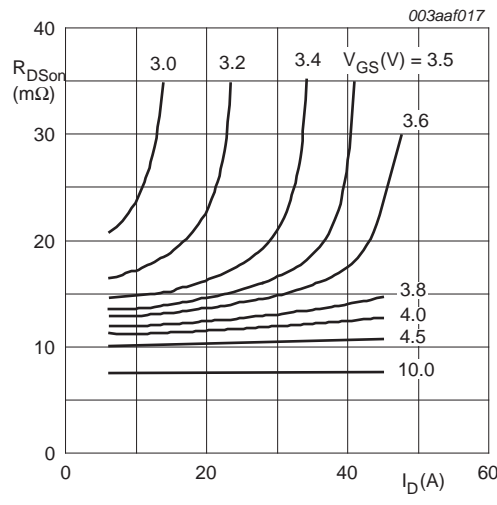
$T_j = 25\text{°C}; V_{DS} = 5\text{V}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



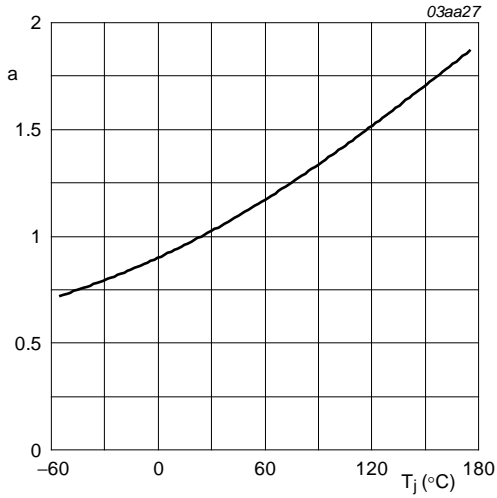
$T_j = 25\text{°C}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



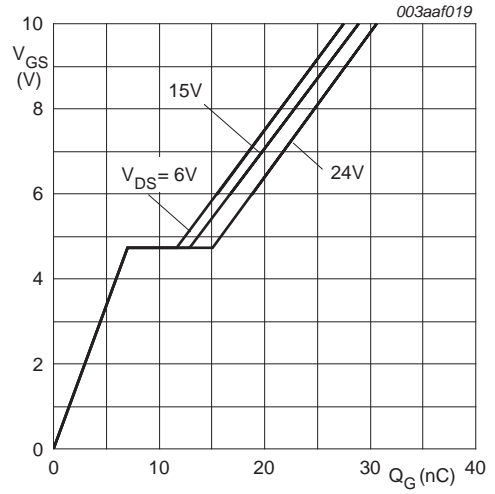
$T_j = 25\text{°C}$

Fig 14. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$

Fig 15. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$

Fig 16. Gate-source voltage as a function of gate charge; typical values

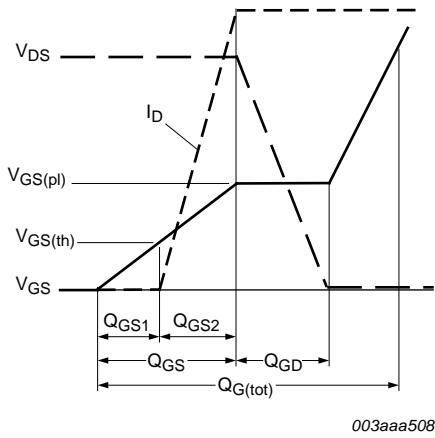
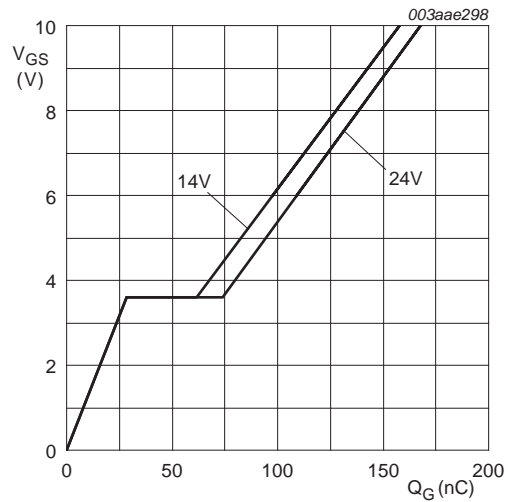
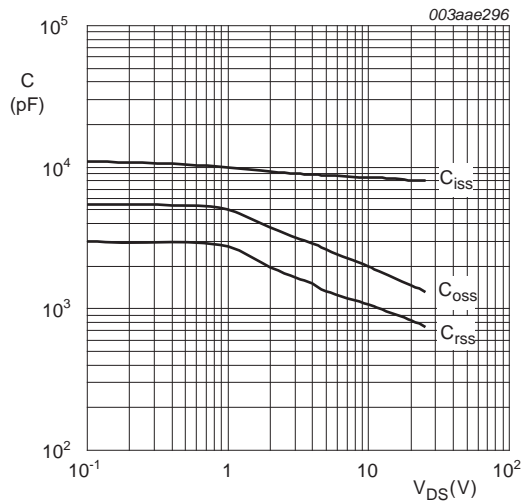


Fig 17. Gate charge waveform definitions



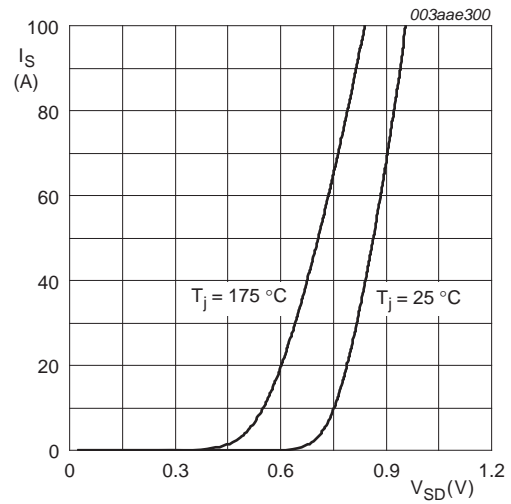
$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$

Fig 18. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 19. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 20. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

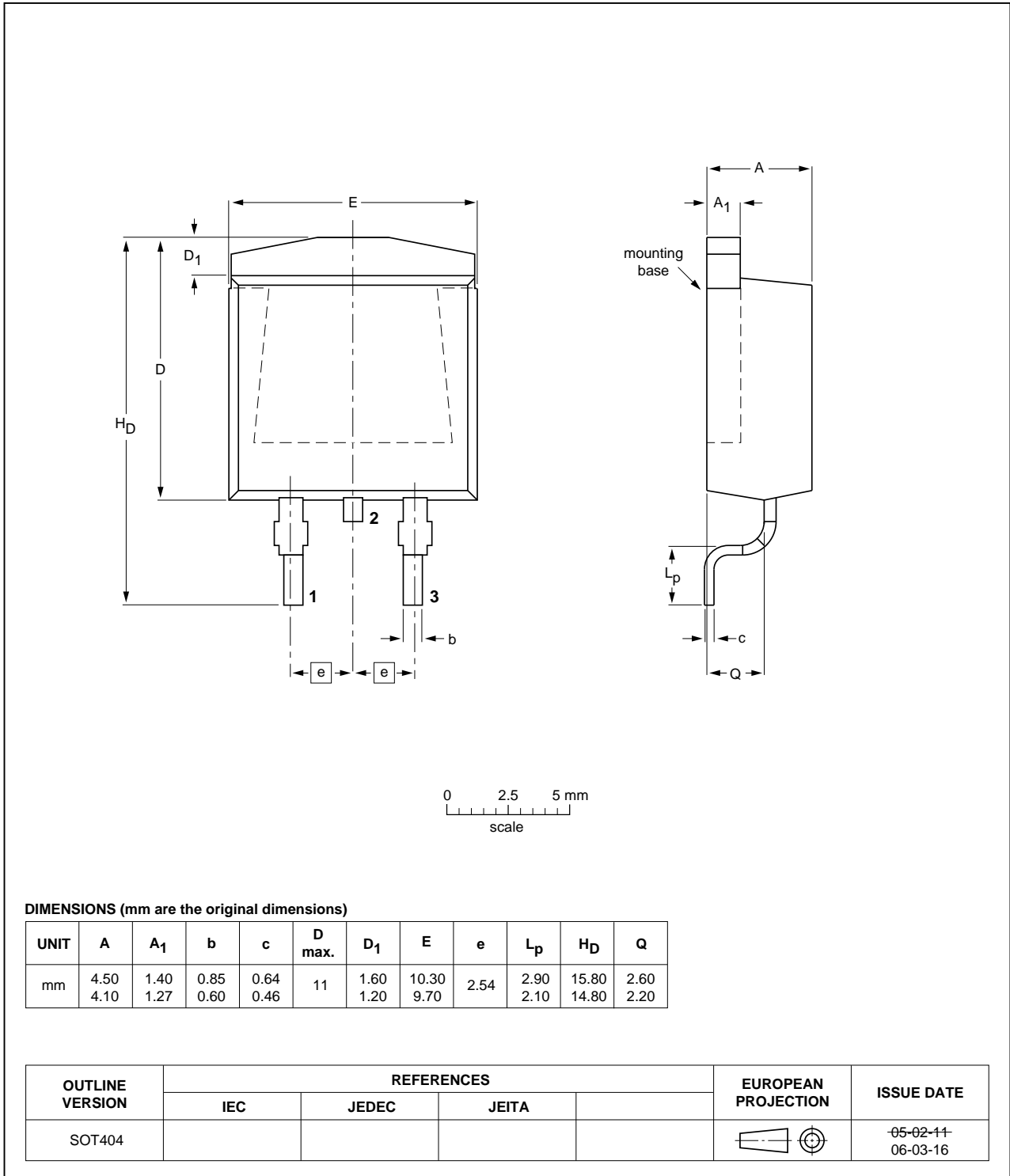


Fig 21. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK661R8-30C v.2	20101228	Product data sheet	-	BUK661R8-30C v.1
Modifications:	<ul style="list-style-type: none">• Data sheet status changed from Objective to Product.• Various changes to content.			
BUK661R8-30C v.1	20090323	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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