

PSMN9R0-30LL

N-channel QFN3333 30 V 9 mΩ logic level MOSFET

Rev. 04 — 7 July 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in QFN3333 package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and power supply equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources
- Small footprint for compact designs

1.3 Applications

- Battery protection
- Load switching
- DC-to-DC converters
- Power ORing

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	-	-	21	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	50	W
T_j	junction temperature		-55	-	150	°C

Static characteristics

$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A};$ $T_j = 25\text{ °C};$ see Figure 12	-	10.6	13	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A};$ $T_j = 100\text{ °C};$ see Figure 13	-	-	11.9	mΩ
		$V_{GS} = 10\text{ V}; I_D = 5\text{ A};$ $T_j = 25\text{ °C};$ see Figure 12	-	8	9	mΩ

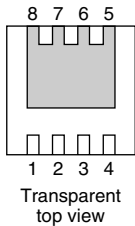
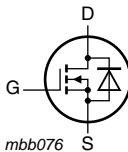


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 10\text{ A};$	-	2.9	-	nC
$Q_{G(\text{tot})}$	total gate charge	$V_{DS} = 15\text{ V};$ see Figure 14 ; see Figure 17	-	20.6	-	nC
		$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A};$ $V_{DS} = 15\text{ V};$ see Figure 17 ; see Figure 14	-	10	-	nC
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ }^\circ\text{C};$ $I_D = 40\text{ A}; V_{\text{sup}} \leq 30\text{ V};$ unclamped; $R_{GS} = 50\text{ } \Omega$	-	-	32	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>Transparent top view</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5,6,7,8	D	mounting base; connected to drain		

SOT873-1 (QFN3333)

3. Ordering information

Table 3. Ordering information

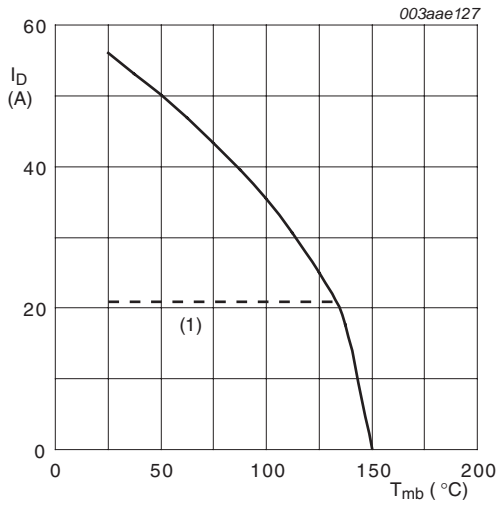
Type number	Package		Version
	Name	Description	
PSMN9R0-30LL	QFN3333	plastic thermal enhanced very thin small outline package; no leads; 8 terminals	SOT873-1

4. Limiting values

Table 4. Limiting values

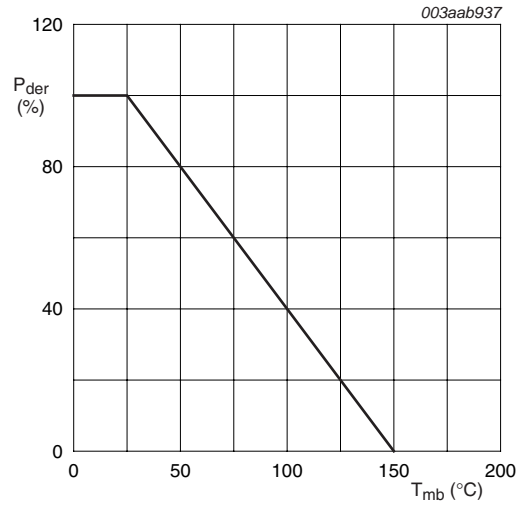
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \leq 150\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	21	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	21	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	226	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	50	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	21	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	226	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 40\text{ A}$; $V_{sup} \leq 30\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$	-	32	mJ



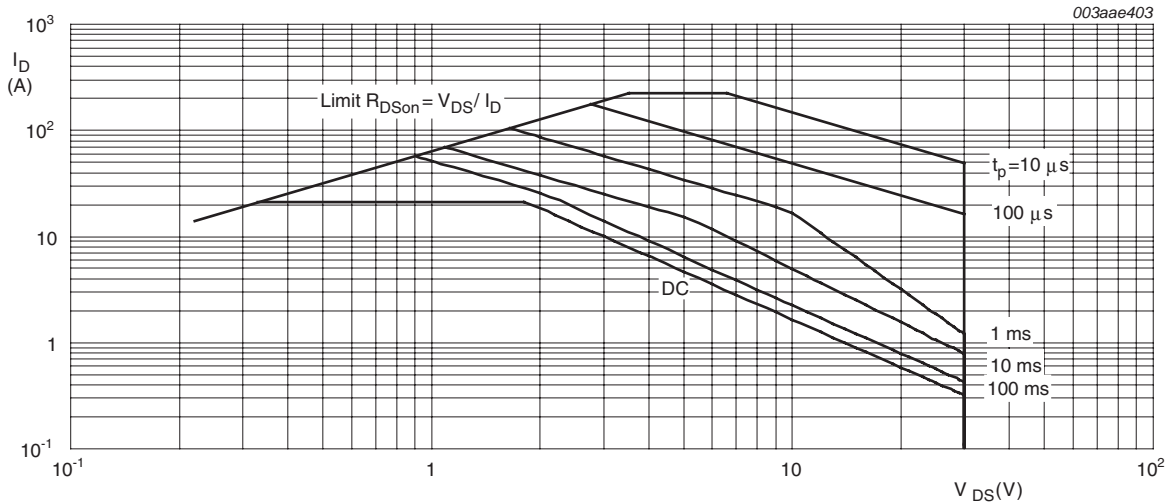
$V_{GS} \geq 10 \text{ V}$; (1) Capped at 21 A due to wires.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{mb} = 25 \text{ }^\circ\text{C}$; I_{DM} is single pulse

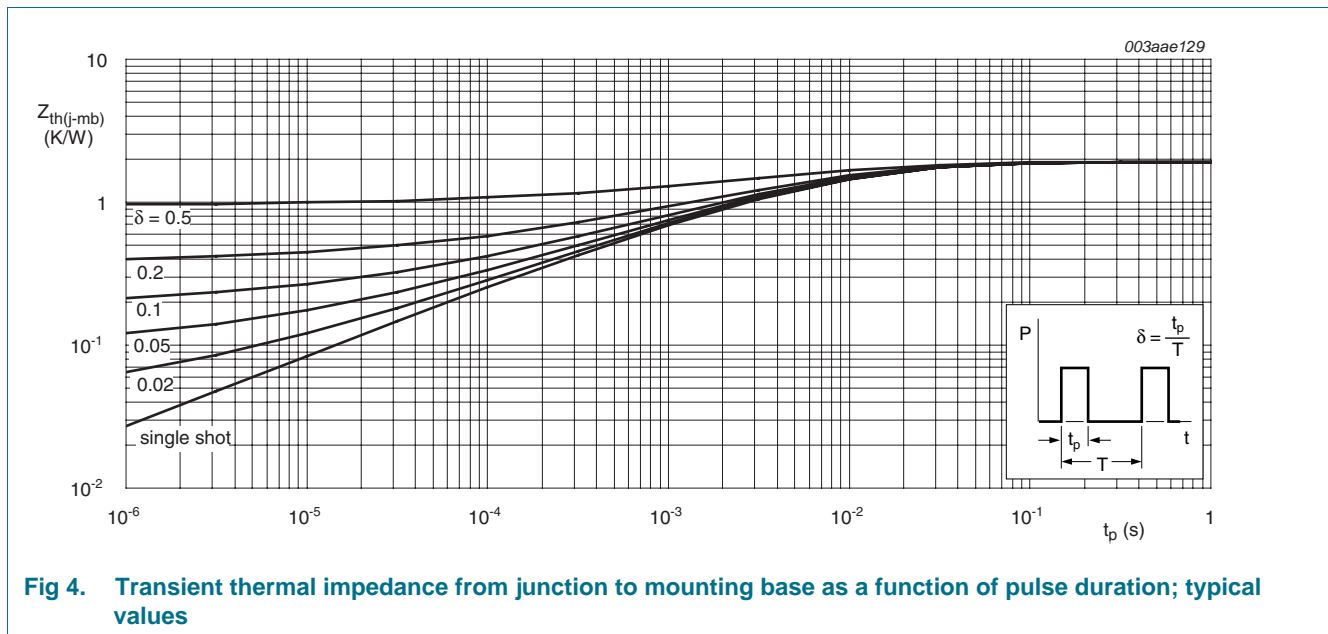
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1.9	4.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	55	60	K/W

[1] $R_{th(j-a)}$ is guaranteed by design and assumes that the device is mounted on a 40mm x 40mm x 70μm copper pad at 20°C ambient temperature. In practice $R_{th(j-a)}$ will be determined by the customer's PCB characteristics



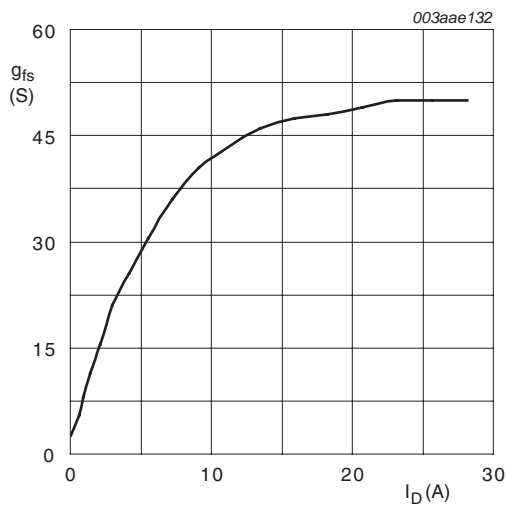
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 10	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 10	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	-	-	2.55	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	5	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12	-	10.6	13	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 13	-	-	11.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 13	-	14.4	16.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12	-	8	9	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1.46	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 17	-	20.6	-	nC
		$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 17 ; see Figure 14	-	10	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	18.6	-	nC
Q_{GS}	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	3.4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.4	-	nC
Q_{GD}	gate-drain charge	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 17	-	2.9	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V};$ see Figure 14 ; see Figure 17	-	2.6	-	V
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 15	-	1193	-	pF
C_{oss}	output capacitance		-	223	-	pF
C_{rss}	reverse transfer capacitance		-	106	-	pF

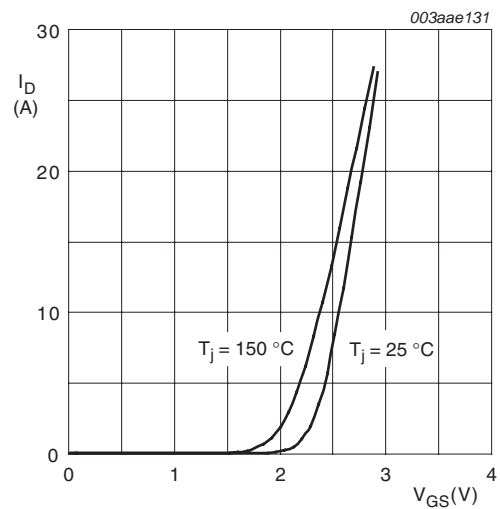
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 1.5\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 4.7\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	16	-	ns
t_r	rise time		-	18	-	ns
$t_{d(off)}$	turn-off delay time		-	22	-	ns
t_f	fall time		-	8	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 7.5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	30	-	ns
Q_r	recovered charge	$V_{DS} = 15\text{ V}$	-	22	-	nC



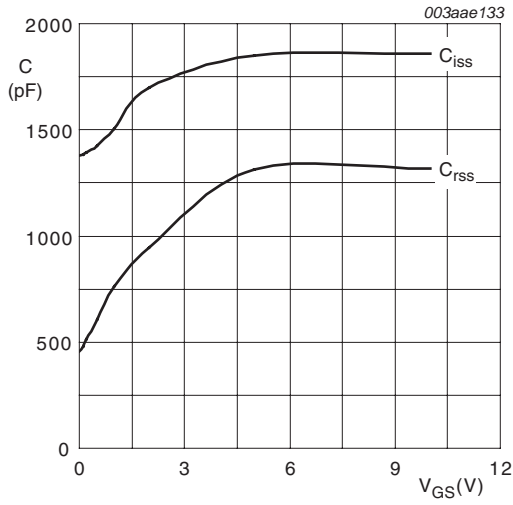
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 10\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



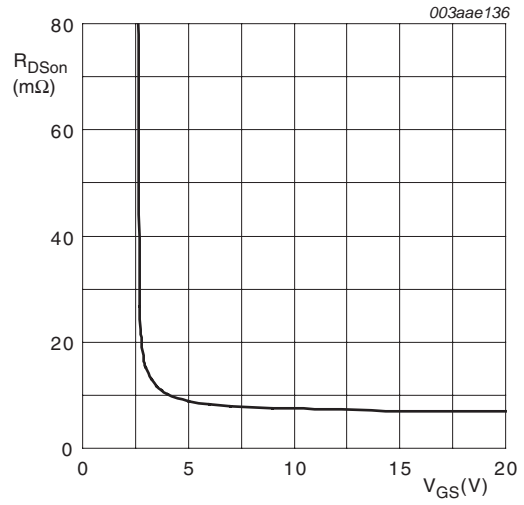
$V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



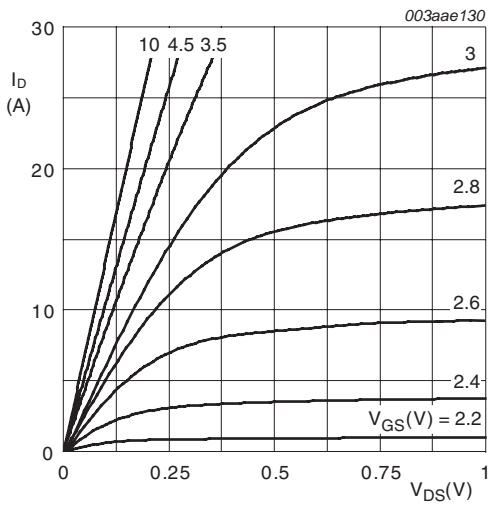
$V_{DS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage, typical values



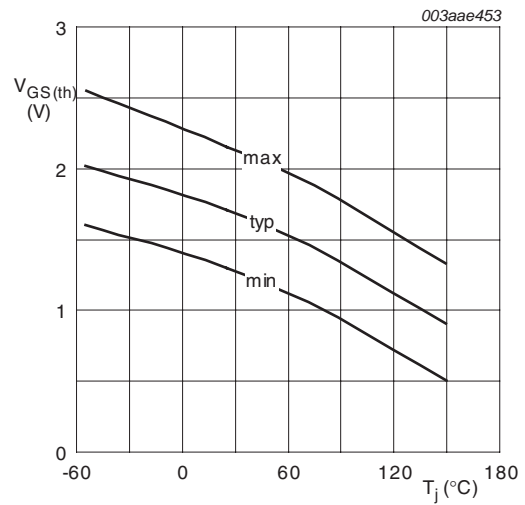
$T_j = 25 \text{ }^\circ\text{C}; I_D = 8 \text{ A}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



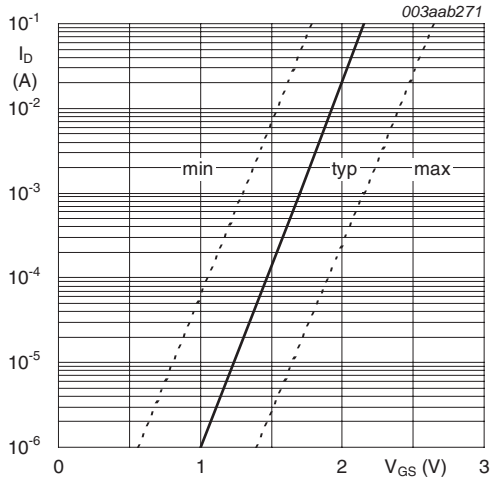
$T_j = 25 \text{ }^\circ\text{C}$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



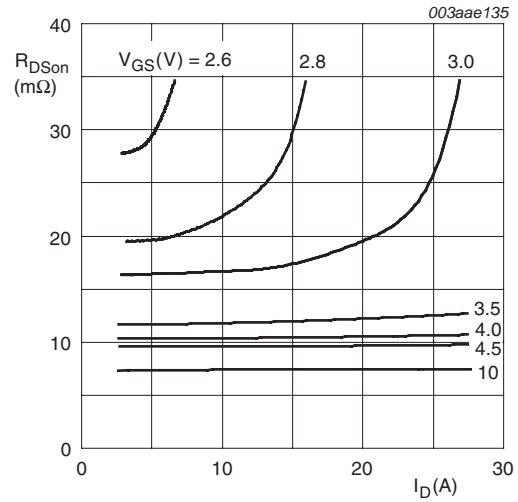
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



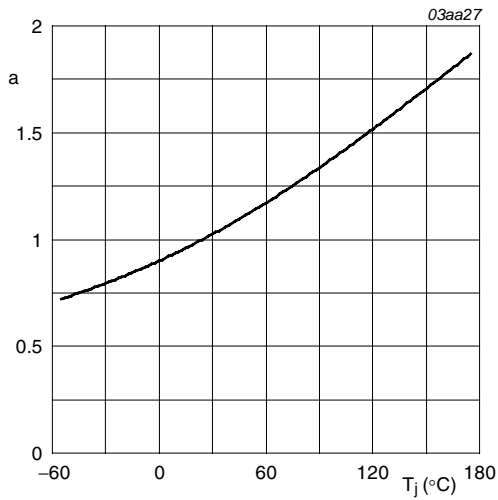
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



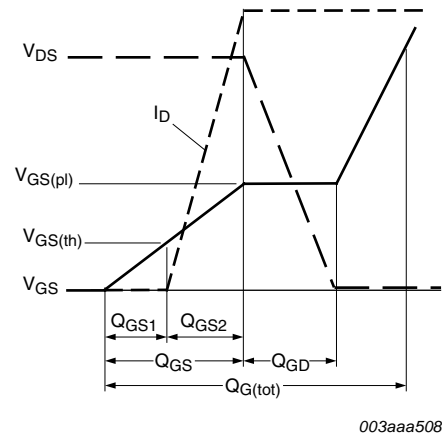
$T_j = 25^\circ\text{C}$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



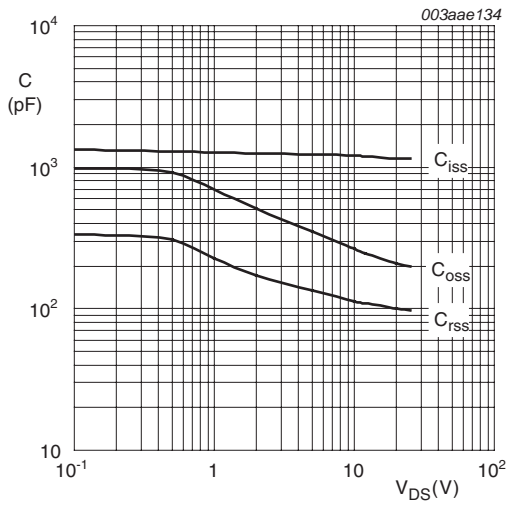
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



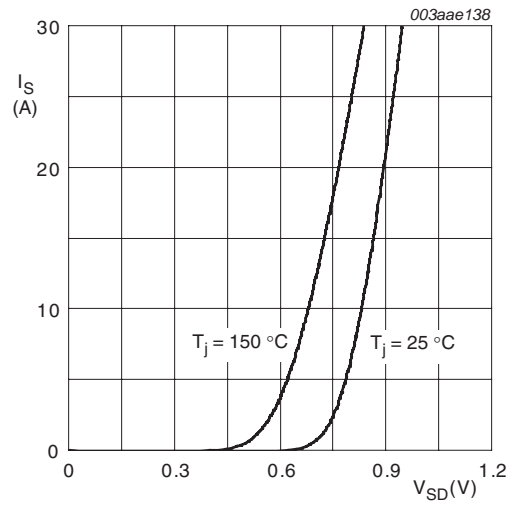
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Fig 14. Gate charge waveform definitions



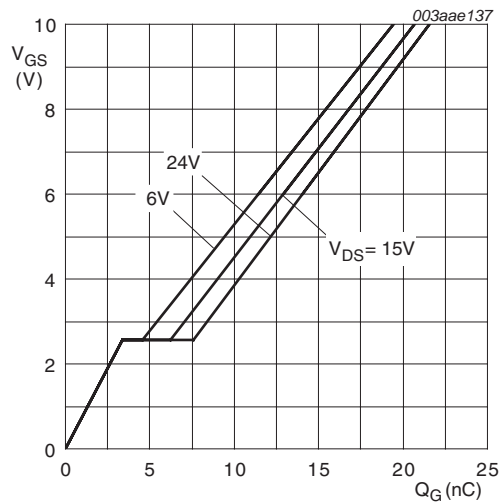
V_{GS} = 0 V; f = 1 MHz

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0V

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



T_j = 25 °C; I_D = 10 A

Fig 17. Gate-source voltage as a function of gate charge; typical values

7. Package outline

QFN3333: plastic thermal enhanced very thin small outline package; no leads;
8 terminals; body 3.3 x 3.3 x 1.0 mm

SOT873-1

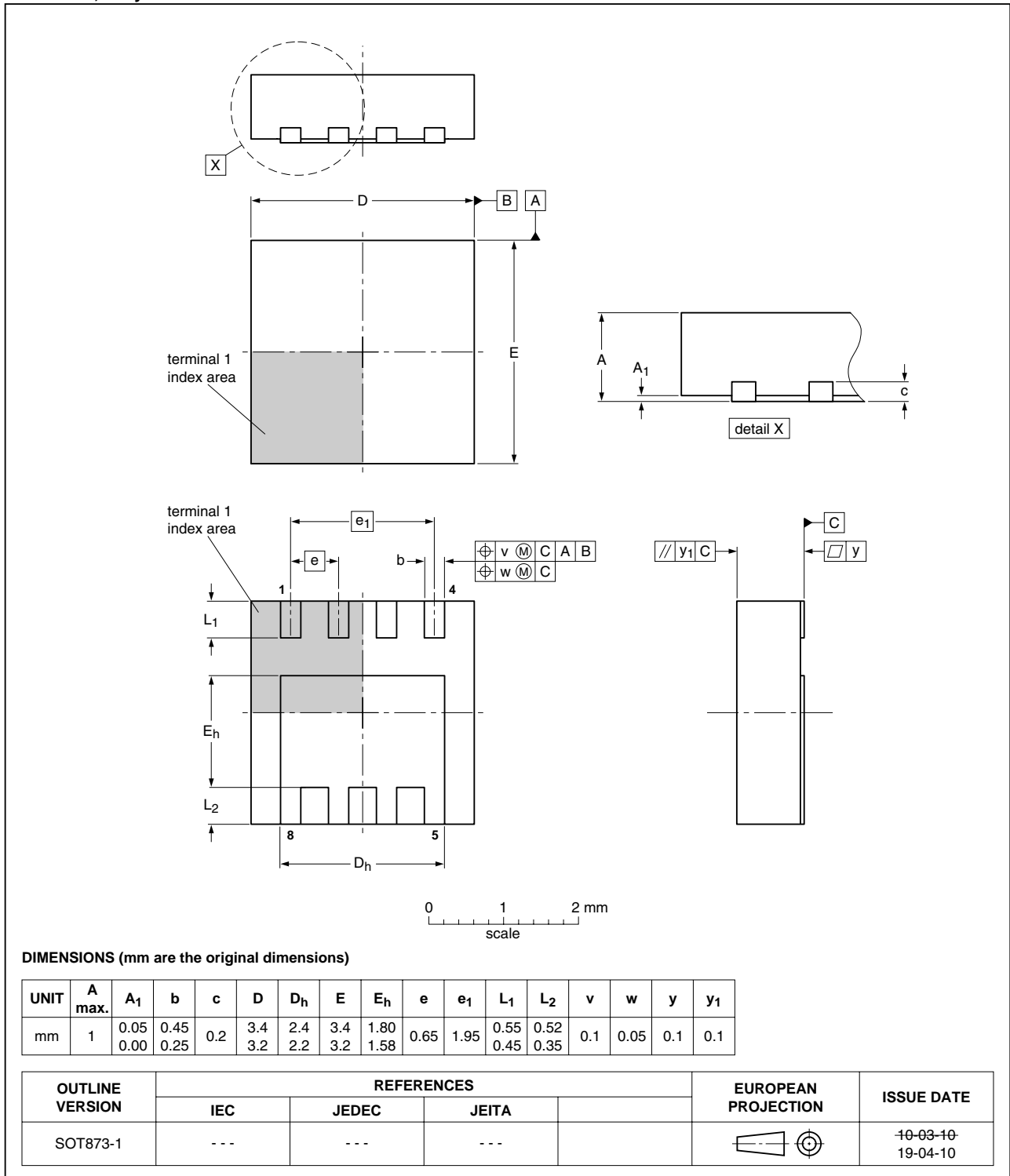


Fig 18. Package outline SOT873-1 (QFN3333)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R0-30LL v.4	20100707	Product data sheet	-	PSMN9R0-30LL v.3
Modifications:	• Status changed from preliminary to product.			
PSMN9R0-30LL v.3	20100623	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 7 July 2010

Document identifier: PSMN9R0-30LL