

8MHz, 64-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

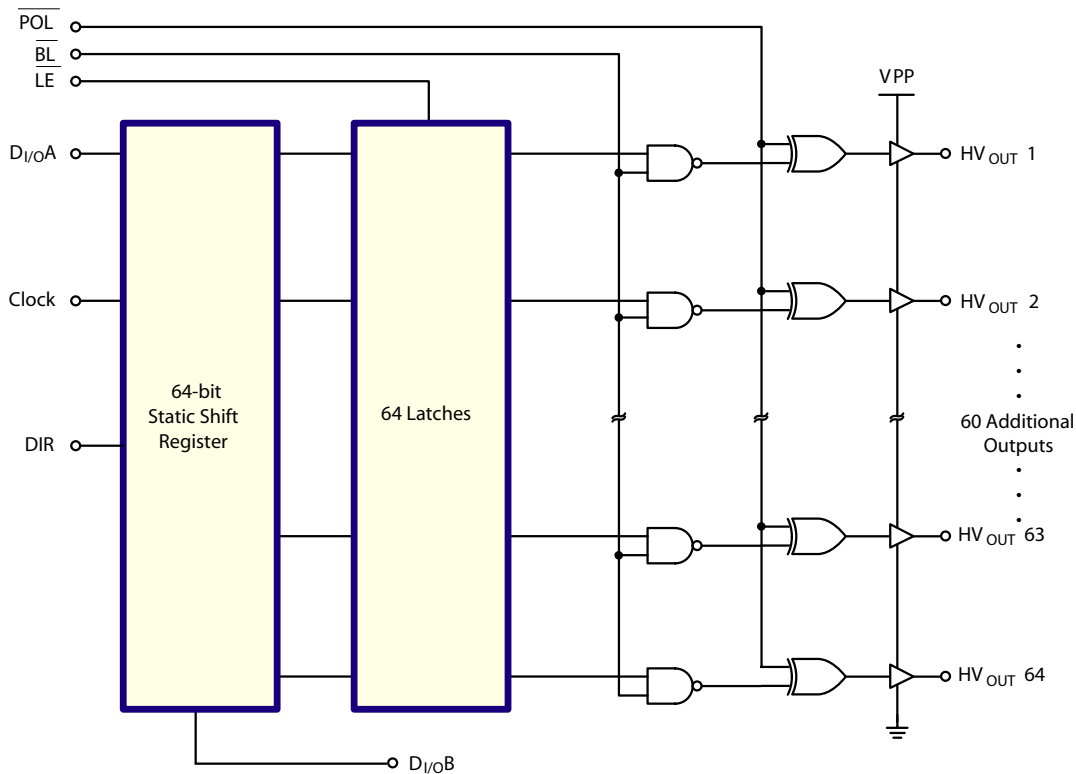
- ▶ HVCMOS® technology
- ▶ 5.0V CMS Logic
- ▶ Output voltage up to +80V
- ▶ Low power level shifting
- ▶ 8.0MHz data rate
- ▶ Latched data outputs
- ▶ Forward and reverse shifting options (DIR pin)
- ▶ Diode to VPP allows efficient power recovery
- ▶ Outputs may be hot switched
- ▶ Hi-Rel processing available

General Description

The HV57908 is a low voltage serial to high voltage parallel converter with push-pull outputs. The device has been designed for use as a driver for EL displays. It can also be used in any application requiring multiple output high voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device consists of a 64-bit shift register, 64 latches and control logic to perform the polarity select and blanking of the outputs. HV_{OUT1} is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to VDD. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HV_{OUT64}). Operation of the shift register is not affected by the \overline{LE} (latch enable), \overline{BL} (blanking), or the \overline{POL} (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the \overline{LE} input is high. The data in the latches is stored when the \overline{LE} is low.

Functional Block Diagram



Ordering Information

Device	Package Options
	80-Lead PQFP 20.00x14.00mm body 3.40mm height (max) 0.80mm pitch
HV57908	HV57908PG-G

-G indicates package is RoHS compliant ("Green")



Absolute Maximum Ratings

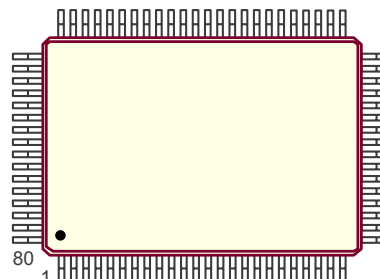
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +7.5V
Output voltage, V_{PP}	-0.5V to +90V
Logic input levels	-0.3V to $V_{DD} + 0.3V$
Ground current ¹	1.5A
Continuous total power dissipation ²	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature ³	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

- Limited by the total dissipated in the package.
- For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.
- 1.6mm (1/16inch) from case for 10 seconds

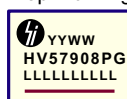
Pin Configuration



80-Lead PQFP (PG)
(top view)

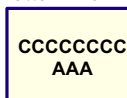
Product Marking

Top Marking



YY = Year Sealed
 WW = Week Sealed
 L = Lot Number
 C = Country of Origin*
 A = Assembler ID*
 — = "Green" Packaging

Bottom Marking



80-Lead PQFP (PG)

*May be part of top marking

Recommended Operating Conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output voltage	8.0	80	V
V_{IH}	High-level input voltage	$V_{DD} - 0.5$	-	V
V_{IL}	Low-level input voltage	0	0.5	V
f_{CLK}	Clock frequency per register	-	8.0	MHz
T_A	Operating free-air temperature	-40	+85	°C

Notes:

Power-up sequence should be the following:

- Apply ground
- Apply V_{DD}
- Set all inputs (Data, CLK, Enable, etc.) to a known state
- Apply V_{PP}
- The V_{PP} should not drop below V_{DD} or float during operation

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics (Over recommended operating conditions unless otherwise noted, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Sym	Parameter	Min	Max	Units	Conditions	
I_{DD}	V_{DD} supply current	-	15	mA	$V_{DD} = V_{DD} \text{ max, } f_{CLK} = 8.0\text{MHz}$	
I_{PP}	High voltage supply current	-	100	μA	Outputs high	
		-	100	μA	Outputs low	
I_{DDQ}	Quiescent V_{DD} supply current	-	100	μA	All $V_{IN} = V_{DD}$	
V_{OH}	High level output	HV_{OUT}	65	-	V	$I_O = -15\text{mA, } V_{PP} = +80\text{V}$
		D_{OUT}	$V_{DD} - 0.5\text{V}$	-	V	$I_O = -100\mu\text{A}$
V_{OL}	Low level output	HV_{OUT}	-	7.0	V	$I_O = +12\text{mA, } V_{PP} = +80\text{V}$
		D_{OUT}	-	0.5	V	$I_O = 100\mu\text{A}$
I_{IH}	High-level logic input current	-	1.0	μA	$V_{IH} = V_{DD}$	
I_{IL}	Low-level logic input current	-	-1.0	μA	$V_{IL} = 0\text{V}$	
V_{OC}	High voltage clamp diode	-	1.0	V	$I_{OC} = 1.0\text{mA}$	

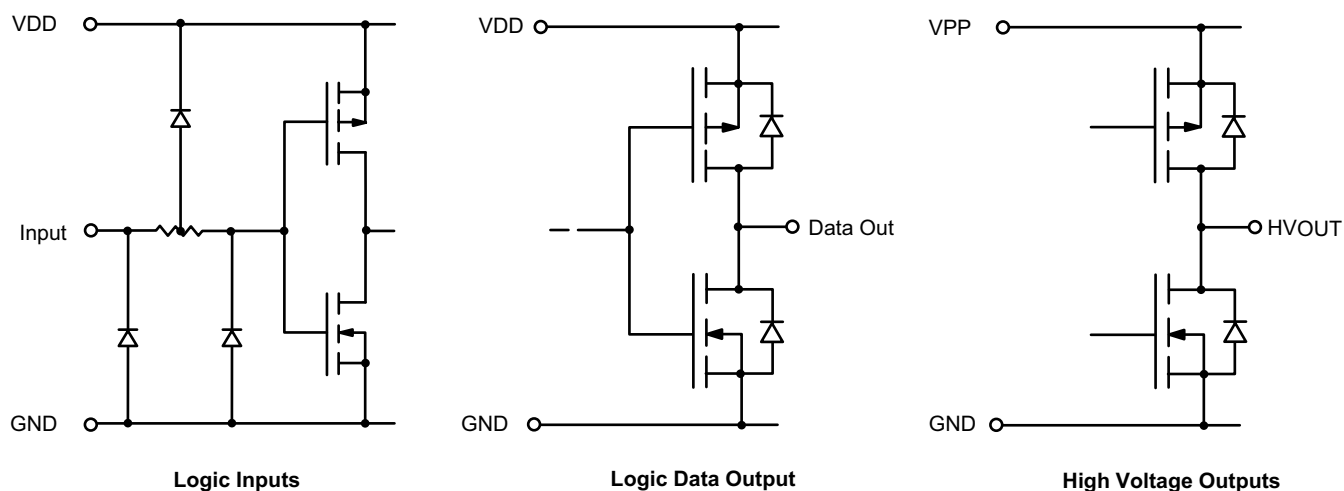
AC Electrical Characteristics ($T_A = +85^\circ\text{C}$ max. Logic signal inputs and data inputs have $t_r, t_f \leq 5.0\text{ns}$ [10% and 90% points])

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	Per register
t_{WL}, t_{WH}	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	10	-	ns	---
t_H	Data hold time after clock rises	15	-	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	-	500	ns	$C_L = 15\text{pF}$
t_{DHL}	Delay time clock to data high to low	-	70	ns	$C_L = 15\text{pF}$
t_{DLH}	Delay time clock to data low to high	-	70	ns	$C_L = 15\text{pF}$
t_{DLE}^*	Delay time clock to \overline{LE} low to high	25	-	ns	---
t_{WLE}	\overline{LE} pulse width	25	-	ns	---
t_{SLE}	\overline{LE} set-up time before clock rises	0	-	ns	---

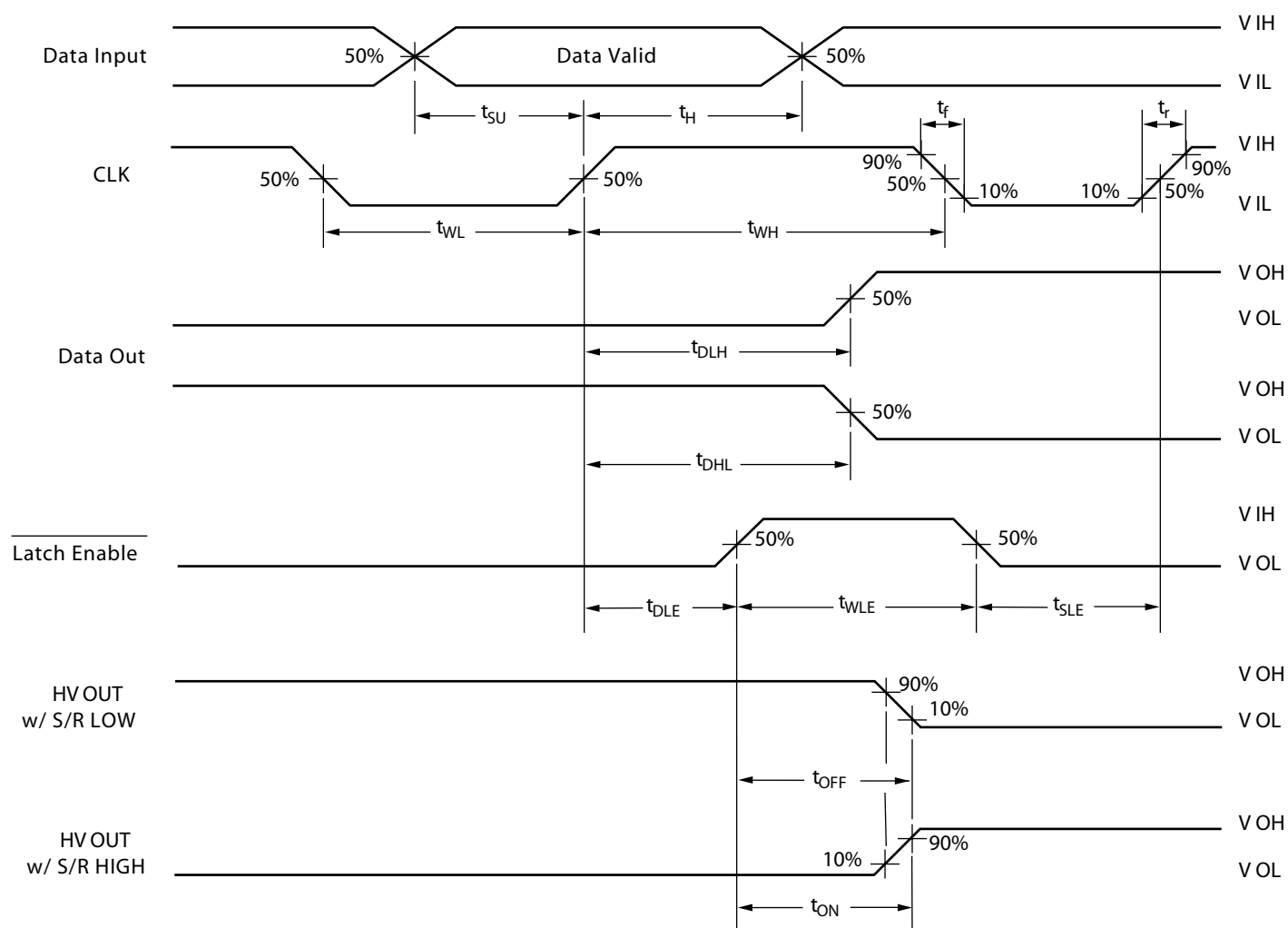
Note:

* t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).

Input and Output Equivalent Circuits



Switching Waveforms



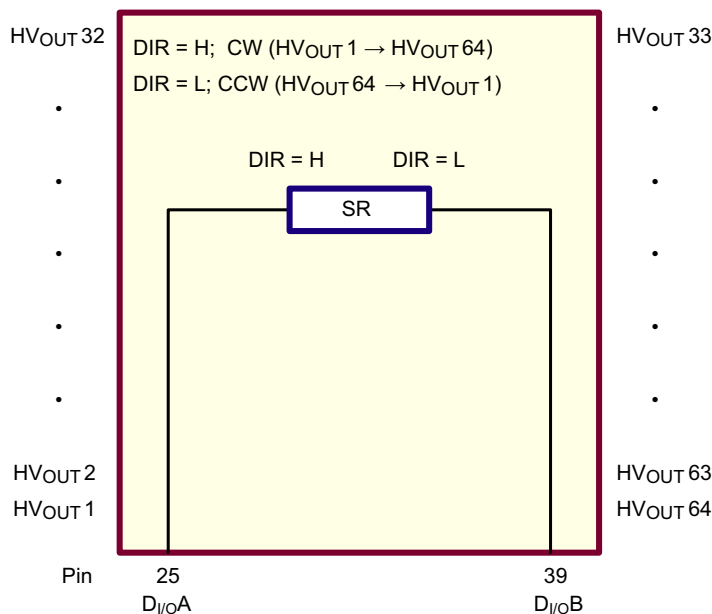
Function Table

Function	Inputs						Outputs		
	Data	CLK	\overline{LE}	\overline{BL}	\overline{POL}	DIR	Shift Reg	HV Outputs	Data Out
All O/P high	X	X	X	L	L	X	-	H	-
All O/P low	X	X	X	L	H	X	-	L	-
O/P normal	X	X	X	H	H	X	-	No inversion	-
O/P inverted	X	X	X	H	L	X	-	Inversion	-
Data falls through (latches transparent)	L	$\text{--}\uparrow\text{--}$	H	H	H	X	L	L	-
	H	$\text{--}\uparrow\text{--}$	H	H	H	X	H	H	-
	L	$\text{--}\uparrow\text{--}$	H	H	L	X	L	H	-
	H	$\text{--}\uparrow\text{--}$	H	H	L	X	H	L	-
Data stored/ latches loaded	X	X	L	H	H	X	*	Stored Data	-
	X	X	L	H	L	X	*	Inversion of stored data	-
I/O relation	$D_{I/OA}$	$\text{--}\uparrow\text{--}$	X	X	X	H	$Q_N \rightarrow Q_{N+1}$	-	$D_{I/OB}$
	$D_{I/OB}$	$\text{--}\uparrow\text{--}$	X	X	X	L	$Q_N \rightarrow Q_{N-1}$	-	$D_{I/OA}$

Notes:

* = dependent upon previous stage's state.

Shift Register Operation



Pin Function

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HV _{OUT} 24/41	21	HV _{OUT} 4/61	41	HV _{OUT} 64/1	61	HV _{OUT} 44/21
2	HV _{OUT} 23/42	22	HV _{OUT} 3/62	42	HV _{OUT} 63/2	62	HV _{OUT} 43/22
3	HV _{OUT} 22/43	23	HV _{OUT} 2/63	43	HV _{OUT} 62/3	63	HV _{OUT} 42/23
4	HV _{OUT} 21/44	24	HV _{OUT} 1/64	44	HV _{OUT} 61/4	64	HV _{OUT} 41/24
5	HV _{OUT} 20/45	25	D _{IO} A	45	HV _{OUT} 60/5	65	HV _{OUT} 40/25
6	HV _{OUT} 19/46	26	N/C	46	HV _{OUT} 59/6	66	HV _{OUT} 39/26
7	HV _{OUT} 18/47	27	N/C	47	HV _{OUT} 58/7	67	HV _{OUT} 38/27
8	HV _{OUT} 17/48	28	N/C	48	HV _{OUT} 57/8	68	HV _{OUT} 37/28
9	HV _{OUT} 16/49	29	\overline{LE}	49	HV _{OUT} 56/9	69	HV _{OUT} 36/29
10	HV _{OUT} 15/50	30	CLK	50	HV _{OUT} 55/10	70	HV _{OUT} 35/30
11	HV _{OUT} 14/51	31	\overline{BL}	51	HV _{OUT} 54/11	71	HV _{OUT} 34/31
12	HV _{OUT} 13/52	32	VDD	52	HV _{OUT} 53/12	72	HV _{OUT} 33/32
13	HV _{OUT} 12/53	33	DIR	53	HV _{OUT} 52/13	73	HV _{OUT} 32/33
14	HV _{OUT} 11/54	34	GND	54	HV _{OUT} 51/14	74	HV _{OUT} 31/34
15	HV _{OUT} 10/55	35	\overline{POL}	55	HV _{OUT} 50/15	75	HV _{OUT} 30/35
16	HV _{OUT} 9/56	36	N/C	56	HV _{OUT} 49/16	76	HV _{OUT} 29/36
17	HV _{OUT} 8/57	37	N/C	57	HV _{OUT} 48/17	77	HV _{OUT} 28/37
18	HV _{OUT} 7/58	38	N/C	58	HV _{OUT} 47/18	78	HV _{OUT} 27/38
19	HV _{OUT} 6/59	39	D _{IO} B	59	HV _{OUT} 46/19	79	HV _{OUT} 26/39
20	HV _{OUT} 5/60	40	VPP	60	HV _{OUT} 45/20	80	HV _{OUT} 25/40

Notes:

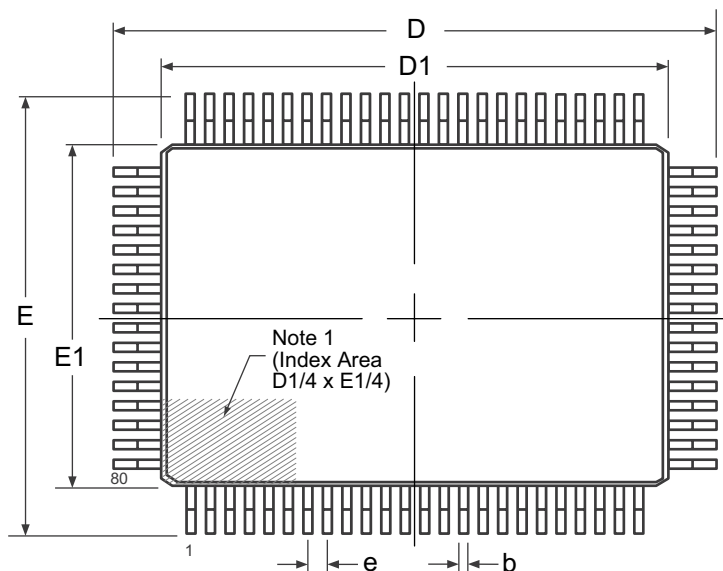
Pin designation for DIR = H/L.

Example: For DIR = H, pin 41 is HV_{OUT}64.

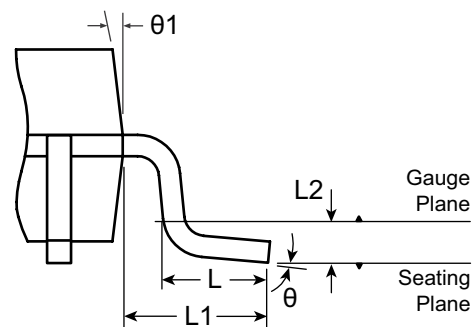
For DIR = L, pin 41 is HV_{OUT}1.

80-Lead PQFP Package Outline (PG)

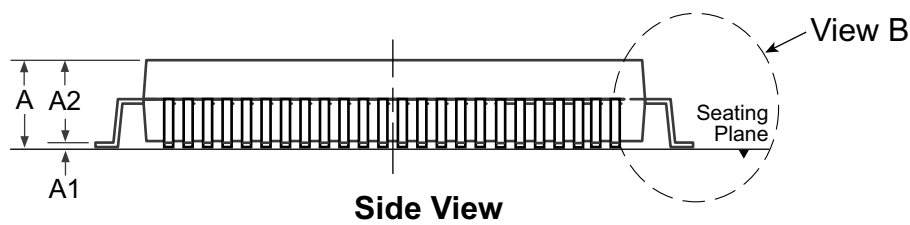
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



View B



Side View

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept. 1995.
 * This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings not to scale.
Supertex Doc. #: DSPD-80PQFP, Version B101708.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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