



FPF1038 / FPF1039

Low On-Resistance, Slew-Rate-Controlled Load Switch

Features

- 1.2V to 5.5V Input Voltage Operating Range
- Typical R_{ON} :
 - 20m Ω at $V_{IN}=5.5V$
 - 21m Ω at $V_{IN}=4.5V$
 - 37m Ω at $V_{IN}=1.8V$
 - 75m Ω at $V_{IN}=1.2V$
- Slew Rate/Inrush Control with t_R : 2.7ms (Typical)
- Output Capacitor Discharge Function on FPF1039
- Low <1 μA Shutdown Current at $V_{ON}=GND$
- ESD Protected: Above 8000V HBM, 1500V CDM
- GPIO/CMOS-Compatible Enable Circuitry

Applications

- HDD, Storage, and Solid State Memory Devices
- Portable Media Devices, UMPC, Tablets & MID's
- Wireless LAN Cards and Modules
- SLR Digital Cameras
- Portable Medical Devices
- GPS and Navigation Equipment
- Industrial Handheld and Enterprise Equipment

Description

The FPF1038/39 advanced load management switches target applications requiring a highly integrated solution for disconnecting loads powered from DC Power Rail (<6V) with stringent off-state current targets and high load capacitances (up to 200 μF). The FPF1038/39 consists of slew-rate controlled low-impedance MOSFET Switch (21m Ω typical) and other integrated analog features. The slew-rate controlled turn-on characteristic prevents inrush-current and the resulting excessive voltage droop on power rails. These devices have exceptionally low off-state current drain (<1 μA max) which facilitate compliance in very low stand-by power applications. The input voltage range operates from 1.2V to 5.5V DC to fulfill a wide range of applications in consumer, optical, medical, storage, portable, and industrial device power management. Switch control is managed by a logic input (Active High) capable of interfacing directly with low voltage control signal/GPIO with no external pull-up required. The device is packaged in advanced full-Green compliant 1x1.5 mm WLCSP (Wafer-Level-Chip-Scale Packaging) device providing excellent thermal conductivity, small footprint and low electrical resistance for wider application usage.

Ordering Information

Part Number	Top Mark	Switch R_{ON} (Typical) At 4.5V $_{IN}$	Input Buffer	Output Discharge	ON Pin Activity	t_R	Package
FPF1038UCX	QE	21m Ω	CMOS	NA	Active HIGH	2.7ms	6-Ball, Wafer-Level Chip-Scale Package (WLCSP), 1.0 x 1.5mm, 0.5mm Pitch
FPF1039UCX	QF	21m Ω	CMOS	65 Ω	Active HIGH	2.7ms	

Application Diagram

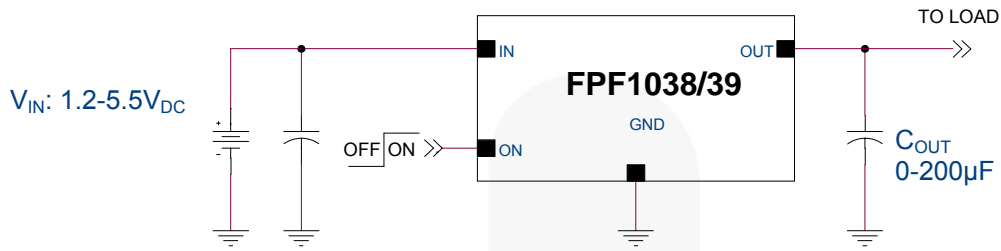


Figure 1. Typical Application

Note:

1. $C_{IN}=1\mu\text{F}$, X5R, 0603, such as Murata GRM185R60J105KE26.

Block Diagram

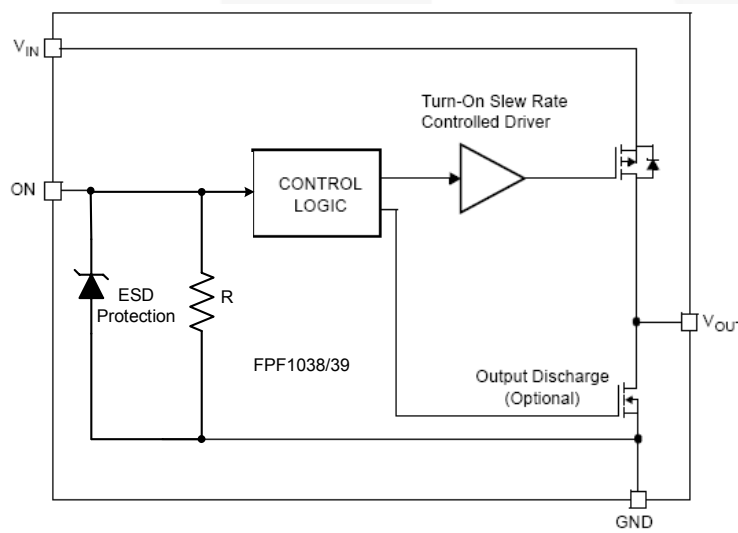


Figure 2. Block Diagram (Output Discharge for FPF1039 Only)

Pin Configurations

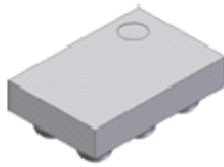


Figure 3. Bumps Facing Down

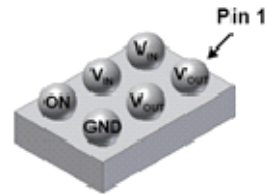


Figure 4. Bumps Facing Up

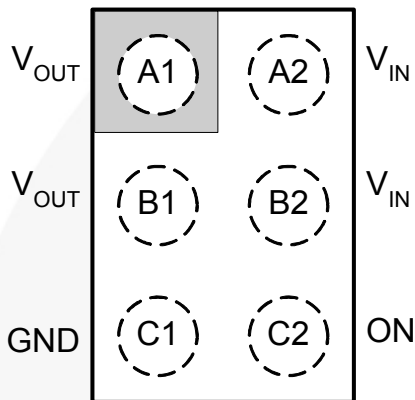


Figure 5. Top View

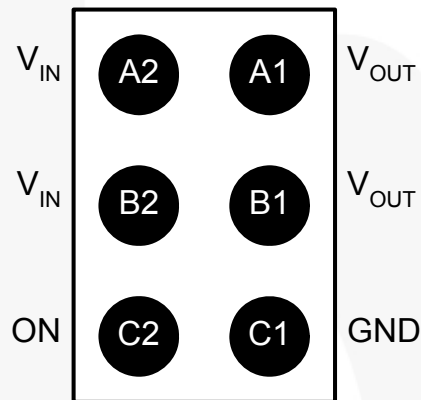


Figure 6. Bottom View

Pin Definitions

Pin #	Name	Description
A1, B1	V_{OUT}	Switch Output
A2, B2	V_{IN}	Supply Input: Input to the Power Switch
C1	GND	Ground
C2	ON	ON/OFF Control, Active High - GPIO Compatible

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	V_{IN} , V_{OUT} , V_{ON} to GND	-0.3	6.0	V
I_{SW}	Maximum Continuous Switch Current		2	A
P_D	Power Dissipation at $T_A=25^\circ\text{C}$		1.2	W
T_{STG}	Storage Junction Temperature	-65	+150	$^\circ\text{C}$
T_A	Operating Temperature Range	-40	+85	$^\circ\text{C}$
Θ_{JA}	Thermal Resistance, Junction-to-Ambient		85	$^\circ\text{C/W}$
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8.0	kV
		Charged Device Model, JESD22-C101	1.5	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.2	5.5	V
T_A	Ambient Operating Temperature	-40	+85	$^\circ\text{C}$

Electrical Characteristics

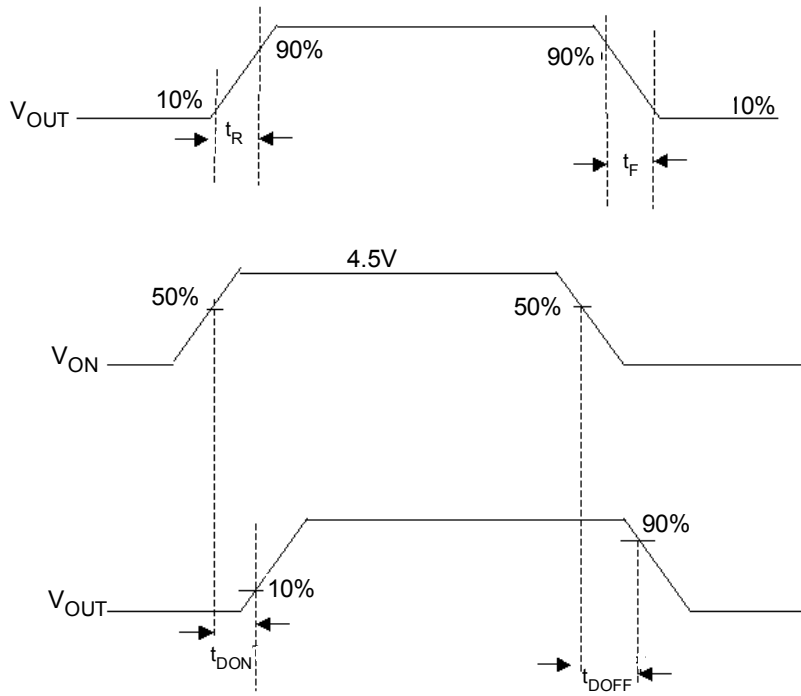
Unless otherwise noted, $V_{IN}=1.2$ to $5.5V$ and $T_A=-40$ to $+85^{\circ}C$; typical values are at $V_{IN}=4.5V$ and $T_A=25^{\circ}C$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
Basic Operation							
V_{IN}	Supply Voltage		1.2		5.5	V	
$I_{Q(OFF)}$	Off Supply Current	$V_{ON}=GND, V_{OUT}=Open$			1	μA	
$I_{SD(OFF)}$	Off Switch Current	$V_{ON}=GND, V_{OUT}=GND$		0.2	1.0	μA	
I_Q	Quiescent Current	$I_{OUT}=0mA$		5.5	8.0	μA	
R_{ON}	On-Resistance	$V_{IN}=5.5V, I_{OUT}=1A^{(2)}$		20		m Ω	
		$V_{IN}=4.5V, I_{OUT}=1A, T_A=25^{\circ}C$		21	25		
		$V_{IN}=3.3V, I_{OUT}=500mA^{(2)}$		24			
		$V_{IN}=2.5V, I_{OUT}=500mA^{(2)}$		28			
		$V_{IN}=1.8V, I_{OUT}=250mA^{(2)}$		37			
		$V_{IN}=1.2V, I_{OUT}=250mA, T_A=25^{\circ}C$		75	100		
R_{PD}	Output Discharge $R_{PULL\ DOWN}$	$V_{IN}=4.5V, V_{ON}=0V, I_{FORCE}=20mA, T_A=25^{\circ}C, PPF1039$ Only		65	85	Ω	
V_{IH}	ON Input Logic High Voltage		1.0			V	
V_{IL}	ON Input Logic Low Voltage				0.4	V	
I_{ON}	ON Input Leakage	PPF1038			1.0	μA	
		PPF1039			1.5		
Dynamic Characteristics: See Definitions Below							
t_{DON}	Turn-On Delay ⁽³⁾			1.7		ms	
t_R	V_{OUT} Rise Time ⁽³⁾	$V_{IN}=4.5V, R_L=5\Omega, C_L=100\mu F, T_A=25^{\circ}C$		2.7		ms	
t_{ON}	Turn-On Time ^(3,5)			4.4		ms	
t_{DOFF}	Turn-Off Delay ⁽³⁾		$V_{IN}=4.5V, R_L=150\Omega, C_L=100\mu F, T_A=25^{\circ}C$		2		ms
t_F	V_{OUT} Fall Time ⁽³⁾			30		ms	
t_{OFF}	Turn-Off ^(3,6)	PPF1038 (No Load Discharge)			32		ms
t_{DOFF}	Turn-Off Delay ⁽³⁾				0.5		ms
t_F	V_{OUT} Fall Time ⁽³⁾	$V_{IN}=4.5V, R_L=150\Omega, C_L=100\mu F, T_A=25^{\circ}C; PPF1039^{(4)}$		10		ms	
t_{OFF}	Turn-Off ^(3,6)				10.5		ms

Notes:

- This parameter is guaranteed by design and characterization; not production tested.
- $t_{DON}/t_{DOFF}/t_R/t_F$ are defined in Figure 7.
- Output discharge enabled during off-state.
- $t_{ON}=t_R + t_{DON}$.
- $t_{OFF}=t_F + t_{DOFF}$.

Timing Diagram



Notes:

- 7. $t_{ON} = t_R + t_{DON}$.
- 8. $t_{OFF} = t_F + t_{DOFF}$.

Figure 7. Timing Diagram



Typical Characteristics

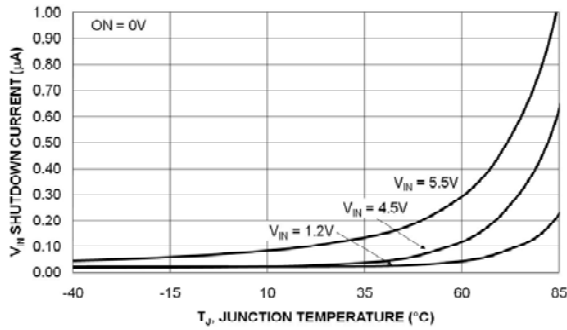


Figure 8. Shutdown Current vs. Temperature

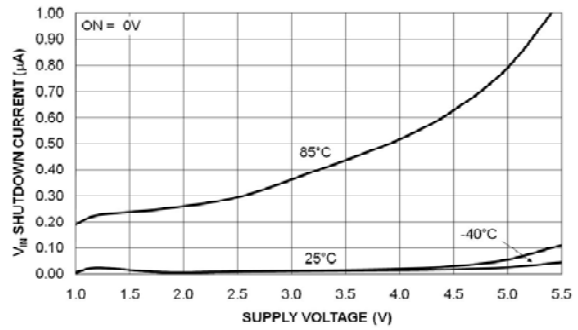


Figure 9. Shutdown Current vs. Supply Voltage

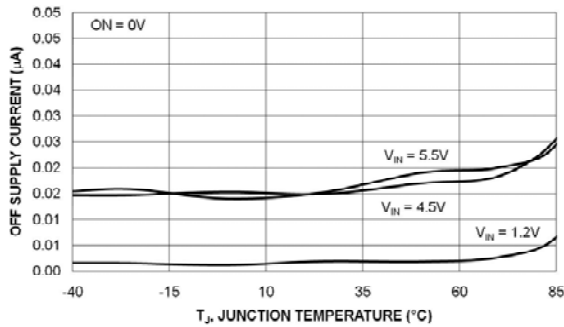


Figure 10. Off Supply Current vs. Temperature (FPF1038, V_{OUT} Floating)

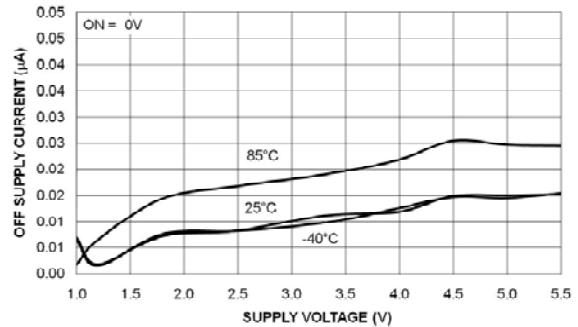


Figure 11. Off Supply Current vs. Supply Voltage (FPF1038, V_{OUT} Floating)

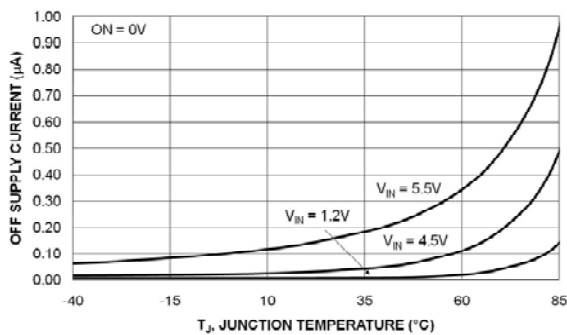


Figure 12. Off Supply Current vs. Temperature (FPF1039, $V_{OUT} = 0V$)

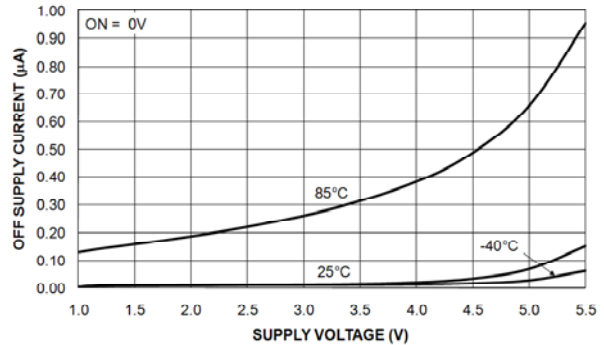


Figure 13. Off Supply Current vs. Supply Voltage (FPF1039, $V_{OUT} = 0V$)

Typical Characteristics (Continued)

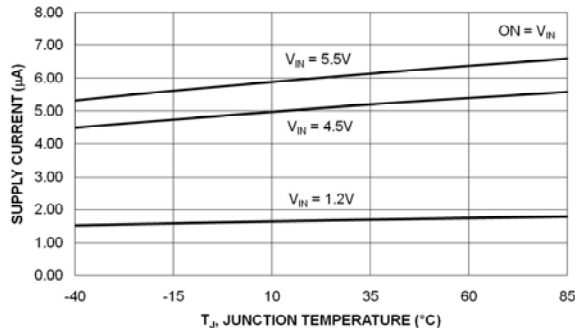


Figure 14. Quiescent Current vs. Temperature

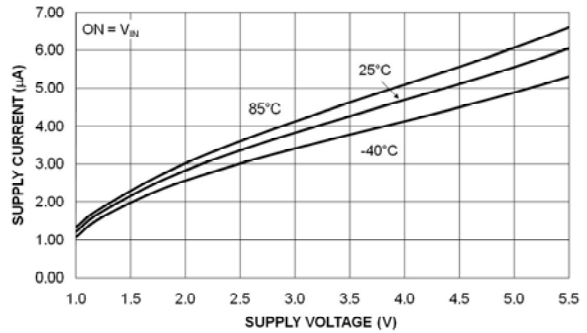


Figure 15. Quiescent Current vs. Supply Voltage

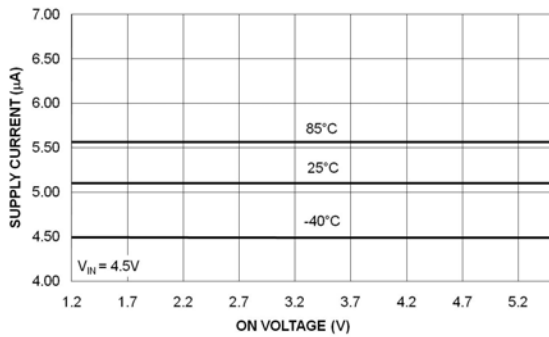


Figure 16. Quiescent Current vs. On Voltage (VIN = 4.5V)

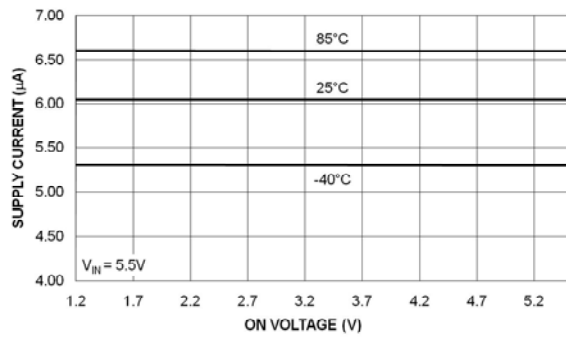


Figure 17. Quiescent Current vs. On Voltage (VIN = 5.5V)

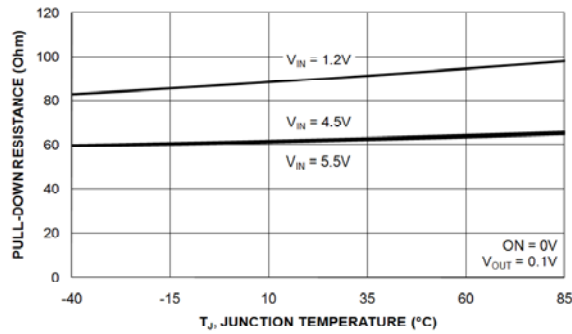


Figure 18. Output Discharge Resistor RPD vs. Temperature (FPF1039 Only)

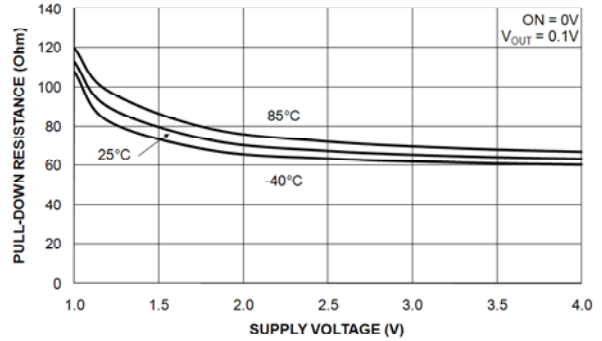


Figure 19. Output Discharge Resistor RPD vs. Supply Voltage (FPF1039 Only)

Typical Characteristics (Continued)

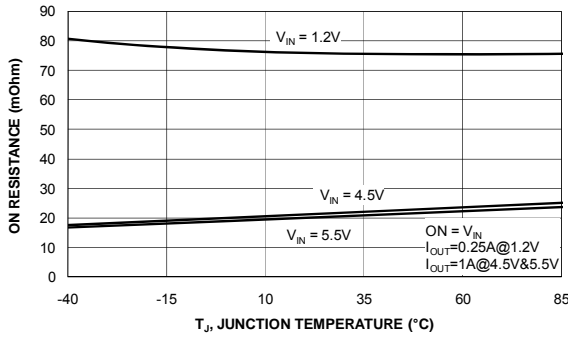


Figure 20. R_{ON} vs. Temperature

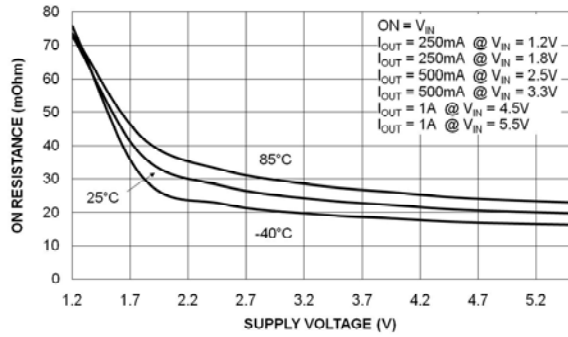


Figure 21. R_{ON} vs. Supply Voltage

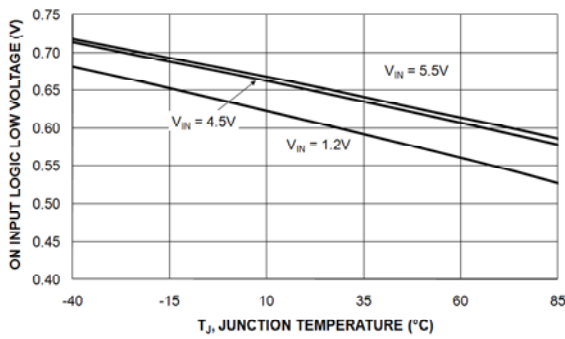


Figure 22. On Pin Threshold Low vs. Temperature

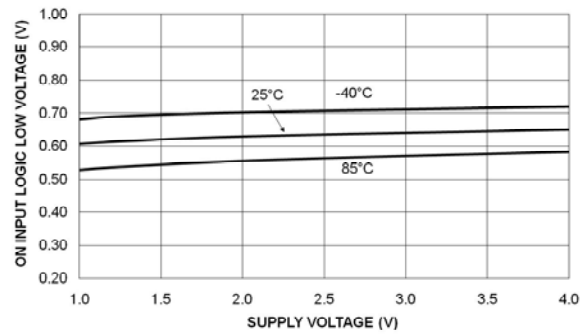


Figure 23. On Pin Threshold Low vs. V_{IN}

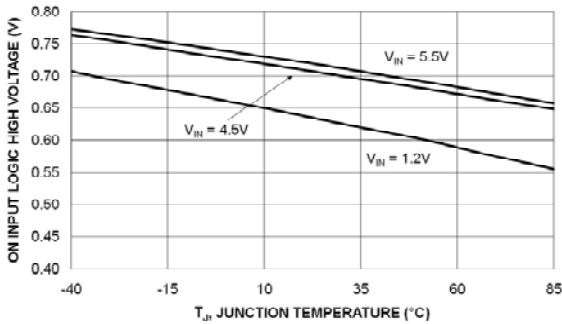


Figure 24. On Pin Threshold High vs. Temperature

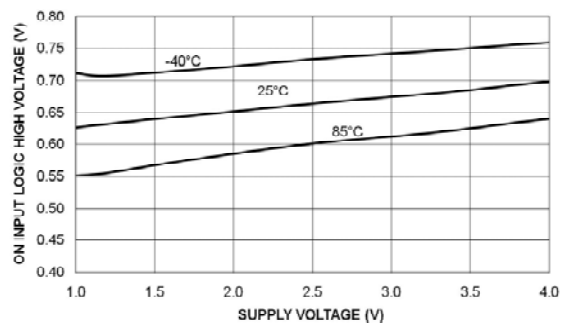


Figure 25. On Pin Threshold High vs. V_{IN}

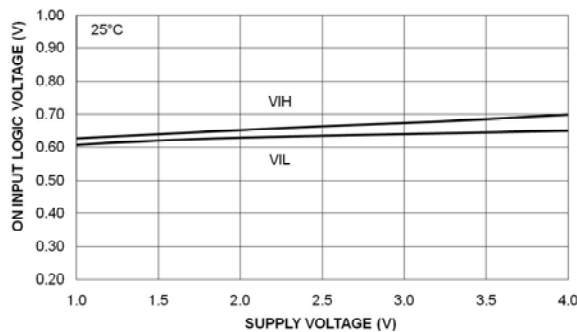


Figure 26. On Pin Threshold vs. Supply Voltage

Typical Characteristics (Continued)

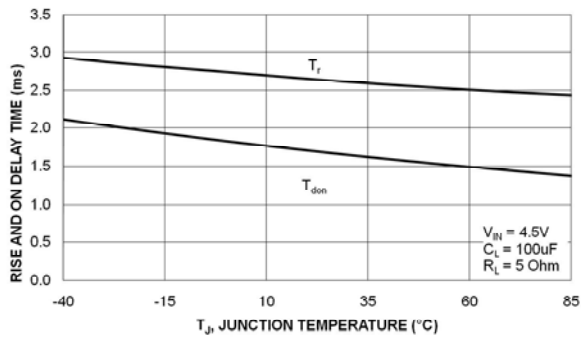


Figure 27. t_{RISE}/t_{DON} vs. Temperature (FPF1038)

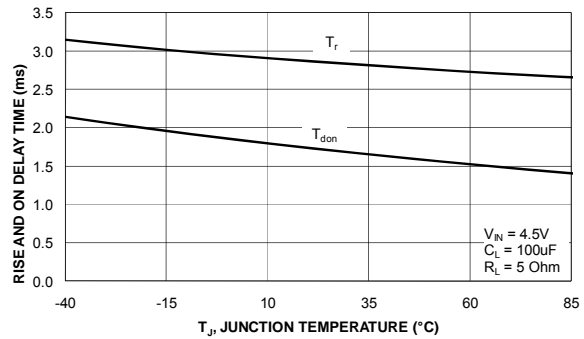


Figure 28. t_{RISE}/t_{DON} vs. Temperature (FPF1039)

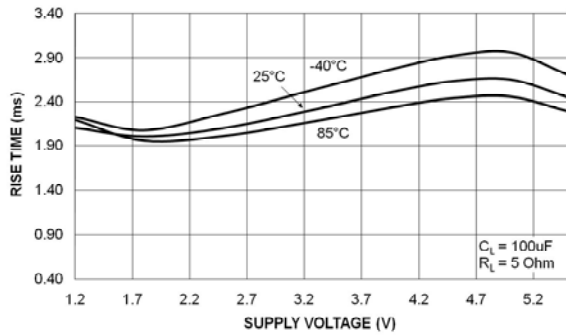


Figure 29. t_{RISE} vs. Supply Voltage

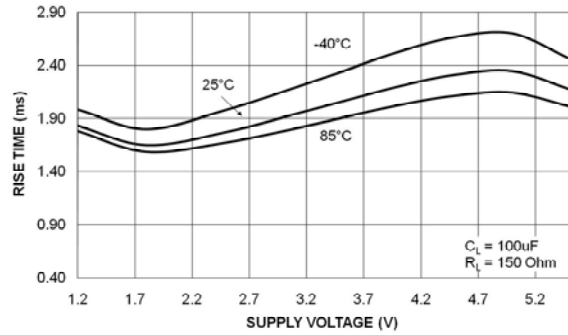


Figure 30. t_{RISE} vs. Supply Voltage

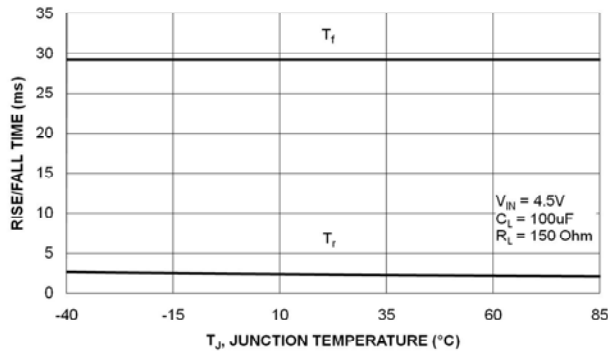


Figure 31. t_{RISE}/t_{FALL} vs. Temperature (FPF1038)

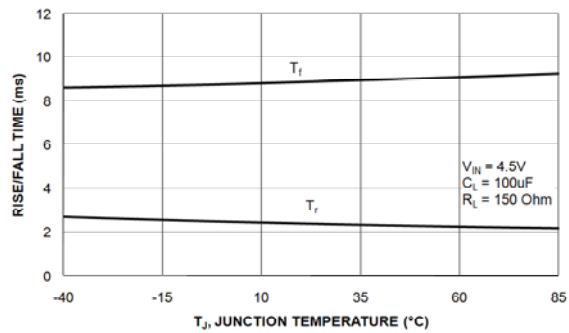


Figure 32. t_{RISE}/t_{FALL} vs. Temperature (FPF1039)

Typical Characteristics (Continued)

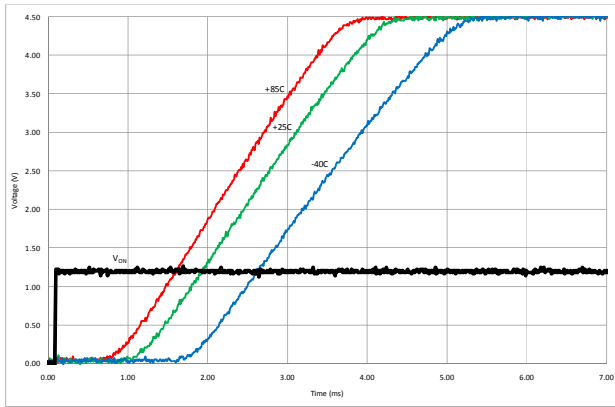


Figure 33. Turn-On Response ($V_{IN}=4.5V$, $C_{IN}=10\mu F$, $C_L=1\mu F$, $R_L=50\Omega$)

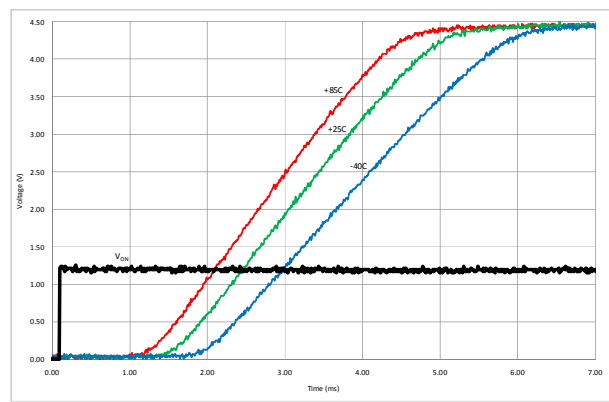


Figure 34. Turn-On Response ($V_{IN}=4.5V$, $C_{IN}=10\mu F$, $C_L=100\mu F$, $R_L=5\Omega$)

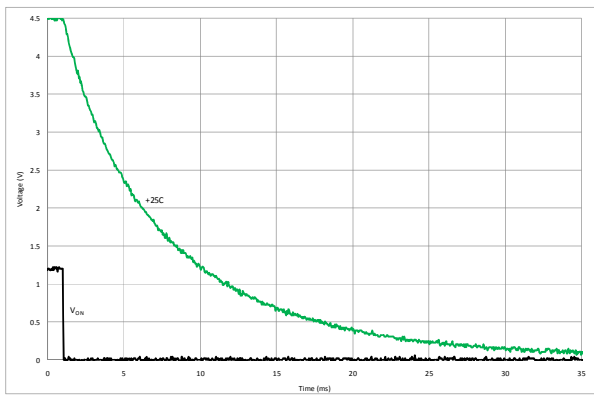


Figure 35. Turn-Off Response ($V_{IN}=4.5V$, $C_{IN}=10\mu F$, $C_L=100\mu F$, FPF1039 without External R_L)

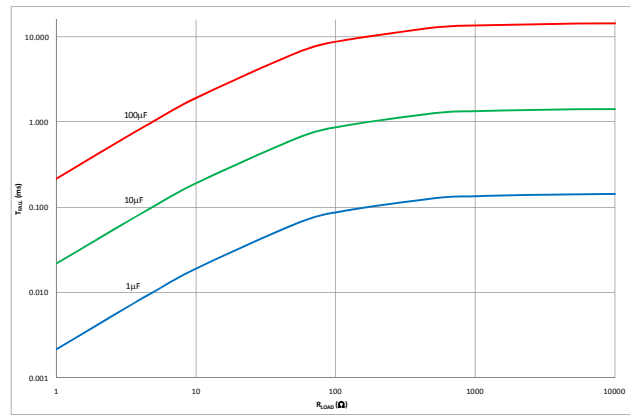


Figure 36. Fall Time as a Function of External Resistive Load ($C_L=1\mu F$, $10\mu F$ and $100\mu F$)

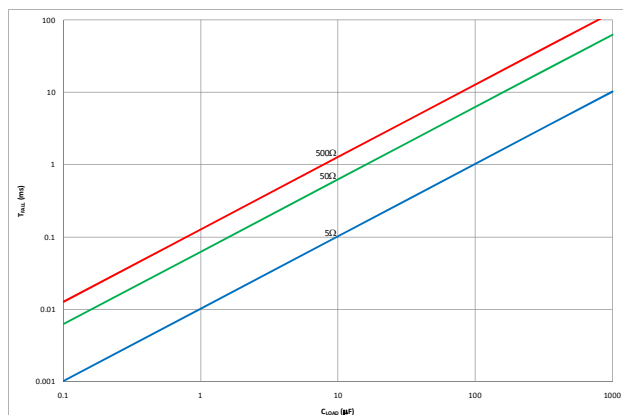


Figure 37. Fall Time as a Function of External Capacitive Load ($R_L=5\Omega$, 50Ω and 500Ω)

Application Information

Input Capacitor

This IntelliMAX™ switch doesn't require an input capacitor. To reduce device inrush current effect, a 0.1μF ceramic capacitor, C_{IN} , is recommended close to the V_{IN} pin. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

This IntelliMAX™ switch works without an output capacitor. However, if parasitic board inductance forces V_{OUT} below GND when switching off, a 0.1μF capacitor, C_{OUT} , should be placed between V_{OUT} and GND.

Fall Time

Device output fall time can be calculated based on RC constant of the external components as follows:

$$t_F = R_L \times C_L \times 2.2 \quad (1)$$

Application Specifics

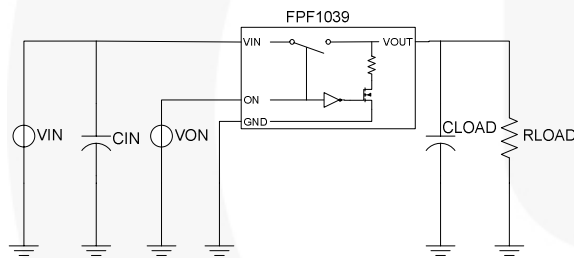


Figure 38. Device Setup

At maximum operational voltage ($V_{IN}=5.5V$) device inrush current might be higher than expected. Spike current should be taken into account if $V_{IN}>5V$ and the output capacitor is much larger than the input capacitor. Input current can be calculated as:

$$I_{IN}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN}) \frac{dV_{OUT}(t)}{dt} \quad (3)$$

Where switch and wire resistances are neglected and capacitors are assumed ideal.

where t_F is 90% to 10% fall time; R_L is output load, and C_L is output capacitor.

The same equation works for a device with a pull-down output resistor. R_L is replaced by a parallel connected pull-down and an external output resistor combination as:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \quad (2)$$

where t_F is 90% to 10% fall time, R_L is output load, $R_{PD}=65\Omega$ is output pull-down resistor, and C_L is the output capacitor.

Resistive Output Load

If resistive output load is missing, the IntelliMAX™ switch without a pull-down output resistor does not discharge the output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

Estimating $V_{OUT}(t)=V_{IN}/10$ and using experimental formula for slew rate ($dV_{OUT}(t)/dt$), spike current can be written as

$$\max(I_{IN}) = \frac{V_{IN}}{10R_{LOAD}} + (C_{LOAD} - C_{IN}) (0.05V_{IN} - 0.255) \quad (4)$$

Where supply voltage V_{IN} is in volts, capacitances are in micro farads and resistance in ohms.

Example: If $V_{IN}=5.5V$, $C_{LOAD}=100\mu F$, $C_{IN}=10\mu F$, and $R_{LOAD}=50\Omega$, calculate the spike current by:

$$\max(I_{IN}) = \frac{5.5}{10 \times 50} + (100 - 10)(0.05 \times 5.5 - 0.255)A = 1.8A \quad (5)$$

Maximum spike current is 1.8A, while average ramp-up current is:

$$I_{IN}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN}) \frac{dV_{IN}(t)}{dt} \quad (6)$$

$$\approx 2.75/50 + 100 \times 0.0022 = 0.275A$$

Recommended Land Pattern and Layout

For best thermal performance and minimal inductance and parasitic effects, it is recommended to keep input and output traces short and capacitors as close to the

device as possible. Figure 39 is a recommended layout for this device to achieve optimum performance.

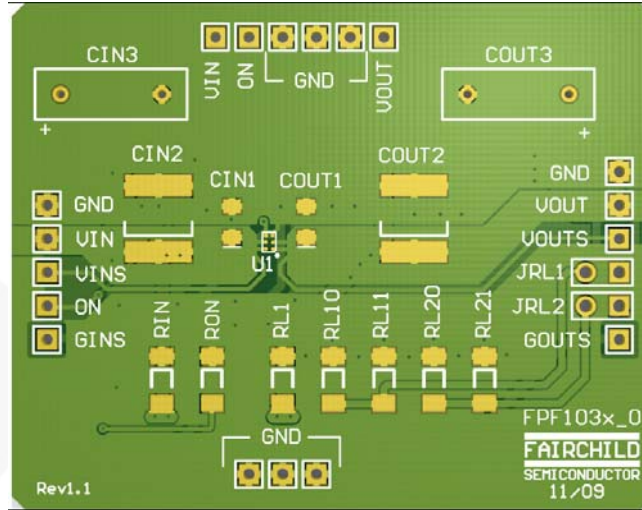
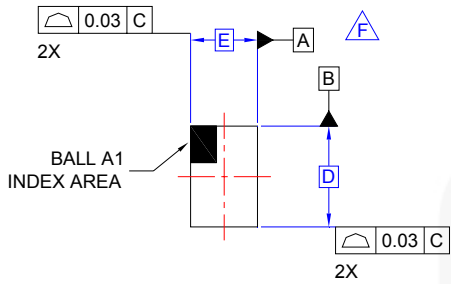
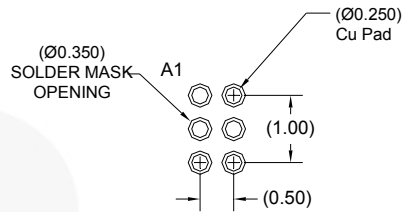


Figure 39. Recommended Land Pattern and Layout

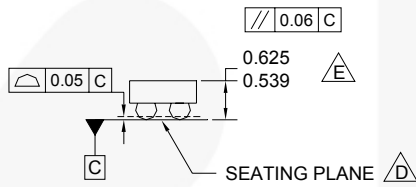
Physical Dimensions



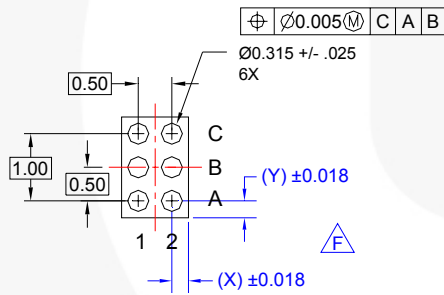
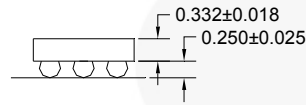
TOP VIEW



RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 582 MICRONS ±43 MICRONS (539-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC006AFrev2.

Figure 40. 6 Ball, 1.0 x 1.5mm Wafer-Level Chip-Scale Packaging (WLCSP)

Product-Specific Dimensions

Product	D	E	X	Y
FPF1038UCX	1.5mm+/-0.03	1.0mm+/-0.03	0.240mm	0.240mm
FPF1039UCX				


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Definition of Terms

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