MRF89XA
Data Sheet

Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

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MRF89XA

Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

Features

- Fully integrated ultra low-power, sub-GHz transceiver
- Wide band - Half-duplex transceiver
- Supports proprietary sub-GHz wireless protocols
- Simple, 4-wire SPI-compatible interface
- CMOS/TTL-compatible I/Os
- On-chip oscillator circuit
- Dedicated clock output
- Supports power-saving modes
- Operating voltage: 2.1V-3.6V
- Low-Current Consumption, Typically:
  - 3 mA in RX mode
  - 25 mA @ +10 dBm in TX mode
  - 0.1 µA (Typical) and 2 µA (Maximum) in Sleep mode
- Supports Industrial Temperature
- Small, 32-pin TQFN package; complies with ETSI EN 300 220 and FCC part 15

RF/Analog Features

- Supports ISM band sub-GHz frequency ranges: 863-870, 902-928 and 950-960 MHz
- Modulation technique: Supports FSK and OOK
- Supports high data rates: Up to 200 kbps, NRZ coding
- Reception sensitivity: Down to -107 dBm at 25 kb/s in FSK, -113 dBm at 2 kb/s in OOK
- RF output power: +12.5 dBm programmable in eight steps
- Wide Received Signal Strength Indicator (RSSI), dynamic range: 70 dB from RX noise floor
- Signal-ended RF input/output
- On-chip frequency synthesizer
- Supports PLL loop filter with lock detect
- Integrated Power Amplifier (PA) and Low Noise Amplifiers (LNA)
- Channel filters
- On-chip IF gain and mixers
- Integrated low phase noise VCO

Baseband Features

- Packet handling feature with data whitening and automatic CRC generation
- Incoming sync word (pattern) recognition
- Built-in bit synchronizer for incoming data, and clock synchronization and recovery
- 64-byte Transmit/Receive FIFO with preload in Standby mode
- Supports Manchester Encoding/Decoding Techniques

Typical Applications

- Home/industrial/building automation
- Remote wireless control
- Wireless PC peripherals
- Remote keyless entry
- Wireless sensor networks
- Vehicle sensor monitoring
- Telemetry
- Data logging systems
- Wireless alarm
- Remote automatic meter reading
- Security systems for home/industrial environments
- Automobile immobilizers
- Sports and performance monitoring
- Wireless toy controls
- Medical applications

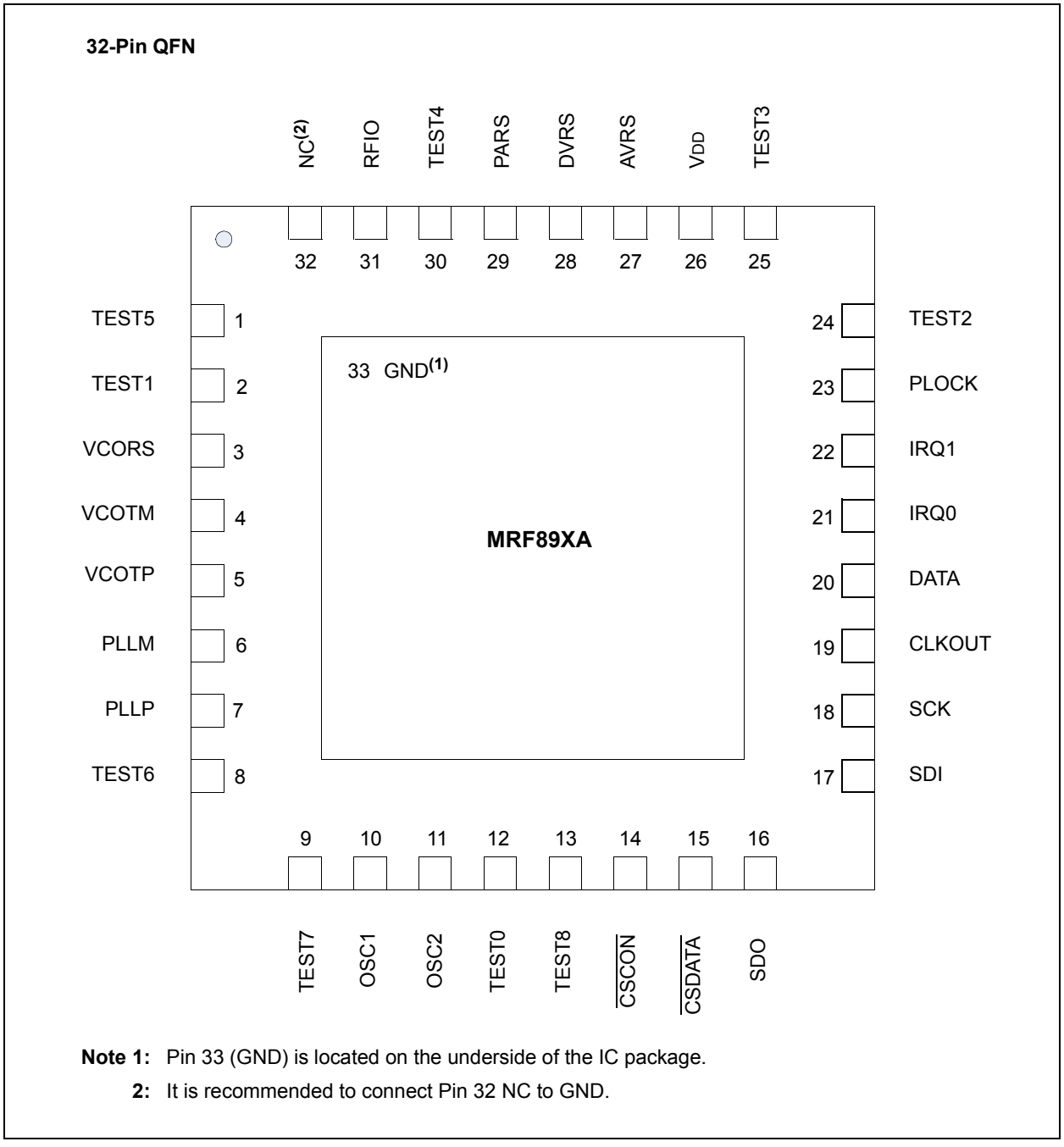
General Description

The MRF89XA is a single chip FSK/OOK transceiver capable of operating in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, as well as the 950-960 MHz frequency band. The low-cost MRF89XA is optimized for very low-power consumption (3 mA in Receiver mode). It incorporates a baseband modem with data rates up to 200 kb/s. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening. Its highly integrated architecture allows for minimum external component count while still maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC Part 15.247 and 15.249) regulatory standards.

Pin Diagram

The following diagram shows the top view pin arrangement of the 32-pin QFN package.

FIGURE 1: MRF89XA 32-PIN QFN PIN DIAGRAM



Note 1: Pin 33 (GND) is located on the underside of the IC package.

2: It is recommended to connect Pin 32 NC to GND.

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NOTES:

1.0 OVERVIEW

Microchip Technology's MRF89XA is a fully integrated, half-duplex, sub-GHz transceiver. This low-power, single chip RF FSK and OOK baseband transceiver supports:

- Super Heterodyne Architecture
- Multi-Channel, Multi-Band Synthesizer with Phase Lock Loop (PLL) for easy RF Design
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q Two Stage Down Converter Mixers
- I/Q Demodulator, FSK/OOK
- Baseband Filters and Amplifiers

The simplified functional block diagram of MRF89XA is shown in Figure 1-1.

The MRF89XA is a good choice for low-cost, high-volume, low data rate (<256 kbps), two-way short range wireless applications. This is a single chip FSK and OOK transceiver capable of operation in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, as well as the 950-960 MHz frequency band.

The low-cost MRF89XA is optimized for very low-power consumption (3 mA in Receiver mode). It incorporates a baseband modem with data rates up to 200 kb/s in FSK and 32 kb/s in OOK. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening. The device also supports Manchester coding techniques. Its highly integrated architecture allows for minimum external component count while still maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set.

The MRF89XA complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC Part 15.247 and 15.249) regulatory standards, and therefore, can be used for all applications looking for FCC, IC, or ETSI certification in the ISM band and licensed bands also.

The MRF89XA supports a stable sensitivity and linearity characteristics for a wide supply range and is internally regulated. The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit. The PLL and low phase noise provides for excellent adjacent channel rejection capability, Bit Error Rate (BER) and larger communication coverage along with higher output power.

The crystal oscillator provided on the MRF89XA device provides the reference clock for the PLL. In order to minimize the total system cost, a communication link in most of the applications can be created using a low-cost, generic 12.8 MHz crystal, a bypass filter and an affordable microcontroller. The MRF89XA provides a clock signal for the microcontroller and avoids the need for a second crystal on the circuit board. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers via a 4-wire SPI, interrupt (IRO), PLL lock and clock out. The interface between the microcontroller and MRF89XA is shown in Figure 1-1.

The MRF89XA supports the following digital data processing features:

- PLL and I/Q VCO Configuration
- Receiver Signal Strength Indicator
- Sync Word Recognition
- Packet Handler
- Interrupt and Flags
- Different Operating Modes (Continuous, Buffer and Packet)
- Data Filtering/Whitening/Encoding
- Baseband Power Amplifier
- TX/RX Data Buffer

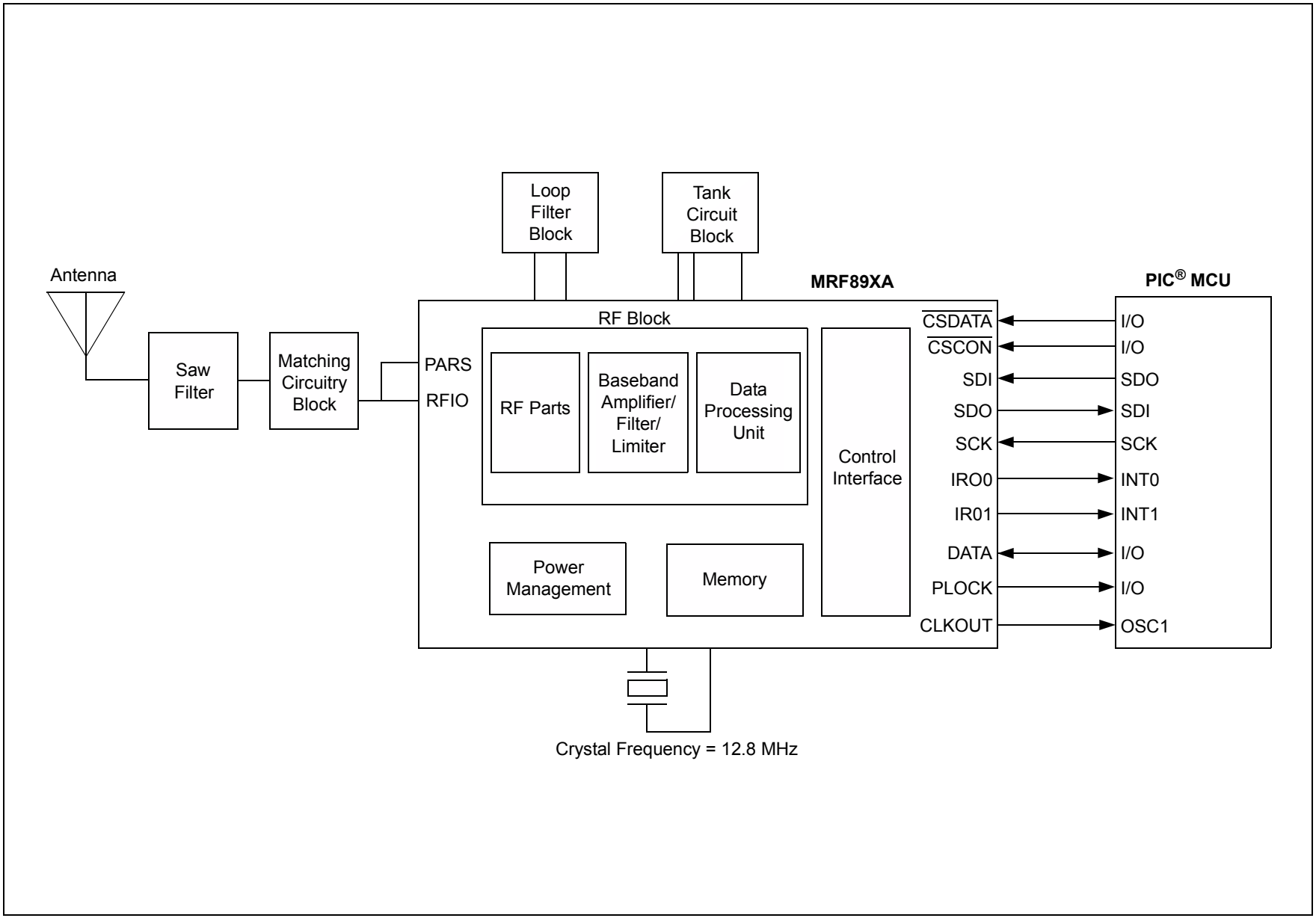
The role is to interface the data to/from the modulator/demodulator and the microcontroller access points (SPI, IRQ and DATA pins). It also controls all the Configuration registers. The receiver's Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations and data rates requirements.

The high-resolution PLL allows:

- The usage of multiple channels in any of the bands
- The rapid settling time allows for faster frequency hopping, bypassing multi-path fading and interference to achieve robust wireless links

An optional Bit Synchronizer (BitSync) is provided, to supply a synchronous clock and data stream to a companion microcontroller in Continuous mode, or to fill the FIFO with glitch-free data in Buffered mode. The transceiver is integrated with different power-saving modes and an internal wake-up time to keep track of the activities, which reduces the overall current consumption and extends the battery life. The small size and low-power consumption of the MRF89XA makes it ideal for various short range radio applications.

FIGURE 1-1: MRF89XA SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



2.0 HARDWARE DESCRIPTION

The MRF89XA is an integrated, single chip, low-power ISM band sub-GHz transceiver. A simplified architectural block diagram of the MRF89XA is shown in Figure 2-1. The frequency synthesizer is clocked by an external 12.8 crystal, and frequency ranges from 863-870 MHz, 902-928 MHz and 950-960 MHz.

The MRF89XA receiver employs a super-heterodyne architecture. Here, the first IF is 1/9th of the RF frequency (approximately 100 MHz). The second down conversion down converts the I and Q signals to baseband in the case of the FSK receiver (Zero IF) and to a low-IF (IF2) for the OOK receiver. After the second down-conversion stage, the received signal is channel select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Image rejection is achieved by the SAW filter.

The baseband I and Q signals at the transmitter side are digitally generated by a DDS whose Digital-to-Analog Converters (DAC) followed by two anti-aliasing low-pass filters transform the digital signal into analog In-Phase (I) and Quadrature (Q) components whose frequency is the selected Frequency Deviation (Fdev). The transmitter supports both FSK and OOK modes of operation. The transmitter has a typical output power of +12.5 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into a single-ended RFIO pin. This pin is connected to the impedance matching circuitry (Balun) and to the external antenna with power amplifier pin, if required. The device operates in the low-voltage range of 2.1V to 3.6V, and in Sleep mode, it operates at a very low-current state, typically 0.1 µA.

The quality of the data is validated using the RSSI and bit synchronizer blocks built into the transceiver. Data is buffered in 64-byte transmitter registers and receiver FIFOs. The frequency synthesizer allows the use of a low-accuracy, low-cost crystal. CLKOUT can be used to clock the external controller. The transceiver is controlled via a 4-wire Serial Peripheral Interface (SPI), interrupt (IRO0 and IRO1), PLOCK, DATA and Chip Select pins for SPI.

The MRF89XA supports the following feature blocks:

- Data Filtering and Whitening
- Bit Synchronization
- 64-Byte Transmit and Receive FIFO Buffer
- General Configuration Registers

These features reduce the processing load, which allows the use of simple, low-cost 8-bit microcontrollers for data processing.

FIGURE 2-1: MRF89XA BLOCK DIAGRAM

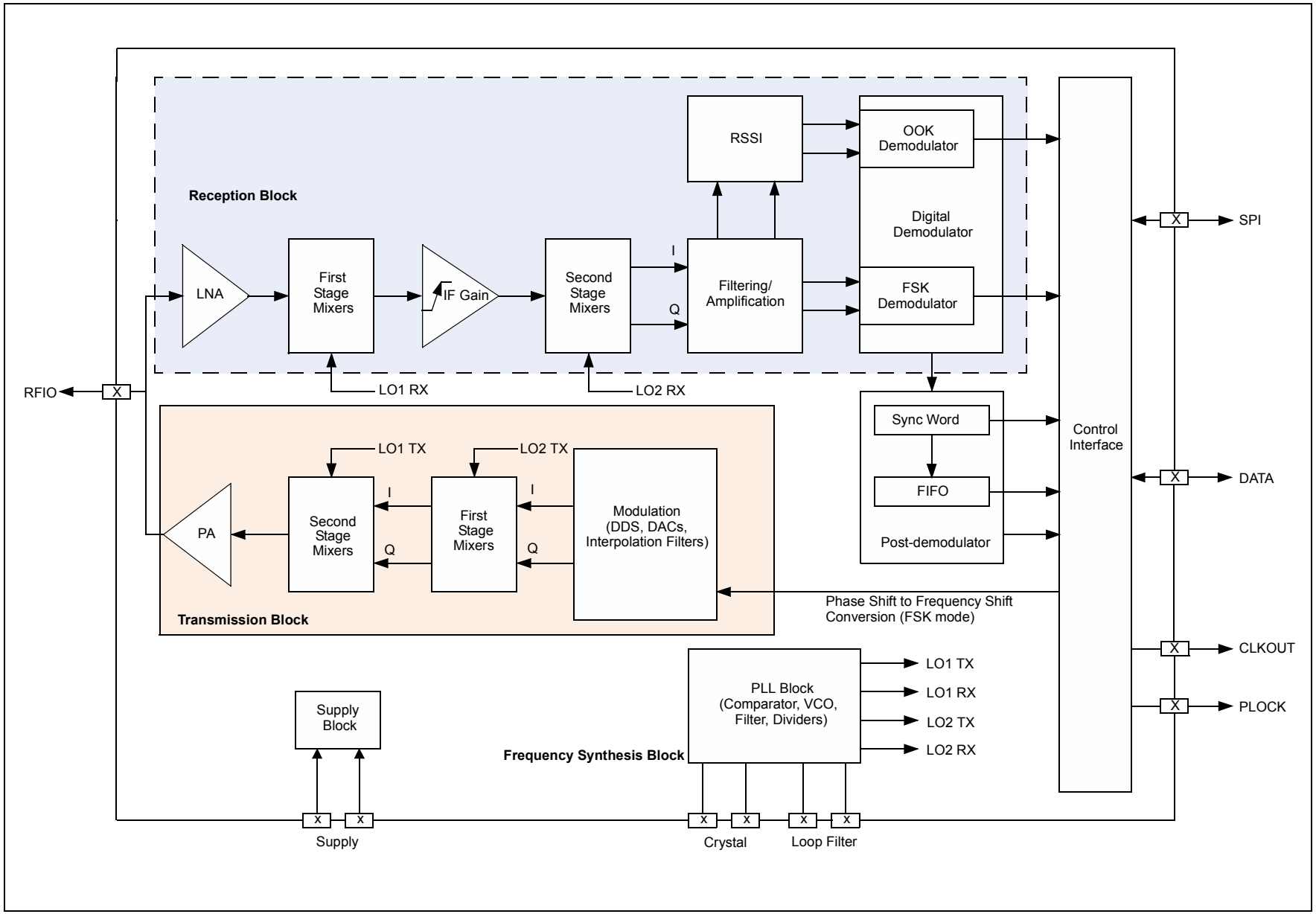
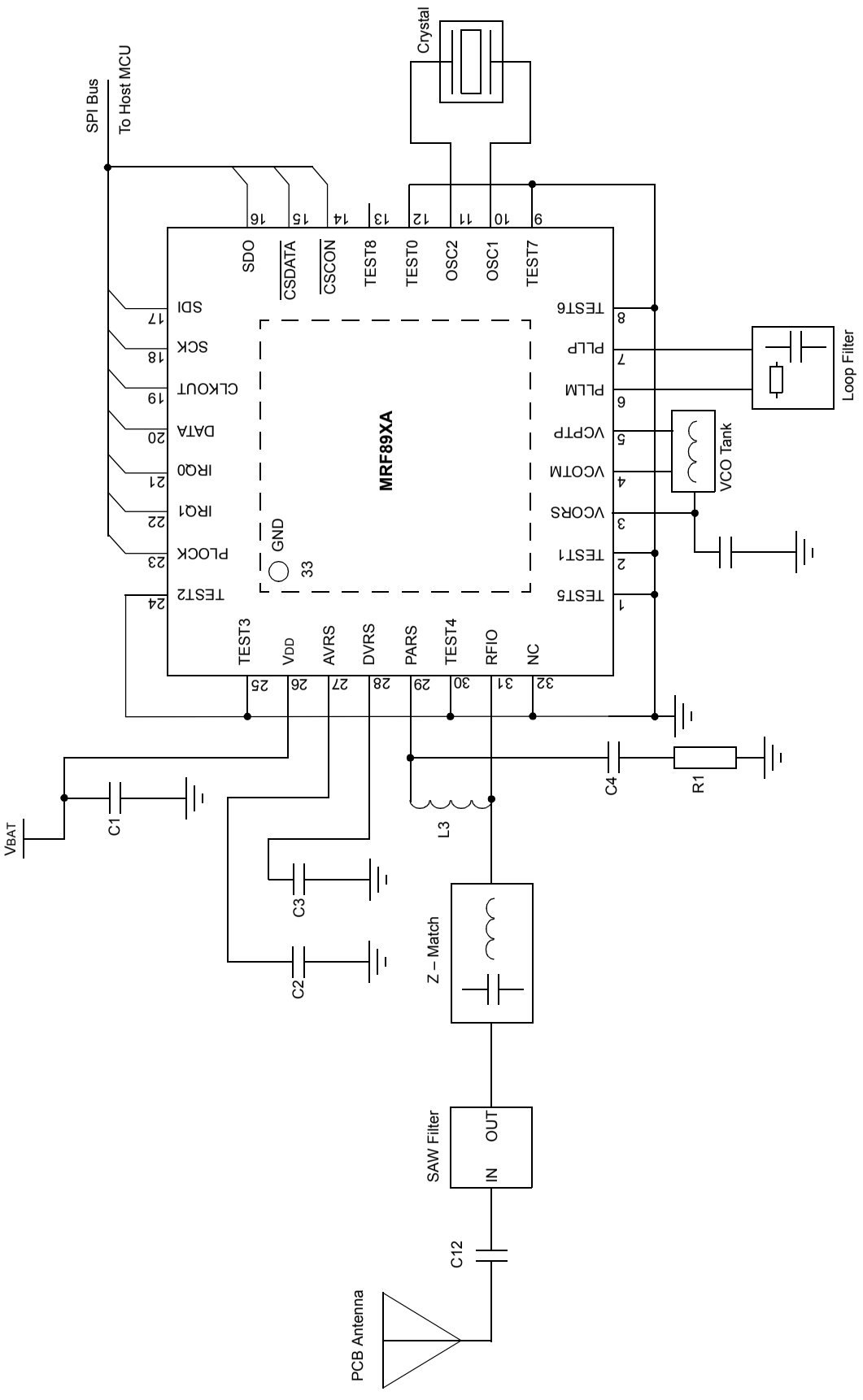


TABLE 2-1: PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Type	Description
1	TEST5	Digital I/O	Test Pin. Connect to Ground.
2	TEST1	Digital I/O	Test Pin. Connect to Ground.
3	VCORS	Analog Output	Regulated voltage supply of the VCO.
4	VCOTM	Analog I/O	VCO tank.
5	VCOTP	Analog I/O	VCO tank.
6	PLLM	Analog I/O	PLL loop filter.
7	PLLP	Analog I/O	PLL loop filter.
8	TEST6	Digital I/O	Test Pin. Connect to Ground.
9	TEST7	Digital I/O	Test Pin. Connect to Ground.
10	OSC1	Analog Input	Crystal connection.
11	OSC2	Analog Input	Crystal connection.
12	TEST0	Digital Input	Test Pin. Connect to Ground.
13	TEST8	Digital I/O	Test Pin. Used for POR (allow pin to float; do not connect signal).
14	$\overline{\text{CSCON}}$	Digital Input	SPI Configure Chip Select.
15	$\overline{\text{CSDATA}}$	Digital Input	SPI Data Chip Select.
16	SDO	Digital Output	Serial data output interface from MRF89XA.
17	SDI	Digital Input	Serial data input interface to MRF89XA.
18	SCK	Digital Input	Serial clock interface.
19	CLKOUT	Digital Output	Clock output.
20	DATA	Digital I/O	NRZ data input and output (Continuous mode).
21	IRQ0	Digital Output	Interrupt request output (‘0’).
22	IRQ1	Digital Output	Interrupt request output (‘1’).
23	PLOCK	Digital Output	PLL lock detection output.
24	TEST2	Digital I/O	Test Pin. Connect to Ground.
25	TEST3	Digital I/O	Test Pin. Connect to Ground.
26	V_{DD}	Power	Supply voltage.
27	AVRS	Analog Output	Regulated supply of the analog circuitry.
28	DVRS	Analog Output	Regulated supply of the digital circuitry.
29	PARS	Analog Output	Regulated supply of the PA.
30	TEST4	Digital I/O	Connect to GND.
31	RFIO	Analog I/O	RF input/output.
32	NC	—	No Connection. Connect to Ground.
33	Vss	Ground	Exposed Pad. Connect to Ground.

FIGURE 2-2: APPLICATION CIRCUIT SCHEMATIC



2.1 Memory Map for MRF89XA Configuration/Control/Status Registers

The memory in the MRF89XA transceiver is implemented as static RAM and is accessible via the SPI port. Each memory location functionally addresses the command, control, status or data/FIFO fields as shown in Table 2-2 and Table 2-3. The control registers provide control, status and configuration information. The device address for the transceiver is done by indexing the base address in the RAM memory. The registers operate fundamentally on parameters common to transmit and receive modes, Interrupt registers, receiver parameters, Sync pattern, transmitter parameters, crystal oscillator parameters and packet handler parameters. The FIFO serves as a temporary buffer for data transmission and reception.

TABLE 2-2: CONFIGURATION/CONTROL/STATUS REGISTER DESCRIPTION

General Parameters Configuration Registers: Size – 13 Bytes, Start Address – 00				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
1.	0	GCONREG	General Configuration Register	Transceiver mode, frequency band selection, VCO trimming, PLL frequency dividers selection
2.	1	DMODREG	Data and Modulation Configuration Register	Modulation type, Data mode, OOK threshold type, IF gain
3.	2	FDEVREG	Frequency Deviation Control Register	Frequency deviation in FSK Transmit mode
4.	3	BRSREG	Bit Rate Set Register	Operational bit rate
5.	4	FLTHREG	Floor Threshold Control Register	Floor threshold in OOK Receive mode
6.	5	FIFOCREG	FIFO Configuration Register	FIFO size and threshold
7.	6	R1CNTSREG	R1 Counter Set Register	Value input for R1 counter
8.	7	P1CNTSREG	P1 Counter Set Register	Value input for P1 counter
9.	8	S1CNTSREG	S1 Counter Set Register	Value input for S1 counter
10.	9	R2CNTSREG	R2 Counter Set Register	Value input for R2 counter
11.	10	P2CNTSREG	P2 Counter Set Register	Value input for P2 counter
12.	11	S2CNTSREG	S2 Counter Set Register	Value input for S2 counter
13.	12	PACONREG	Power Amplifier Control Register	PA regulator output voltage

Interrupt Parameters Configuration Registers: Size – 3 Bytes, Start Address – 13				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
14.	13	FTXRXIREG	FIFO, Transmit and Receive Interrupt Request Configuration Register	Interrupt request (‘0’ and ‘1’) in Receive mode, interrupt request (‘1’) in Transmit mode, interrupt request for FIFO full, empty and overrun
15.	14	FTPRIREG	FIFO Transmit PLL and RSSI Interrupt Configuration Register	FIFO fill method, FIFO fill, interrupt request for TX start and end, interrupt request for RSSI, PLL lock enable and status
16.	15	RSTHIREG	RSSI Threshold Interrupt Request Configuration Register	RSSI threshold for interrupt

TABLE 2-2: CONFIGURATION/CONTROL/STATUS REGISTER DESCRIPTION (CONTINUED)

Receiver Parameters Configuration Registers: Size – 6 Bytes, Start Address – 16				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
17.	16	FILCONREG	Filter Configuration Register	Passive filter bandwidth selection, sets the receiver bandwidth (Butterworth filter),
18.	17	PFCONREG	Polyphase Filter Configuration Register	Selects the central frequency of the polyphase filter
19.	18	SYNCREG	Sync Control Register	Enables polyphase filter (in OOK receive mode, bit synchronizer control, Sync word recognition, Sync word size, Sync word error
20.	19	RESVREG	Reserved Register	Reserved for future use
21.	20	RSTSREG	RSSI Status Read Register	RSSI output
22.	21	OOKCREG	OOK Configuration Register	RSSI threshold size in OOK demodulator, RSSI threshold period in OOK demodulator, cut-off frequency of the OOK threshold in demodulator

Sync Word Parameters Configuration Registers: Size – 4 Bytes, Start Address – 22				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
23.	22	SYNCV31REG	Sync Value 1st Byte Configuration Register	Configuring 1st byte of the 32-bit Sync word
24.	23	SYNCV23REG	Sync Value 2nd Byte Configuration Register	Configuring 2nd byte of the 32-bit Sync word
25.	24	SYNCV15REG	Sync Value 3rd Byte Configuration Register	Configuring 3rd byte of the 32-bit Sync word
26.	25	SYNCV07REG	Sync Value 4th Byte Configuration Register	Configuring 4th byte of the 32-bit Sync word

Transmitter Parameters Configuration Registers: Size – 1 Byte, Start Address – 26				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
27.	26	TXPARCREG	Transmit Parameters Configuration Register	Transmit interpolation cut-off frequency, power output

Oscillator Parameters Configuration Registers: Size – 1 Byte, Start Address – 27				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
28.	27	CLKOUTREG	Clock Output Control Register	Clock-out control, frequency

TABLE 2-2: CONFIGURATION/CONTROL/STATUS REGISTER DESCRIPTION (CONTINUED)

Packet Handling Parameters Configuration Registers: Size – 4 Bytes, Start Address – 28				
Sl. No.	**Register Address**	**Register Name**	**Register Description**	**Related Control Functions**
29.	28	PLOADREG	Payload Configuration Register	Enable Manchester encoding/decoding, payload length
30.	29	NADDSREG	Node Address Set Register	Node's local address for filtering of received packets
31.	30	PKTCREG	Packet Configuration Register	Packet format, size of the preamble, whitening, CRC on/off, address filtering of received packets, CRC status
32.	31	FCRCREG	FIFO CRC Configuration Register	FIFO auto-clear (if CRC failed), FIFO access

TABLE 2-3: CONFIGURATION/CONTROL/STATUS REGISTER MAP

Register Function/ Parameter Type	Register Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
General	0	GCONREG	CMOD2	CMOD1	CMOD0	FBS1	FBS0	VCOT1	VCOT0	RPS	0x28
	1	DMODREG	MODSEL1	MODSEL0	DMODE0	OOKTYP1	OOKTYP0	DMODE1	IFGAIN1	IFGAIN	0x88
	2	FDEVREG	FDVAL7	FDVAL6	FDVAL5	FDVAL4	FDVAL3	FDVAL2	FDVAL1	FDVAL0	0x03
	3	BRSREG	Reserved	BRVAL6	BRVAL5	BRVAL4	BRVAL3	BRVAL2	BRVAL1	BRVAL0	0x07
	4	FLTHREG	FTOVAL7	FTOVAL6	FTOVAL5	FTOVAL4	FTOVAL3	FTOVAL2	FTOVAL1	FTOVAL0	0x0C
	5	FIFOCREG	FSIZE1	FSIZE0	FTINT5	FTINT4	FTINT3	FTINT2	FTINT1	FTINT0	0x0F
	6	R1CNTSREG	R1CVAL7	R1CVAL6	R1CVAL5	R1CVAL4	R1CVAL3	R1CVAL2	R1CVAL1	R1CVAL0	0x77
	7	P1CNTSREG	P1CVAL7	P1CVAL6	P1CVAL5	P1CVAL4	P1CVAL3	P1CVAL2	P1CVAL1	P1CVAL0	0x64
	8	S1CNTSREG	S1CVAL7	S1CVAL6	S1CVAL5	S1CVAL4	S1CVAL3	S1CVAL2	S1CVAL1	S1CVAL0	0x32
	9	R2CNTSREG	R2CVAL7	R2CVAL6	R2CVAL5	R2CVAL4	R2CVAL3	R2CVAL2	R2CVAL1	R2CVAL0	0x74
	10	P2CNTSREG	P2CVAL7	P2CVAL6	P2CVAL5	P2CVAL4	P2CVAL3	P2CVAL2	P2CVAL1	P2CVAL0	0x62
	11	S2CNTSREG	S2CVAL7	S2CVAL6	S2CVAL5	S2CVAL4	S2CVAL3	S2CVAL2	S2CVAL1	S2CVAL0	0x32
	12	PACONREG	Reserved	Reserved	Reserved	PARC1	PARC0	Reserved	Reserved	Reserved	0x38
	13	FTXRXIREG	IRQ0RXS1	IRQ0RXS0	IRQ1RXS1	IRQ1RXS0	TXIRQ1	FIFOFULL	FIFOMTY	FOVRRUN	0x00
Interrupt	14	FTPRIREG	FIFOFM	FIFOSC	TXDONE	TXSTIRQ0	Reserved	RIRQS	LSTSPLL	LENPLL	0x01
	15	RSTHIREG	RTIVAL7	RTIVAL6	RTIVAL5	RTIVAL4	RTIVAL3	RTIVAL2	RTIVAL1	RTIVAL0	0x00
	16	FILCONREG	PASFILV3	PASFILV2	PASFILV1	PASFILV0	BUTFILV3	BUTFILV2	BUTFILV1	BUTFILV0	0xA3
Receiver	17	PFCONREG	POLCFV3	POLCFV2	POLCFV1	POLCFV0	Reserved	Reserved	Reserved	Reserved	0x38
	18	SYNCREG	POLFILEN	BSYNCEN	SYNCREN	SYNCWSZ1	SYNCWSZ0	SYNCTEN1	SYNCTEN0	Reserved	0x18
	19	RESVREG	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x07
	20	RSTSREG	RSSIVAL7	RSSIVAL6	RSSIVAL5	RSSIVAL4	RSSIVAL3	RSSIVAL2	RSSIVAL1	RSSIVAL0	Read-only
	21	OOKCREG	OOKTHSV2	OOKTHSV1	OOKTHSV0	OOKTHPV2	OOKTHPV1	OOKTHPV0	OOKATHC1	OOKATHC0	0x00
Sync Word	22	SYNCV31REG	SYNC1BV7	SYNC1BV6	SYNC1BV5	SYNC1BV4	SYNC1BV3	SYNC1BV2	SYNC1BV1	SYNC1BV0	0x00
	23	SYNCV23REG	SYNC2BV7	SYNC2BV6	SYNC2BV5	SYNC2BV4	SYNC2BV3	SYNC2BV2	SYNC2BV1	SYNC2BV0	0x00
	24	SYNCV15REG	SYNC3BV7	SYNC3BV6	SYNC3BV5	SYNC3BV4	SYNC3BV3	SYNC3BV2	SYNC3BV1	SYNC3BV0	0x00
	25	SYNCV07REG	SYNC4BV7	SYNC4BV6	SYNC4BV5	SYNC4BV4	SYNC4BV3	SYNC4BV2	SYNC4BV1	SYNC4BV0	0x00
Transmitter	26	TXPARCREG	TXIPOLFV3	TXIPOLFV2	TXIPOLFV1	TXIPOLFV0	TXOPVAL2	TXOPVAL1	TXOPVAL0	Reserved	0x7C
Clock-out	27	CLKOUTREG	CLKOCNTRL	CLKOFREQ5	CLKOFREQ4	CLKOFREQ3	CLKOFREQ2	CLKOFREQ1	Reserved	Reserved	0xBC
Packet	28	PLOADREG	MCHSTREN	PLDPLEN6	PLDPLEN5	PLDPLEN4	PLDPLEN3	PLDPLEN2	PLDPLEN1	PLDPLEN0	0x00
	29	NADDSREG	NLADDR7	NLADDR6	NLADDR5	NLADDR4	NLADDR3	NLADDR2	NLADDR1	NLADDR0	0x00
	30	PKTCREG	PKTLENF	PRESIZE1	PRESIZE0	WHITEN1	CHKCRCEN	ADDFIL1	ADDFIL0	STSCRCEN	0x68
	31	FCRCREG	ACFCRC	FRWAXS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00

3.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -55°C to +125°C
Lead temperature (soldering, max 10s) ..... +260°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to 6V
Voltage on any combined digital and analog pin with respect to V_{SS} (except RFIO and V_{DD}) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on open-collector outputs (RFIO)(1) ..... -0.3V to 3.7V
Input current into pin (except V_{DD} and V_{SS}) ..... -25 mA to 25 mA
Electrostatic discharge with human body model 1000V

Note 1: At maximum, voltage on RFIO cannot be higher than 6V.

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.1 ESD Notice

The MRF89XA is a high-performance radio frequency device. It satisfies:

- Class II of the JEDEC standard JESD22-A114-B (Human Body Model) of 2 KV, except on all of the RF pins where it satisfies Class 1A.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins.

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

TABLE 3-1: RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit	Condition
Ambient Operating Temperature	-40	—	+85	°C	—
Supply Voltage for RF, Analog and Digital Circuits	2.1	—	3.6	V	—
Supply Voltage for Digital I/O	2.1	—	3.6	V	—
Input High Voltage (V_{IH})	0.5 * V_{DD}	—	V_{DD} + 0.3	V	—
Input Low Voltage (V_{IL})	-0.3V	—	0.2 * V_{DD}	V	—
DC Voltage on Open Collector Outputs (RFIO)(1,2)	V_{DD} – 1.5	—	V_{DD} + 1.5	V	—
AC Peak Voltage on Open Collector Outputs (IO)(1)	V_{DD} – 1.5	—	V_{DD} + 1.5	V	—

Note 1: At minimum, V_{DD} – 1.5V should not be lower than 1.8V.

2: At maximum, V_{DD} + 1.5V should not be higher than 3.7V.

TABLE 3-2: CURRENT CONSUMPTION(3)

Chip Mode	Min	Typ	Max	Unit	Condition
Sleep	—	0.1	2	µA	Sleep clock disabled, all blocks disabled
Idle	—	65	80	µA	Oscillator and baseband enabled(2)
Frequency Synthesizer	—	1.3	1.7	mA	Frequency synthesizer running
TX	—	25	30	mA	Output power = +10 dBm
TX	—	16	21	mA	Output power = +1 dBm(1)
RX	—	3.0	3.5	mA	—

Note 1: Guaranteed by design and characterization.

2: Crystal C_{LOAD} = 10 pF, C0 = 2.5 pF, R_M = 15 Ohms.

3: Measurement Conditions: Temp = 25°C, V_{DD} = 3.3V, crystal frequency = 12.8 MHz, carrier frequency = 869 or 915 MHz, modulation FSK, data rate = 25 kb/s, F_{DEV} = 50 kHz, fc = 100 kHz, unless otherwise specified.

TABLE 3-3: DIGITAL I/O PIN INPUT SPECIFICATIONS(1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IL}	Input Low Voltage	—	—	0.2 * V_{DD}	V	—
V_{IH}	Input High Voltage	0.8 * V_{DD}	—	—	V	—
I_{IL}	Input Low Leakage Current(2)	-0.5	—	0.5	µA	V_{IL} = 0V
I_{IH}	Input High Leakage Current	-0.5	—	0.5	µA	V_{IH} = V_{DD}, V_{DD} = 3.7
V_{OL}	Digital Low Output Voltage	—	—	0.1 * V_{DD}	—	I_{OL} = 1 mA
V_{OH}	Digital Low Output	0.9 * V_{DD}	—	—	V	I_{OH} = -1 mA

Note 1: Measurement Conditions: T_A = 25°C, V_{DD} = 3.3V, crystal frequency = 12.8 MHz, unless otherwise specified.

2: Negative current is defined as the current sourced by the pin.

3: On Pin 10 (OSC1) and 11 (OSC2), maximum voltages of 1.8V can be applied.

TABLE 3-4: PLL PARAMETERS AC CHARACTERISTICS(1)

Parameter	Min	Typ	Max	Unit	Condition
Frequency Ranges	863	—	870	MHz	Programmable but requires specific BOM
	902	—	928	MHz	
	950	—	960	MHz	
Bit Rate (FSK)	1.56	—	200	kb/s	NRZ
Bit Rate (OOK)	1.56	—	32	kb/s	NRZ
Frequency Deviation (FSK)	33	50	200	kHz	—
Crystal Oscillator Frequency	9	12.8	15	MHz	—
Frequency Synthesizer Step	—	2	—	kHz	Variable, depending on the frequency
Oscillator Wake-up Time	—	1.5	5	ms	From Sleep mode(1)
Frequency Synthesizer Wake-up Time; at most, 10 kHz away from the Target	—	500	800	µs	From Stand-by mode
Frequency Synthesizer Hop Time; at most, 10 kHz away from the Target	—	180	—	µs	200 kHz step
	—	200	—	µs	1 MHz step
	—	250	—	µs	5 MHz step
	—	260	—	µs	7 MHz step
	—	290	—	µs	12 MHz step
	—	320	—	µs	20 MHz step
	—	340	—	µs	27 MHz step

Note 1: Guaranteed by design and characterization

TABLE 3-5: RECEIVER AC CHARACTERISTICS(1)

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity (FSK)	—	-107	—	dBm	869 MHz, BR = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz
	—	-103	—	dBm	869 MHz, BR = 66.7 kb/s, Fdev = 100 kHz, fc = 200 kHz
	—	-105	—	dBm	915 MHz, BR = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz
	—	-101	—	dBm	915 MHz, BR = 66.7 kb/s, Fdev = 100 kHz, fc = 200 kHz
Sensitivity (OOK)	—	-113	—	dBm	869 MHz, 2kb/s NRZ fc – fo = 50 kHz, fo = 50 kHz
	—	-106	—	dBm	869 MHz, 16.7 kb/s NRZ fc – fo = 100 kHz, fo = 100 kHz
	—	-111	—	dBm	915 MHz, 2 kb/s NRZ fc – fo = 50 kHz, fo = 50 kHz
	—	-105	—	dBm	915 MHz, 16.7 kb/s NRZ fc – fo = 100 kHz, fo = 100 kHz
Co-Channel Rejection	—	-12	—	dBc	Modulation as wanted signal
Adjacent Channel Rejection	—	27	—	dB	Offset = 300 kHz, unwanted tone is not modulated
	—	52	—	dB	Offset = 600 kHz, unwanted tone is not modulated
	—	57	—	dB	Offset = 1.2 MHz, unwanted tone is not modulated
Blocking Immunity	—	-48	—	dBm	Offset = 1 MHz, unmodulated
	—	-37	—	dBm	Offset = 2 MHz, unmodulated, no SAW
	—	-33	—	dBm	Offset = 10 MHz, unmodulated, no SAW
Receiver Bandwidth in FSK Mode(2)	50	—	250	kHz	Single side BW, Polyphase Off
Receiver Bandwidth in OOK Mode(2)	50	—	400	kHz	Single side BW, Polyphase On
Input Third Order Intercept Point	—	-28	—	dBm	Interferers at 1 MHz and 1.950 MHz offset
Receiver Wake-up Time	—	280	500	µs	From FS to RX ready
Receiver Wake-up Time	—	600	900	µs	From Stand-by to RX ready
Receiver Hop Time from RX Ready to RX Ready with a Frequency Hop	—	400	—	µs	200 kHz step
	—	400	—	µs	1 MHz step
	—	460	—	µs	5 MHz step
	—	480	—	µs	7 MHz step
	—	520	—	µs	12 MHz step
	—	550	—	µs	20 MHz step
	—	600	—	µs	27 MHz step
RSSI Sampling Time	—	—	1/Fdev	s	From RX ready
RSSI Dynamic Range	—	70	—	dB	Ranging from sensitivity

Note 1: Guaranteed by design and characterization.

2: This reflects the whole receiver bandwidth, as described by conditions for active and passive filters.

TABLE 3-6: TRANSMITTER AC CHARACTERISTICS(1)

Description	Min	Typ	Max	Unit	Condition
RF Output Power, Programmable with 8 Steps of typ. 3 dB	—	+12.5	—	dBm	Maximum power setting.
	—	-8.5	—	dBm	Minimum power setting.
Phase Noise	—	-112	—	dBc/Hz	Measured with a 600 kHz offset at the transmitter output.
Transmitted Spurious	—	—	-47	dBc	At any offset between 200 kHz and 600 kHz, unmodulated carrier, Fdev = 50 kHz.
Transmitter Wake-up Time	—	120	500	µs	From FS to TX ready.
Transmitter Wake-up Time	—	600	900	µs	From standby to TX ready.

Note 1: Guaranteed by design and characterization.

3.2 Timing Specification and Diagram

TABLE 3-7: SPI TIMING SPECIFICATION(1,2,3)

Parameter	Min	Typ	Max	Unit	Condition
SPI Configure Clock Frequency	—	—	6	MHz	—
SPI Data Clock Frequency	—	—	1	MHz	—
Data Hold and Setup Time	2	—	—	µs	—
SDI Setup Time for SPI Configure	250	—	—	ns	—
SDI Setup Time for SPI Data	312	—	—	ns	—
$\overline{\text{CSCON}}$ Low to SCK Rising Edge; SCK Falling Edge to /CSCON High	500	—	—	ns	—
$\overline{\text{CSDATA}}$ Low to SCK Rising Edge; SCK Falling Edge to /CSDATA High	625	—	—	ns	—
$\overline{\text{CSCON}}$ Rising to Falling Edge	500	—	—	ns	—
$\overline{\text{CSDATA}}$ Rising to Falling Edge	625	—	—	ns	—

Note 1: Typical Values: T_A = 25°C, V_{DD} = 3.3V, crystal frequency = 12.8 MHz, unless otherwise specified.

2: Negative current is defined as the current sourced by the pin.

3: On Pin 10 (OSC1) and 11 (OSC2), maximum voltages of 1.8V can be applied.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (January 2010)

This is the initial released version of this document.

NOTES:

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Temperature Range	I = -40ºC to +85ºC (Industrial)
Package	MQ = QFN (Quad Flat, No Lead) T = Tape and Reel

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