

# IGLOO Low Power Flash FPGAs with Flash\*Freeze Technology



## Features and Benefits

### Low Power

- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- 5  $\mu$ W Power Consumption in Flash\*Freeze Mode
- Low Power Active FPGA Operation
- Flash\*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Easy Entry to / Exit from Ultra-Low Power Flash\*Freeze Mode

### High Capacity

- 15 k to 1 Million System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 300 User I/Os

### Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off
- 250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance

### In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except ARM<sup>®</sup>-enabled IGLOO<sup>®</sup> devices) via JTAG (IEEE 1532-compliant)<sup>†</sup>
- FlashLock<sup>®</sup> to Secure FPGA Contents

### High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure

### Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (AGL250 and above)

- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X<sup>†</sup>, and LVCMOS 2.5 V / 5.0 V Input<sup>†</sup>
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (AGL250 and above)
- Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V
- Wide Range Power Supply Voltage Support per JESD8-12, Allowing I/Os to Operate from 1.14 V to 1.575 V
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os<sup>†</sup>
- Programmable Output Slew Rate<sup>†</sup> and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO Family

### Clock Conditioning Circuit (CCC) and PLL<sup>†</sup>

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

### Embedded Memory

- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit<sup>†</sup> RAM Blocks (x1, x2, x4, x9, and x18 organizations)
- True Dual-Port SRAM (except x18)<sup>†</sup>

### ARM Processor Support in IGLOO FPGAs

- M1 IGLOO Devices—Cortex™-M1 Soft Processor Available with or without Debug

IGLOO Devices	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000
ARM-Enabled IGLOO Devices					<b>M1AGL250</b>		<b>M1AGL600</b>	<b>M1AGL1000</b>
System Gates	15 k	30 k	60 k	125 k	250 k	400 k	600 k	1 M
Typical Equivalent Macrocells	128	256	512	1,024	2,048	–	–	–
VersaTiles (D-flip-flops)	384	768	1,536	3,072	6,144	9,216	13,824	24,576
Flash*Freeze Mode (typical, $\mu$ W)	5	5	10	16	24	32	36	53
RAM kbits (1,024 bits)	–	–	18	36	36	54	108	144
4,608-Bit Blocks	–	–	4	8	8	12	24	32
FlashROM Bits	1 k	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP <sup>1</sup>	–	–	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs <sup>2</sup>	–	–	1	1	1	1	1	1
VersaNet Globals <sup>3</sup>	6	6	18	18	18	18	18	18
I/O Banks	2	2	2	2	4	4	4	4
Maximum User I/Os	49	81	96	133	143	194	235	300
Package Pins								
UC/CS		UC81 CS81	CS121	CS196	CS196, <sup>4</sup> QN132 <sup>4,5</sup>	CS196	CS281	CS281
QFN	QN68	QN48, QN68, QN132	QN132	QN132	VQ100 FG144			
VQFP FBGA		VQ100 FG144 <sup>5</sup>	VQ100 FG144	VQ100 FG144		FG144, FG256, FG484	FG144, FG256, FG484	FG144, FG256, FG484

#### Notes:

1. AES is not available for ARM-enabled IGLOO devices.
2. AGL060 in CS121 does not support the PLL.
3. Six chip (main) and twelve quadrant global networks are available for AGL060 and above.
4. The M1AGL250 device does not support this package.
5. Device/package support TBD
6. The IGLOOe datasheet and IGLOOe FPGA Fabric User's Guide provide information on higher densities and additional features.

<sup>†</sup> AGL015 and AGL030 devices do not support this feature.

<sup>‡</sup> Supported only by AGL015 and AGL030 devices.

## I/Os Per Package<sup>1</sup>

IGLOO Devices	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000				
ARM-Enabled IGLOO Devices					M1AGL250 <sup>2</sup>	M1AGL400	M1AGL600	M1AGL1000				
Package	I/O Type											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O <sup>3</sup>	Differential I/O Pairs	Single-Ended I/O <sup>3</sup>	Differential I/O Pairs	Single-Ended I/O <sup>3</sup>	Differential I/O Pairs	Single-Ended I/O <sup>3</sup>	Differential I/O Pairs
QN48	-	34	-	-	-	-	-	-	-	-	-	-
QN68	49	49	-	-	-	-	-	-	-	-	-	-
UC81	-	66	-	-	-	-	-	-	-	-	-	-
CS81	-	66	-	-	-	-	-	-	-	-	-	-
CS121	-	-	96	-	-	-	-	-	-	-	-	-
VQ100	-	77	71	71	68	13	-	-	-	-	-	-
QN132	-	81	80	84	87 <sup>4</sup>	19 <sup>4</sup>	-	-	-	-	-	-
CS196	-	-	-	133	143	35	143	35	-	-	-	-
FG144	-	-	96 <sup>4</sup>	97	97	24	97	25	97	25	97	25
FG256 <sup>5</sup>	-	-	-	-	-	-	178	38	177	43	177	44
CS281	-	-	-	-	-	-	-	-	215	53	215	53
FG484 <sup>5</sup>	-	-	-	-	-	-	194	38	235	60	300	74

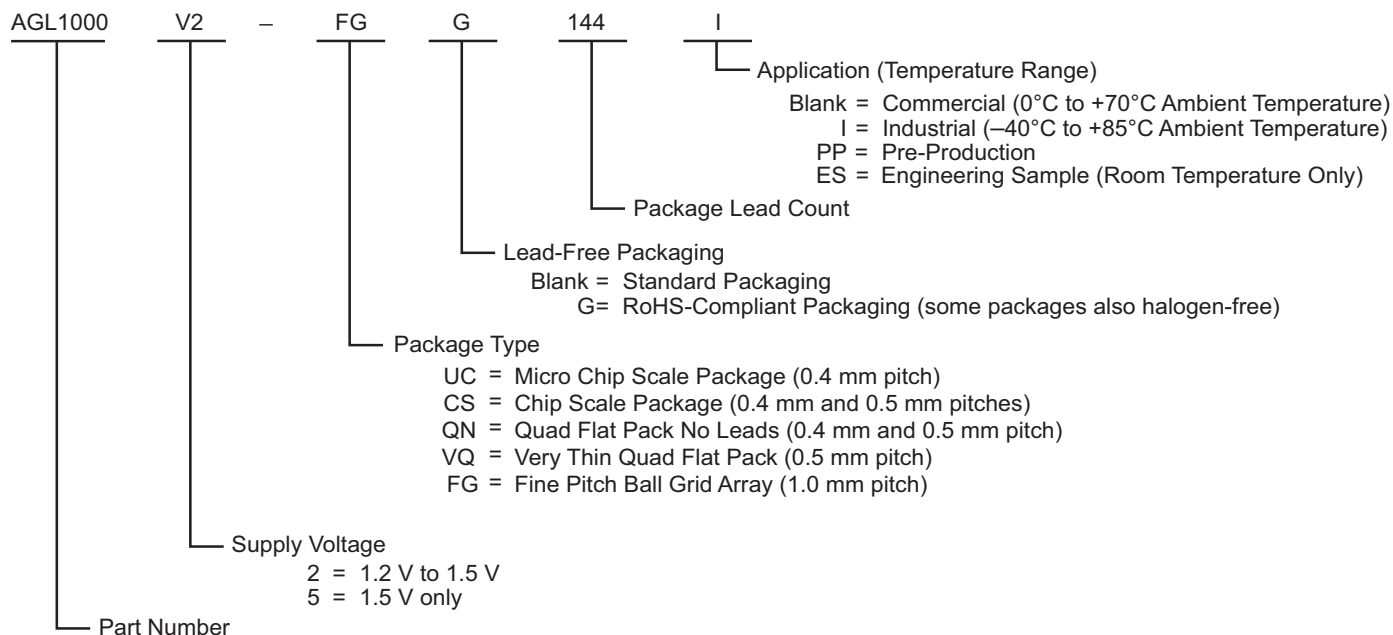
### Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the IGLOO FPGA Fabric User's Guide to ensure compliance with design and board migration requirements.
- The M1AGL250 device does not support QN132 or CS196 packages. Refer to the IGLOO FPGA Fabric User's Guide for position assignments of the 15 LVPECL pairs.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- Device/package support TBD.
- FG256 and FG484 are footprint-compatible packages.
- When the Flash\*Freeze pin is used to directly enable Flash\*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.
- "G" indicates RoHS-compliant packages. Refer to "IGLOO Ordering Information" on page III for the location of the "G" in the part number.

Table 1 • IGLOO FPGAs Package Sizes Dimensions

Package	UC81	CS81	CS121	QN68	QN132	CS196	CS281	FG144	VQ100	FG256	FG484
Length x Width (mm\mm)	4 x 4	5 x 5	6 x 6	8 x 8	8 x 8	8 x 8	10 x 10	13 x 13	14 x 14	17 x 17	23 x 23
Nominal Area (mm <sup>2</sup> )	16	25	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

## IGLOO Ordering Information



### IGLOO Devices

AGL015 = 15,000 System Gates  
 AGL030 = 30,000 System Gates  
 AGL060 = 60,000 System Gates  
 AGL125 = 125,000 System Gates  
 AGL250 = 250,000 System Gates  
 AGL400 = 400,000 System Gates  
 AGL600 = 600,000 System Gates  
 AGL1000 = 1,000,000 System Gates

### IGLOO Devices with Cortex-M1

M1AGL250 = 250,000 System Gates  
 M1AGL600 = 600,000 System Gates  
 M1AGL1000 = 1,000,000 System Gates

*Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.*

## Temperature Grade Offerings

Package	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000
					M1AGL250 <sup>4</sup>		M1AGL600	M1AGL1000
QN48	–	C, I	–	–	–	–	–	–
QN68	C, I	–	–	–	–	–	–	–
UC81	–	C, I	–	–	–	–	–	–
CS81	–	C, I	–	–	–	–	–	–
CS121	–	–	C, I	–	–	–	–	–
VQ100	–	C, I	C, I	C, I	C, I	–	–	–
QN132	–	C, I	C, I <sup>3</sup>	C, I	C, I <sup>3</sup>	–	–	–
CS196	–	–	–	C, I	C, I	C, I	–	–
FG144	–	–	C, I <sup>3</sup>	C, I	C, I	C, I	C, I	C, I
FG256	–	–	–	–	–	C, I	C, I	C, I
CS281	–	–	–	–	–	–	C, I	C, I
CS284	–	–	–	–	–	–	–	–
FG484	–	–	–	–	–	C, I	C, I	C, I

### Notes:

1. C = Commercial temperature range: 0°C to 70°C ambient temperature.
2. I = Industrial temperature range: –40°C to 85°C ambient temperature.
3. Device/package support TBD.
4. The M1AGL250 device does not support FG256 or QN132 packages.

## IGLOO Device Status

IGLOO Devices	Status	M1 IGLOO Devices	Status
AGL015	Production		
AGL030	Production		
AGL060	Production		
AGL125	Production		
AGL250	Production	M1AGL250	Production
AGL400	Production		
AGL600	Production	M1AGL600	Production
AGL1000	Production	M1AGL1000	Production

References made to IGLOO devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Actel representative for device availability:

<http://www.actel.com/contact/default.aspx>.

### **AGL015 and AGL030**

The AGL015 and AGL030 are architecturally compatible; there are no RAM or PLL features.

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# 1 – IGLOO Device Family Overview

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## General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash\*Freeze technology used in IGLOO devices enables entering and exiting an ultra-low power mode that consumes as little as 5  $\mu$ W while retaining SRAM and register data. Flash\*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption (from 12  $\mu$ W) while the IGLOO device is completely functional in the system. This allows the IGLOO device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). IGLOO is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGL015 and AGL030 devices have no PLL or RAM support. IGLOO devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

M1 IGLOO devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOO device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Actel for use in M1 IGLOO FPGAs.

The ARM-enabled devices have Actel ordering numbers that begin with M1AGL and do not support AES decryption.

## Flash\*Freeze Technology

The IGLOO device offers unique Flash\*Freeze technology, allowing the device to enter and exit ultra-low power Flash\*Freeze mode. IGLOO devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash\*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOO device enters Flash\*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash\*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOO devices the best fit for portable electronics.

## Flash Advantages

### Low Power

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash\*Freeze technology, gives the IGLOO device the lowest total system power offered by any FPGA.

### Security

The nonvolatile, flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO device provides the most impenetrable security for programmable logic designs.

### Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### Live at Power-Up

The Actel flash-based IGLOO devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOO devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO flash FPGAs allow the user to quickly enter and exit Flash\*Freeze mode. This is done almost instantly (within 1  $\mu$ s) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.



## **Reduced Cost of Ownership**

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

## **Firm-Error Immunity**

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## **Advanced Flash Technology**

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

## **Advanced Architecture**

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

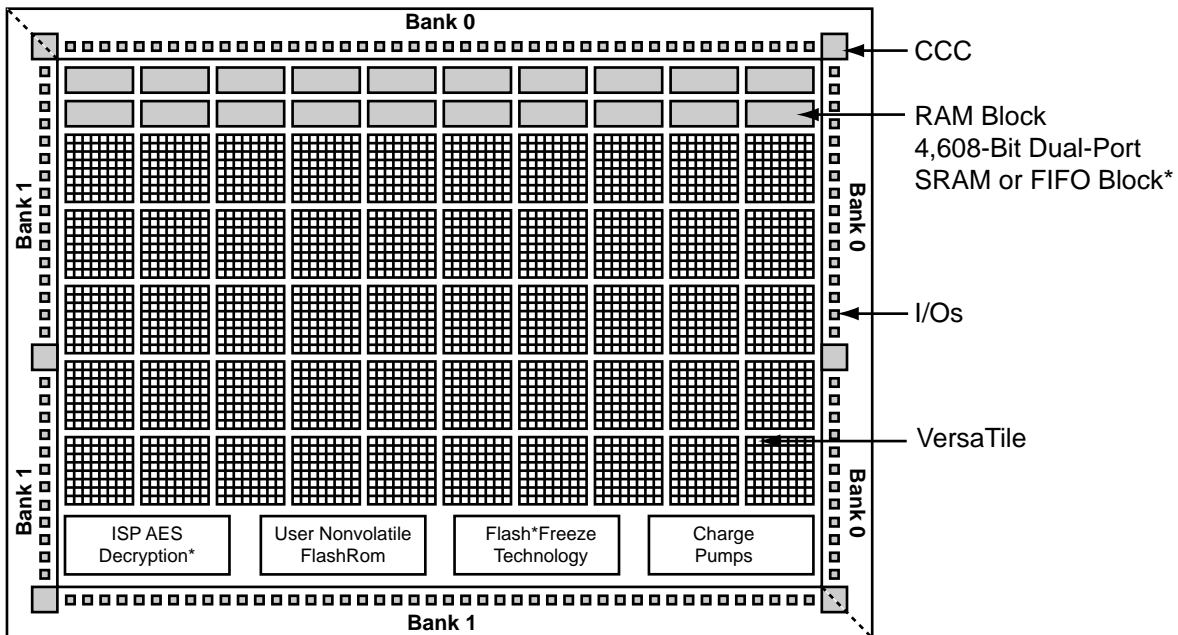
- Flash\*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory<sup>†</sup>
- Extensive CCCs and PLLs<sup>†</sup>
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

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<sup>†</sup> The AGL015 and AGL030 do not support PLL or SRAM.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface.



Note: \*Not supported by AGL015 and AGL030 devices

Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)

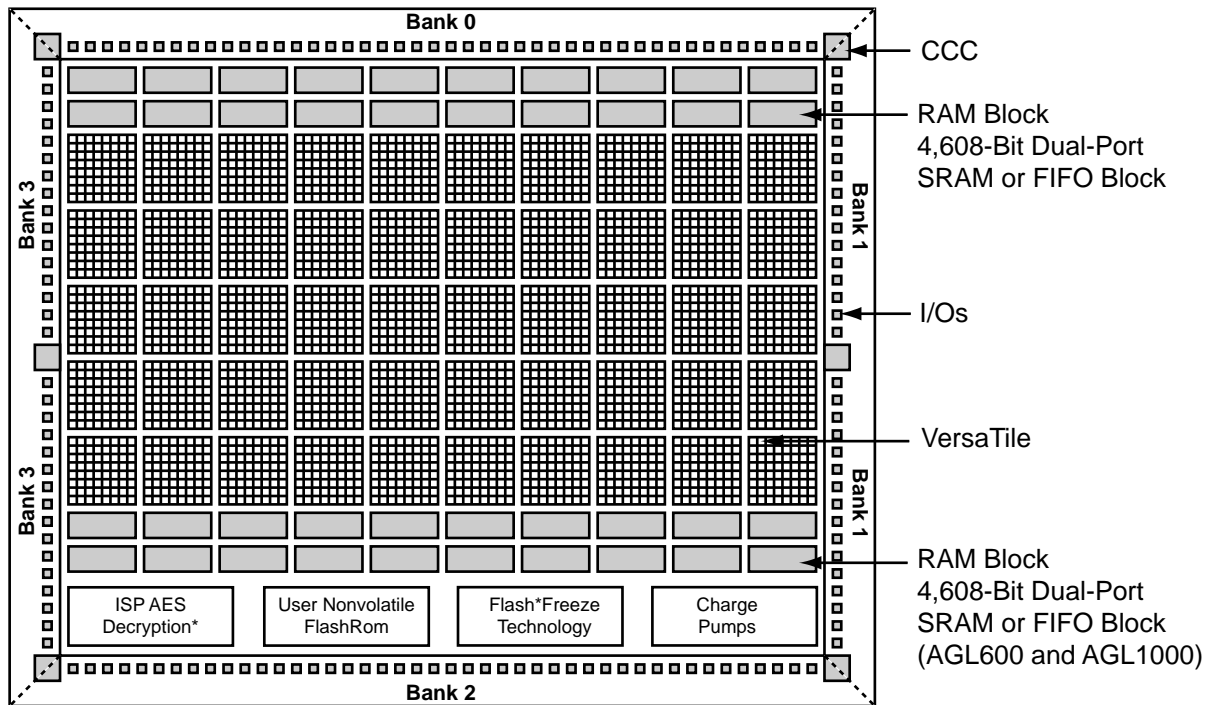


Figure 1-2 • IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)

### Flash\*Freeze Technology

The IGLOO device has an ultra-low power static mode, called Flash\*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash\*Freeze technology enables the user to quickly (within 1  $\mu$ s) enter and exit Flash\*Freeze mode by activating the Flash\*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash\*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5  $\mu$ W in this mode.

Flash\*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash\*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash\*Freeze pin as a regular I/O if Flash\*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 12  $\mu$ W) and dynamic capabilities of the IGLOO device. Refer to [Figure 1-3](#) for an illustration of entering/exiting Flash\*Freeze mode.

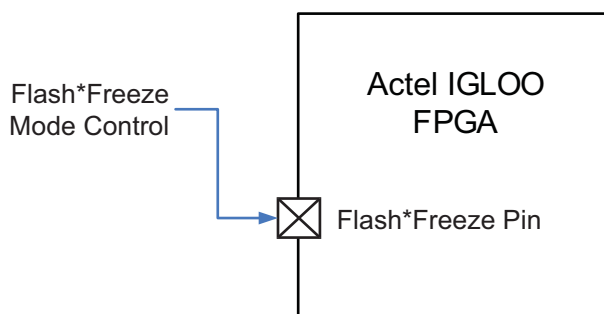


Figure 1-3 • IGLOO Flash\*Freeze Mode

### VersaTiles

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The IGLOO VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-4](#) for VersaTile configurations.

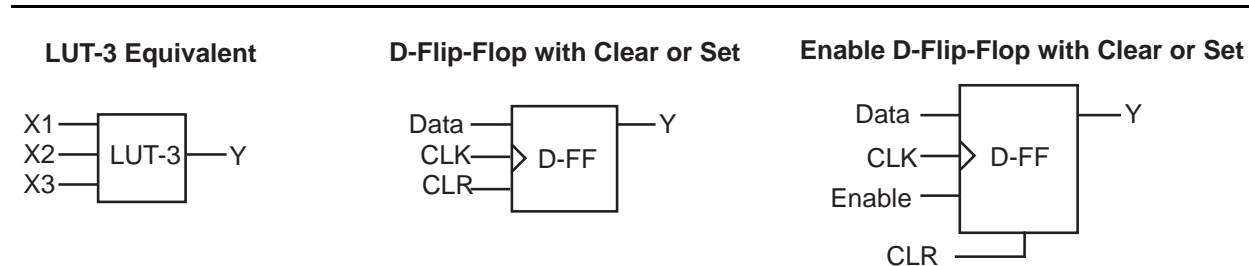


Figure 1-4 • VersaTile Configurations

## **User Nonvolatile FlashROM**

Actel IGLOO devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGL015 and AGL030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## **SRAM and FIFO**

IGLOO devices (except the AGL015 and AGL030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, and 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGL015 and AGL030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## **PLL and CCC**

IGLOO devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO family contains six CCCs. One CCC (center west side) has a PLL. The AGL015 and AGL030 do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ( $f_{IN\_CCC}$ ) = 1.5 MHz up to 250 MHz
- Output frequency range ( $f_{OUT\_CCC}$ ) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz /  $f_{OUT\_CCC}$  (for PLL only)

### Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

### I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1).

**Table 1 • I/O Standards Supported**

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west banks of AGL250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of AGL250 and larger devices All banks of AGL060 and AGL125K	✓	✓	Not supported
Standard	All banks of AGL015 and AGL030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

## Wide Range I/O Support

Actel IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## 2 – IGLOO DC and Switching Characteristics

### General Specifications

#### Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

**Table 2-1 • Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	−0.3 to 1.65	V
VJTAG	JTAG DC voltage	−0.3 to 3.75	V
VPUMP	Programming voltage	−0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	−0.3 to 1.65	V
VCCI and VMV <sup>3</sup>	DC I/O buffer supply voltage	−0.3 to 3.75	V
VI	I/O input voltage	−0.3 V to 3.6 V (when I/O hot insertion mode is enabled) −0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T <sub>STG</sub> <sup>2</sup>	Storage Temperature	−65 to +150	°C
T <sub>J</sub> <sup>2</sup>	Junction Temperature	+125	°C

**Notes:**

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4 on page 2-3](#).
2. For flash programming and retention, maximum limits refer to [Table 2-3 on page 2-2](#), and for recommended operating limits, refer to [Table 2-2 on page 2-2](#).
3. VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the [IGLOO FPGA Fabric User's Guide](#) for further information.

**Table 2-2 • Recommended Operating Conditions**<sup>4</sup>

Symbol	Parameter	Commercial	Industrial	Units	
T <sub>A</sub>	Ambient Temperature	0 to +70	-40 to +85	°C	
T <sub>J</sub>	Junction Temperature <sup>6</sup>	0 to +85	-40 to +100	°C	
VCC <sup>3</sup>	1.5 V DC core supply voltage <sup>1</sup>	1.425 to 1.575	1.425 to 1.575	V	
	1.2 V–1.5 V wide range DC core supply voltage <sup>2,10</sup>	1.14 to 1.575	1.14 to 1.575	V	
VJTAG	JTAG DC voltage	1.4 to 3.6	1.4 to 3.6	V	
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation <sup>5</sup>	0 to 3.45	0 to 3.45	V
VCCPLL <sup>7</sup>	Analog power supply (PLL)	1.5 V DC core supply voltage <sup>1</sup>	1.4 to 1.6	1.4 to 1.6	V
		1.2 V –1.5 V DC core supply voltage <sup>2,10</sup>	1.14 to 1.26	1.14 to 1.26	V
VCCI and VMV <sup>8</sup>	1.2 V DC core supply voltage <sup>2</sup>	1.14 to 1.26	1.14 to 1.26	V	
	1.2 V DC wide range DC supply voltage <sup>2</sup>	1.14 to 1.575	1.14 to 1.575	V	
	1.5 V DC supply voltage	1.425 to 1.575	1.425 to 1.575	V	
	1.8 V DC supply voltage	1.7 to 1.9	1.7 to 1.9	V	
	2.5 V DC supply voltage	2.3 to 2.7	2.3 to 2.7	V	
	3.0 V DC supply voltage <sup>9</sup>	2.7 to 3.6	2.7 to 3.6	V	
	3.3 V DC supply voltage	3.0 to 3.6	3.0 to 3.6	V	
	LVDS differential I/O	2.375 to 2.625	2.375 to 2.625	V	
LVPECL differential I/O	3.0 to 3.6	3.0 to 3.6	V		

**Notes:**

1. For IGLOO<sup>®</sup> V5 devices
2. For IGLOO V2 devices only, operating at VCCI ≥ VCC.
3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-24 on page 2-24](#). VCCI should be at the same voltage within a given I/O bank.
4. All parameters representing voltages are measured with respect to GND unless otherwise specified.
5. VPUMP can be left floating during operation (not programming mode).
6. To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.
7. VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the [IGLOO FPGA Fabric User's Guide](#) for further information.
8. VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the [IGLOO FPGA Fabric User's Guide](#) for further information.
9. 3.3 V wide range is compliant to the JESD-8B specification and supports 3.0 V VCCI operation.
10. All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by 1.2 V supply must switch the core supply to 1.5 V for in-system programming.

**Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature**<sup>1</sup>

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T <sub>STG</sub> (°C) <sup>2</sup>	Maximum Operating Junction Temperature T <sub>J</sub> (°C) <sup>2</sup>
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

**Notes:**

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.



**Table 2-4 • Overshoot and Undershoot Limits<sup>1</sup>**

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle <sup>2</sup>	Maximum Overshoot/Undershoot <sup>2</sup>
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

**Notes:**

1. Based on reliability requirements at junction temperature at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#).

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-1 on page 2-4](#) and [Figure 2-2 on page 2-5](#)).
2.  $VCCI > VCC - 0.75 \text{ V}$  (typical)
3. Chip is in the operating mode.

**VCCI Trip Point:**

Ramping up (V5 devices):  $0.6 \text{ V} < \text{trip\_point\_up} < 1.2 \text{ V}$

Ramping down (V5 Devices):  $0.5 \text{ V} < \text{trip\_point\_down} < 1.1 \text{ V}$

Ramping up (V2 devices):  $0.75 \text{ V} < \text{trip\_point\_up} < 1.05 \text{ V}$

Ramping down (V2 devices):  $0.65 \text{ V} < \text{trip\_point\_down} < 0.95 \text{ V}$

**VCC Trip Point:**

Ramping up (V5 devices):  $0.6 \text{ V} < \text{trip\_point\_up} < 1.1 \text{ V}$

Ramping down (V5 devices):  $0.5 \text{ V} < \text{trip\_point\_down} < 1.0 \text{ V}$

Ramping up (V2 devices):  $0.65 \text{ V} < \text{trip\_point\_up} < 1.05 \text{ V}$

Ramping down (V2 devices):  $0.55 \text{ V} < \text{trip\_point\_down} < 0.95 \text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

### PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ( $0.75\text{ V} \pm 0.25\text{ V}$  for V5 devices, and  $0.75\text{ V} \pm 0.2\text{ V}$  for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC<sup>®</sup>3* and *ProASIC3E* FPGA fabric user's guides for information on clock and lock recovery.

### Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

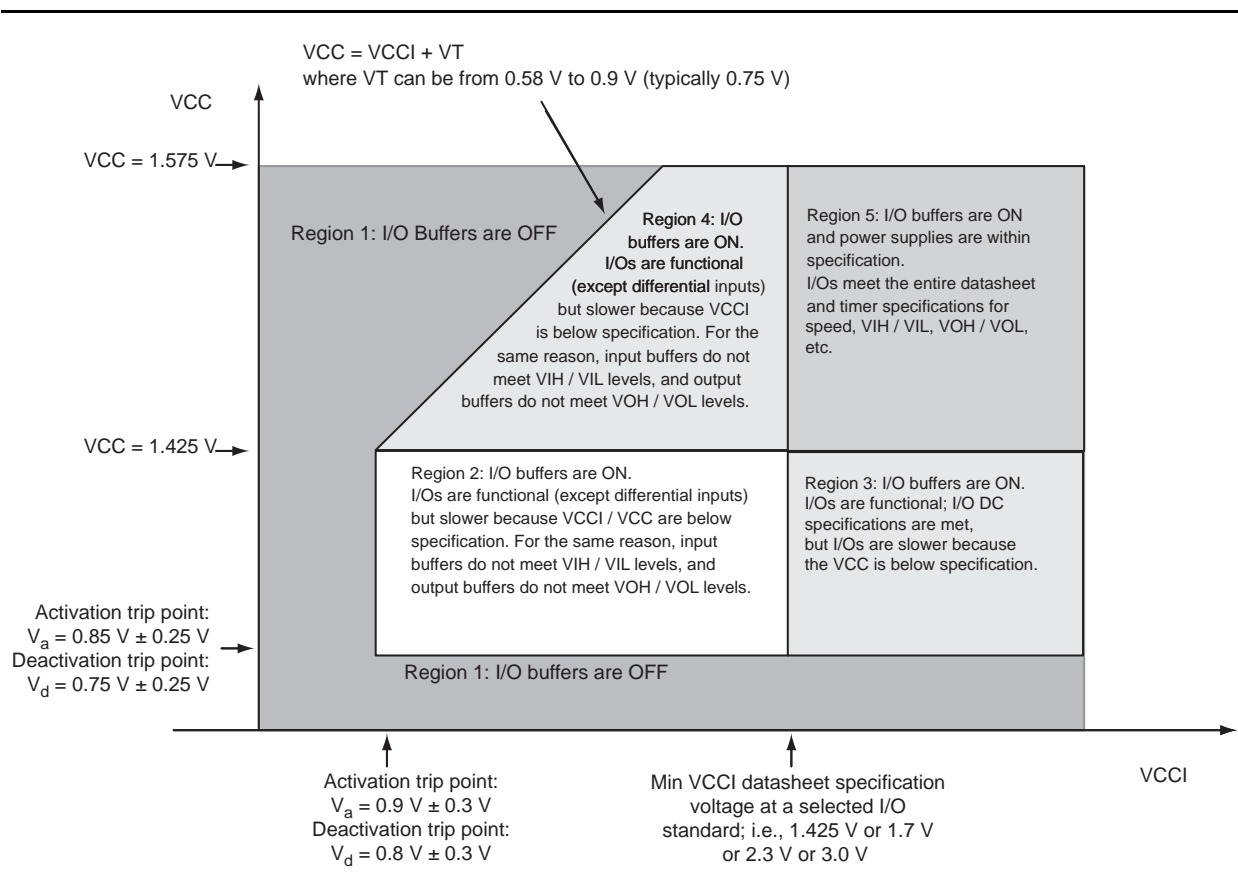
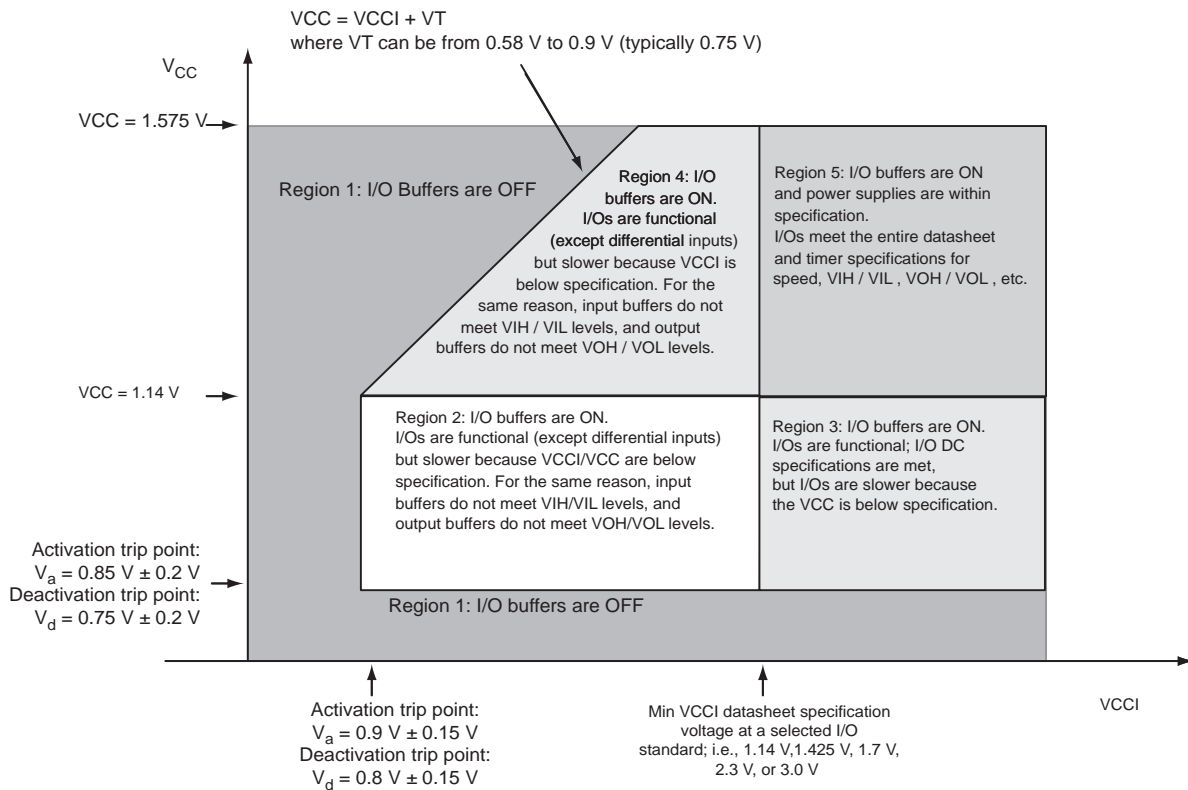


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels



**Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

## Thermal Characteristics

### Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

$T_A$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient  $\Delta T = \theta_{ja} * P$

$\theta_{ja}$  = Junction-to-ambient of the package.  $\theta_{ja}$  numbers are located in [Table 2-5 on page 2-6](#).

P = Power dissipation

### Package Thermal Characteristics

The device junction-to-case thermal resistivity is  $\theta_{jc}$  and the junction-to-ambient air thermal resistivity is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for the AGL1000-FG484 package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{110^\circ\text{C} - 70^\circ\text{C}}{23.3^\circ\text{C/W}} = 1.71 \text{ W}$$

EQ 2

**Table 2-5 • Package Thermal Resistivities**

Package Type	Device	Pin Count	$\theta_{jc}$	$\theta_{ja}$			Unit
				Still Air	1 m/s	2.5 m/s	
Quad Flat No Lead	AGL030	132	TBD	21.4	16.8	15.3	C/W
	AGL060	132	TBD	21.2	16.6	15.0	C/W
	AGL125	132	TBD	21.1	16.5	14.9	C/W
	AGL250	132	TBD	21.0	16.4	14.8	C/W
	AGL030	68	13.4	68.4	TBD	TBD	C/W
Very Thin Quad Flat Pack (VQFP)*		100	10.0	35.3	29.4	27.1	C/W
Chip Scale Package (CSP)*		196	TBD	57.8	47.6	43.3	C/W
Chip Scale Package (CSP)	AGLN020	81	12.5	34.0	29.9	28.5	C/W
	AGL030	81	12.4	32.8	28.5	27.2	C/W
	AGL060	81	11.1	28.8	24.8	23.5	C/W
	AGLN250	81	10.4	28.0	23.4	22.0	C/W
	AGL250	81	10.4	26.9	22.3	20.9	C/W
Micro Chip Scale Package (UC)	AGLN020	81	18.2	44.3	39.0	37.5	C/W
	AGL030	81	16.9	40.6	35.2	33.7	C/W
Fine Pitch Ball Grid Array (FBGA)	AGL060	144	18.6	55.2	49.4	47.2	C/W
	AGL1000	144	6.3	31.6	26.2	24.2	C/W
	AGL400	144	6.8	37.6	31.2	29.0	C/W
	AGL250	256	12.0	38.6	34.7	33.0	C/W
	AGL1000	256	6.6	28.1	24.4	22.7	C/W
	AGLE3000	324	2.9	24.0	TBD	TBD	C/W
	AGL1000	484	8.0	23.3	19.0	16.7	C/W

Note: \*Thermal Resistances for other device-package combinations will be posted on the next revision.

#### Disclaimer:

The simulation for determining the junction-to-air thermal resistance is based on JEDEC standards (JESD51) and assumptions made in building the model. Junction-to-case is based on SEMI G38-88. JESD51 is only used for comparing one package to another package, provided the two tests use the same condition. They have little relevance in actual application and therefore should be used with a degree of caution.

## Temperature and Voltage Derating Factors

**Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ )**  
For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ( $^\circ\text{C}$ )						
	$-40^\circ\text{C}$	$-20^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$100^\circ\text{C}$
1.425	0.934	0.953	0.971	1.000	1.007	1.013	1.425
1.500	0.855	0.874	0.891	0.917	0.924	0.929	1.500
1.575	0.799	0.816	0.832	0.857	0.864	0.868	1.575

**Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$ )**  
For IGLOO V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ( $^\circ\text{C}$ )						
	$-40^\circ\text{C}$	$-20^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$100^\circ\text{C}$
1.14	0.967	0.973	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.869	0.874	0.885	0.894	0.899	0.902
1.26	0.794	0.799	0.803	0.814	0.821	0.827	0.830

## Calculating Power Dissipation

### Quiescent Supply Current

Quiescent supply current ( $I_{DD}$ ) calculation depends on multiple factors, including operating voltages ( $V_{CC}$ ,  $V_{CCI}$ , and  $V_{JTAG}$ ), operating temperature, system clock frequency, and power modes usage. Actel recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature

**Table 2-8 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics, IGLOO Flash\*Freeze Mode\***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
Typical ( $25^\circ\text{C}$ )	1.2 V	4	4	8	13	20	27	30	44	$\mu\text{A}$
	1.5 V	6	6	10	18	34	51	72	127	$\mu\text{A}$

*Note:*  $I_{DD}$  includes  $V_{CC}$ ,  $V_{PUMP}$ ,  $V_{CCI}$ ,  $V_{JTAG}$ , and  $V_{CCPLL}$  currents. Values do not include I/O static contribution ( $PDC6$  and  $PDC7$ ).

**Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode\***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note:  $I_{DD}$  includes  $V_{CC}$ ,  $V_{PUMP}$ , and  $V_{CCPLL}$  currents. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).

**Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode**

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	μA

Note:  $I_{DD}$  includes  $V_{CC}$ ,  $V_{PUMP}$ ,  $V_{CCI}$ ,  $V_{JTAG}$ , and  $V_{CCPLL}$  currents. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).

**Table 2-11 • Quiescent Supply Current (IDD), No IGLOO Flash\*Freeze Mode<sup>1</sup>**

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
<b>I<sub>CCA</sub> Current<sup>2</sup></b>										
Typical (25°C)	1.2 V	5	6	10	13	18	25	28	42	μA
	1.5 V	14	16	20	28	44	66	82	137	μA
<b>I<sub>CCI</sub> or I<sub>JTAG</sub> Current<sup>3, 4</sup></b>										
V <sub>CCI</sub> /V <sub>JTAG</sub> = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
V <sub>CCI</sub> /V <sub>JTAG</sub> = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
V <sub>CCI</sub> /V <sub>JTAG</sub> = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
V <sub>CCI</sub> /V <sub>JTAG</sub> = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
V <sub>CCI</sub> /V <sub>JTAG</sub> = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

**Notes:**

1. To calculate total device I<sub>DD</sub>, multiply the number of banks used by I<sub>CCI</sub> and add I<sub>CCA</sub> contribution.
2. Includes VCC, VPUMP, and VCCPLL currents.
3. Per V<sub>CCI</sub> or V<sub>JTAG</sub> bank.
4. Values do not include I/O static contribution (PDC6 and PDC7).

## Power per I/O Pin

**Table 2-12 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings  
Applicable to Advanced I/O Banks**

	VCCI (V)	Static Power PDC6 (mW) <sup>1</sup>	Dynamic Power PAC9 (μW/MHz) <sup>2</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.27
3.3V LVCMOS Wide Range <sup>3</sup>	3.3	–	16.27
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.61
1.5 V LVCMOS (JESD8-11)	1.5	–	0.96
1.2 V LVCMOS <sup>4</sup>	1.2	–	0.58
1.2 V LVCMOS Wide Range <sup>4</sup>	1.2	–	0.58
3.3 V PCI	3.3	–	17.67
3.3 V PCI-X	3.3	–	17.67
<b>Differential</b>			
LVDS	2.5	2.26	23.39
LVPECL	3.3	5.72	59.05

**Notes:**

1.  $P_{DC6}$  is the static power (where applicable) measured on VCCI.
2.  $P_{AC9}$  is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable for IGLOO V2 devices only

**Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings  
Applicable to Standard Plus I/O Banks**

	VCCI (V)	Static Power PDC6 (mW) <sup>1</sup>	Dynamic Power PAC9 (μW/MHz) <sup>2</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.41
3.3V LVCMOS Wide Range <sup>3</sup>	3.3	–	16.41
2.5 V LVCMOS	2.5	–	4.75
1.8 V LVCMOS	1.8	–	1.66
1.5 V LVCMOS (JESD8-11)	1.5	–	1.00
1.2 V LVCMOS <sup>4</sup>	1.2	–	0.61
1.2 V LVCMOS Wide Range <sup>4</sup>	1.2	–	0.61
3.3 V PCI	3.3	–	17.78
3.3 V PCI-X	3.3	–	17.78

**Notes:**

1.  $P_{DC6}$  is the static power (where applicable) measured on VCCI.
2.  $P_{AC9}$  is the total dynamic power measured on VCCI.
3. Applicable for IGLOO V2 devices only.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.



**Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings  
Applicable to Standard I/O Banks**

	VCCI (V)	Static Power PDC6 (mW) <sup>1</sup>	Dynamic Power PAC9 (μW/MHz) <sup>2</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3V LVCMOS Wide Range <sup>3</sup>	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.64
1.8 V LVCMOS	1.8	–	2.63
1.5 V LVCMOS (JESD8-11)	1.5	–	1.97
1.2 V LVCMOS <sup>4</sup>	1.2	–	0.57
1.2 V LVCMOS Wide Range <sup>4</sup>	1.2	–	0.57

**Notes:**

1. PDC6 is the static power (where applicable) measured on VCCI.
2. PAC9 is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable for IGLOO V2 devices only.

**Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings<sup>1</sup>  
Applicable to Advanced I/O Banks**

	C <sub>LOAD</sub> (pF)	VCCI (V)	Static Power PDC7 (mW) <sup>2</sup>	Dynamic Power PAC10 (μW/MHz) <sup>3</sup>
<b>Single-Ended</b>				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	136.95
3.3V LVCMOS Wide Range <sup>4</sup>	5	3.3	–	136.95
2.5 V LVCMOS	5	2.5	–	76.84
1.8 V LVCMOS	5	1.8	–	49.31
1.5 V LVCMOS (JESD8-11)	5	1.5	–	33.36
1.2 V LVCMOS <sup>5</sup>	5	1.2	–	16.24
1.2 V LVCMOS Wide Range <sup>5</sup>	5	1.2	–	16.24
3.3 V PCI	10	3.3	–	194.05
3.3 V PCI-X	10	3.3	–	194.05
<b>Differential</b>				
Differential				
LVDS	–	2.5	7.74	156.22
LVPECL	–	3.3	19.54	339.35

**Notes:**

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P<sub>DC7</sub> is the static power (where applicable) measured on VCCI.
3. P<sub>AC10</sub> is the total dynamic power measured on VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
5. Applicable for IGLOO V2 devices only.

**Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings<sup>1</sup>  
Applicable to Standard Plus I/O Banks**

	$C_{LOAD}$ (pF)	VCCI (V)	Static Power PDC7 (mW) <sup>2</sup>	Dynamic Power PAC10 ( $\mu$ W/MHz) <sup>3</sup>
<b>Single-Ended</b>				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	122.16
3.3V LVCMOS Wide Range <sup>4</sup>	5	3.3	–	122.16
2.5 V LVCMOS	5	2.5	–	68.37
1.8 V LVCMOS	5	1.8	–	34.53
1.5 V LVCMOS (JESD8-11)	5	1.5	–	23.66
1.2 V LVCMOS <sup>5</sup>	5	1.2	–	14.90
1.2 V LVCMOS Wide Range <sup>5</sup>	5	1.2	–	14.90
3.3 V PCI	10	3.3	–	181.06
3.3 V PCI-X	10	3.3	–	181.06

**Notes:**

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2.  $P_{DC7}$  is the static power (where applicable) measured on VCCI.
3.  $P_{AC10}$  is the total dynamic power measured on VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
5. Applicable for IGLOO V2 devices only.

**Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings<sup>1</sup>  
Applicable to Standard I/O Banks**

	$C_{LOAD}$ (pF)	VCCI (V)	Static Power PDC7 (mW) <sup>2</sup>	Dynamic Power PAC10 ( $\mu$ W/MHz) <sup>3</sup>
<b>Single-Ended</b>				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	104.38
3.3V LVCMOS Wide Range <sup>4</sup>	5	3.3	–	104.38
2.5 V LVCMOS	5	2.5	–	59.86
1.8 V LVCMOS	5	1.8	–	31.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	21.96
1.2 V LVCMOS <sup>5</sup>	5	1.2	–	13.49
1.2 V LVCMOS Wide Range <sup>5</sup>	5	1.2	–	13.49

**Notes:**

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2.  $P_{DC7}$  is the static power (where applicable) measured on VCCI.
3.  $P_{AC10}$  is the total dynamic power measured on VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
5. Applicable for IGLOO V2 devices only.

## Power Consumption of Various Internal Resources

**Table 2-18 • Different Components Contributing to Dynamic Power Consumption in IGLOO Devices For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power ( $\mu\text{W}/\text{MHz}$ )							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PAC1	Clock contribution of a Global Rib	14.48	12.77	12.77	11.03	11.03	9.3	9.3	9.3
PAC2	Clock contribution of a Global Spine	2.48	1.85	1.58	1.58	0.81	0.81	0.41	0.41
PAC3	Clock contribution of a VersaTile row	0.81							
PAC4	Clock contribution of a VersaTile used as a sequential module	0.11							
PAC5	First contribution of a VersaTile used as a sequential module	0.057							
PAC6	Second contribution of a VersaTile used as a sequential module	0.207							
PAC7	Contribution of a VersaTile used as a combinatorial module	0.17							
PAC8	Average contribution of a routing net	0.7							
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-10 through Table 2-14 on page 2-11.							
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 on page 2-11 through Table 2-17 on page 2-12.							
PAC11	Average contribution of a RAM block during a read operation	25.00							
PAC12	Average contribution of a RAM block during a write operation	30.00							
PAC13	Dynamic contribution PLL	2.70							

\* For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Actel Libero® Integrated Design Environment (IDE).

**Table 2-19 • Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-11 on page 2-9.							
PDC2	Array static power in Static (Idle) mode	See Table 2-10 on page 2-8.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-8 on page 2-7.							
PDC4	Static PLL contribution	1.84							
PDC5	Bank quiescent power (V <sub>CCI</sub> -dependent)	See Table 2-11 on page 2-9.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-10 through Table 2-14 on page 2-11.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-15 on page 2-11 through Table 2-17 on page 2-12.							

\* For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Actel Libero® Integrated Design Environment (IDE).

**Table 2-20 • Different Components Contributing to Dynamic Power Consumption in IGLOO Devices For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power ( $\mu\text{W}/\text{MHz}$ )							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PAC1	Clock contribution of a Global Rib	9.28	8.19	8.19	7.07	7.07	5.96	5.96	5.96
PAC2	Clock contribution of a Global Spine	1.59	1.19	1.01	1.01	0.52	0.52	0.26	0.26
PAC3	Clock contribution of a VersaTile row	0.52							
PAC4	Clock contribution of a VersaTile used as a sequential module	0.07							
PAC5	First contribution of a VersaTile used as a sequential module	0.045							
PAC6	Second contribution of a VersaTile used as a sequential module	0.186							
PAC7	Contribution of a VersaTile used as a combinatorial module	0.11							
PAC8	Average contribution of a routing net	0.45							
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-10 through Table 2-14 on page 2-11.							
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 on page 2-11 through Table 2-17 on page 2-12.							
PAC11	Average contribution of a RAM block during a read operation	25.00							
PAC12	Average contribution of a RAM block during a write operation	30.00							
PAC13	Dynamic PLL contribution	2.10							

\* For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.

**Table 2-21 • Different Components Contributing to the Static Power Consumption in IGLOO Device For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-11 on page 2-9.							
PDC2	Array static power in Static (Idle) mode	See Table 2-10 on page 2-8.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-8 on page 2-7.							
PDC4	Static PLL contribution	0.90							
PDC5	Bank quiescent power (VCCI-Dependent)	See Table 2-11 on page 2-9.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-10 through Table 2-14 on page 2-11.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-15 on page 2-11 through Table 2-17 on page 2-12.							

\* For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Actel Libero<sup>®</sup> Integrated Design Environment (IDE).

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-22 on page 2-19](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-23 on page 2-19](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-23 on page 2-19](#). The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption— $P_{TOTAL}$

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$P_{STAT}$  is the total static power consumption.

$P_{DYN}$  is the total dynamic power consumption.

#### Total Static Power Consumption— $P_{STAT}$

$$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$$

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$N_{BANKS}$  is the number of I/O banks powered in the design.

#### Total Dynamic Power Consumption— $P_{DYN}$

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

#### Global Clock Contribution— $P_{CLOCK}$

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

$N_{SPINE}$  is the number of global spines used in the user design—guidelines are provided in [Table 2-22 on page 2-19](#).

$N_{ROW}$  is the number of VersaTile rows used in the design—guidelines are provided in [Table 2-22 on page 2-19](#).

$F_{CLK}$  is the global clock signal frequency.

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$ ,  $P_{AC2}$ ,  $P_{AC3}$ , and  $P_{AC4}$  are device-dependent.

#### Sequential Cells Contribution— $P_{S-CELL}$

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-22 on page 2-19](#).

$F_{CLK}$  is the global clock signal frequency.

**Combinatorial Cells Contribution— $P_{C-CELL}$** 

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-22 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**Routing Net Contribution— $P_{NET}$** 

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-22 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**I/O Input Buffer Contribution— $P_{INPUTS}$** 

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 2-22 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**I/O Output Buffer Contribution— $P_{OUTPUTS}$** 

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 2-22 on page 2-19.

$\beta_1$  is the I/O buffer enable rate—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**RAM Contribution— $P_{MEMORY}$** 

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

$N_{BLOCKS}$  is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$  is the memory read clock frequency.

$\beta_2$  is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$  is the memory write clock frequency.

$\beta_3$  is the RAM enable rate for write operations—guidelines are provided in Table 2-23 on page 2-19.

**PLL Contribution— $P_{PLL}$** 

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

$F_{CLKOUT}$  is the output clock frequency.<sup>1</sup>

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ( $P_{AC13} * F_{CLKOUT}$  product) to the total PLL contribution.



## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - ...
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate =  $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

**Table 2-22 • Toggle Rate Guidelines Recommended for Power Calculation**

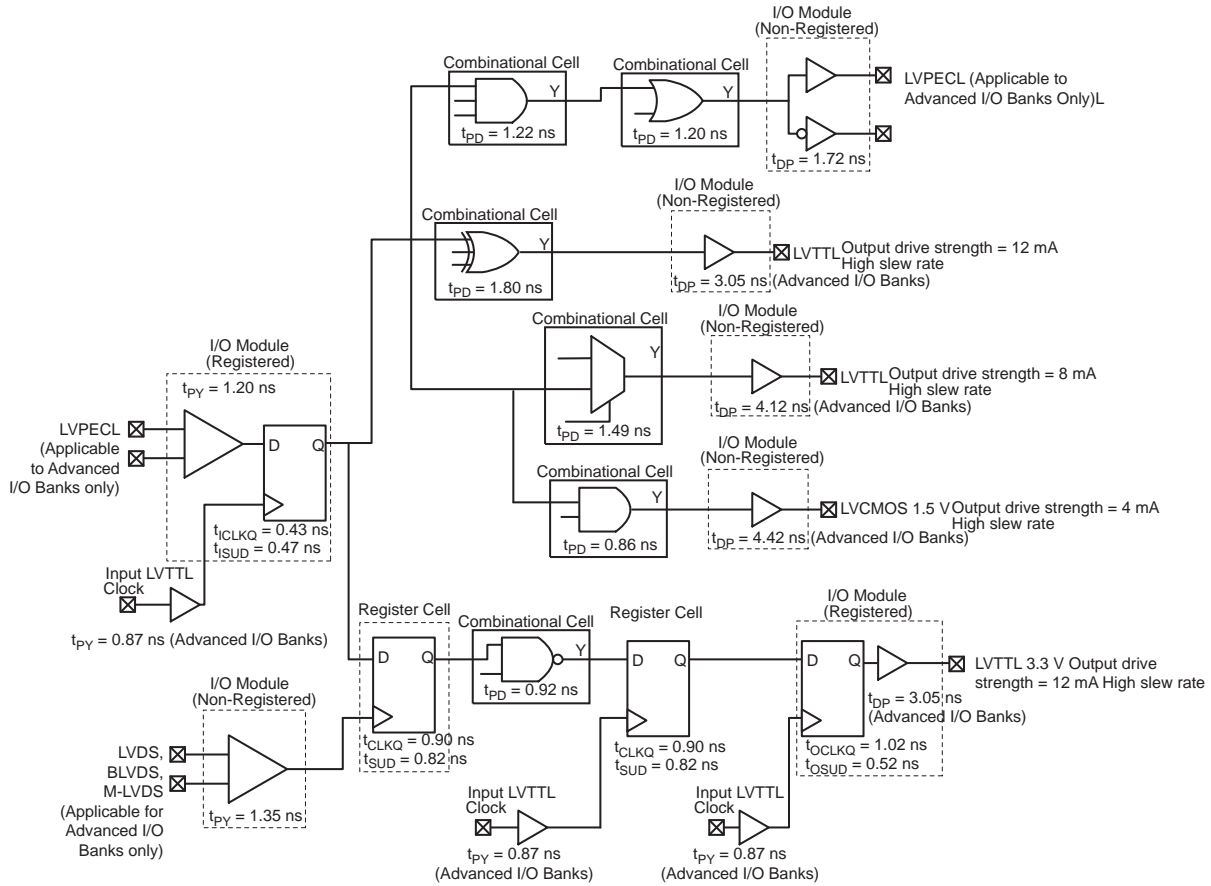
Component	Definition	Guideline
$\alpha_1$	Toggle rate of VersaTile outputs	10%
$\alpha_2$	I/O buffer toggle rate	10%

**Table 2-23 • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
$\beta_1$	I/O output buffer enable rate	100%
$\beta_2$	RAM enable rate for read operations	12.5%
$\beta_3$	RAM enable rate for write operations	12.5%

# User I/O Characteristics

## Timing Model



**Figure 2-3 • Timing Model**  
**Operating Conditions: Std. Speed, Commercial Temperature Range ( $T_J = 70^\circ\text{C}$ ), Worst-Case VCC = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices**

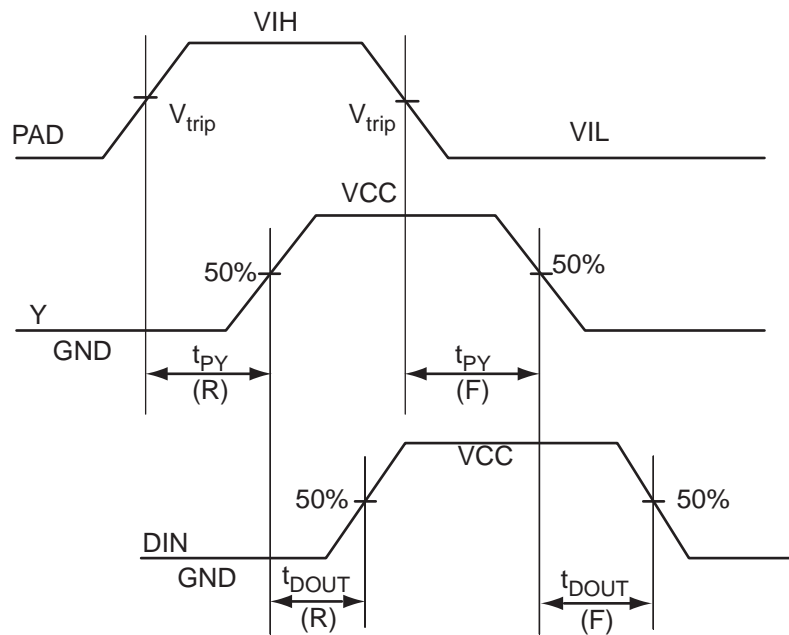
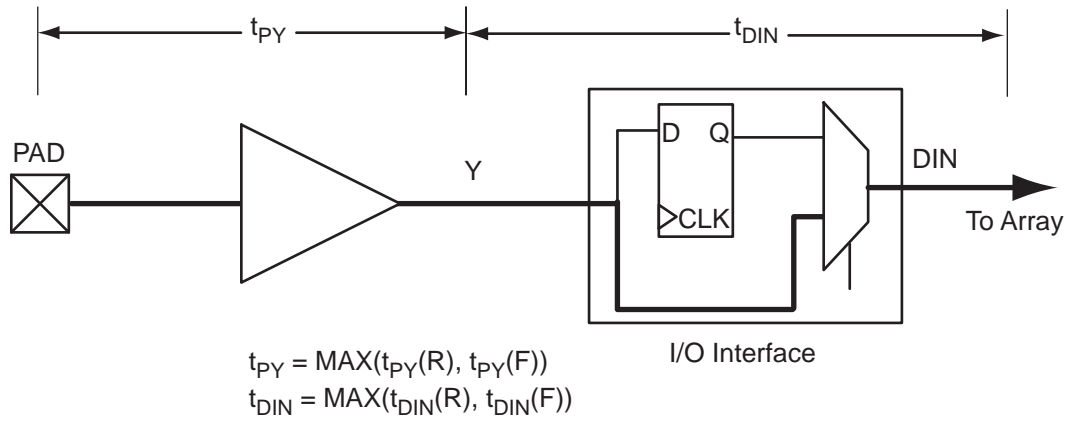


Figure 2-4 • Input Buffer Timing Model and Delays (example)

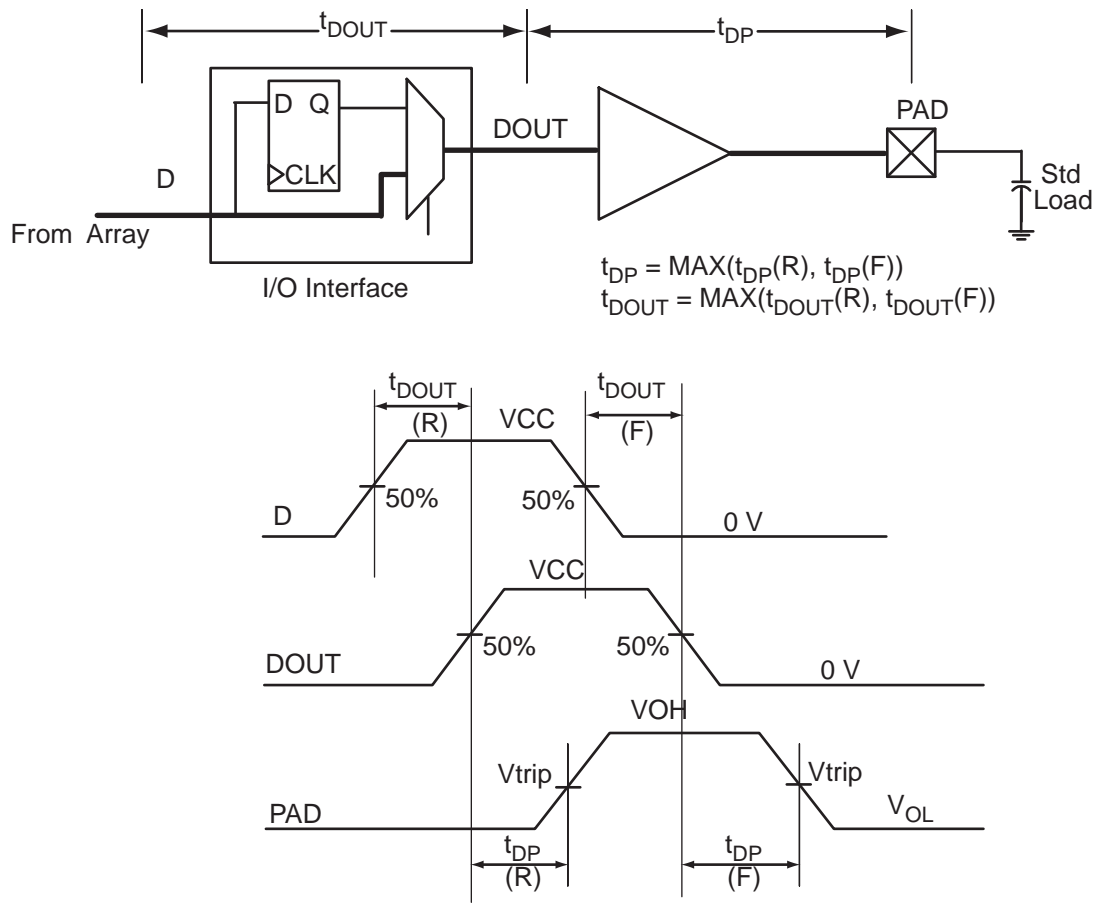


Figure 2-5 • Output Buffer Model and Delays (example)

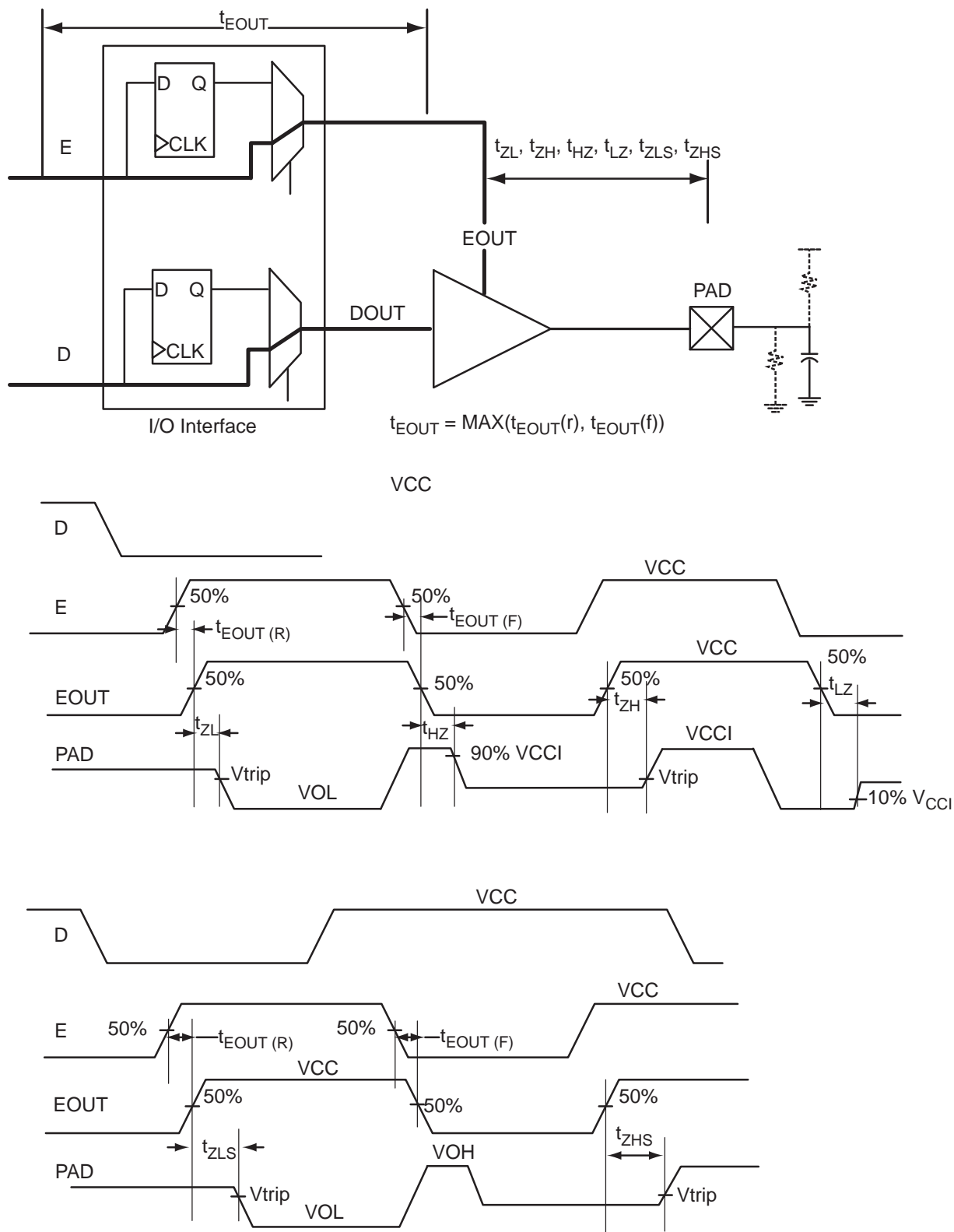


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-24 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**  
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>2</sup>	Slew Rate	VIL		VIH		V <sub>OL</sub>	VOH	I <sub>OL</sub> <sup>1</sup>	I <sub>OH</sub> <sup>1</sup>
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range <sup>3</sup>	100 $\mu$ A	12 mA	High	-0.3	0.8	2	3.6	0.2	VCCI - 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS <sup>4</sup>	2 mA	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range <sup>4,5</sup>	100 $\mu$ A	2 mA	High	-0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI - 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

**Notes:**

1. Currents are measured at 85°C junction temperature.
2. Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100  $\mu$ A drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to V2 Devices operating at VCCI  $\geq$  VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

**Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>2</sup>	Slew Rate	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range <sup>3</sup>	100 μA	12 mA	High	-0.3	0.8	2	3.6	0.2	VDD-0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS <sup>4</sup>	2 mA	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range <sup>4</sup>	100 μA	2 mA	High	-0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI - 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

**Notes:**

1. Currents are measured at 85°C junction temperature.
2. Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to V2 Devices operating at VCCI ≥ VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

**Table 2-26 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings  
Applicable to Standard I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>2</sup>	Slew Rate	VIL		VIH		VOL	VOH	IO <sup>L</sup> <sup>1</sup>	IO <sup>H</sup> <sup>1</sup>
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	-0.3	0.8	2	3.6	0.4	2.4	8	8
3.3 V LVCMOS Wide Range <sup>3</sup>	100 $\mu$ A	8 mA	High	-0.3	0.8	2	3.6	0.2	VDD-0.2	0.1	0.1
2.5 V LVCMOS	8 mA	8 mA	High	-0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4
1.5 V LVCMOS	2 mA	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS <sup>4</sup>	1 mA	1 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1
1.2 V LVCMOS Wide Range <sup>4,5</sup>	100 $\mu$ A	1 mA	High	-0.3	0.3 * VCCI	0.7 * VCCI	3.6	0.1	VCCI - 0.1	0.1	0.1

**Notes:**

1. Currents are measured at 85°C junction temperature.
2. Note that 1.2 V LVCMOS and 3.3 V LVCMOS wide range is applicable to 100  $\mu$ A drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to V2 Devices operating at VCCI  $\geq$  VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.



**Table 2-27 • Summary of Maximum and Minimum DC Input Levels  
Applicable to Commercial and Industrial Conditions**

DC I/O Standards	Commercial <sup>1</sup>		Industrial <sup>2</sup>	
	$I_{IL}$ <sup>4</sup>	$I_{IH}$ <sup>5</sup>	$I_{IL}$ <sup>4</sup>	$I_{IH}$ <sup>5</sup>
	$\mu\text{A}$	$\mu\text{A}$	$\mu\text{A}$	$\mu\text{A}$
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS <sup>3</sup>	10	10	15	15
1.2 V LVCMOS Wide Range <sup>3</sup>	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

**Notes:**

1. Commercial range ( $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ )
2. Industrial range ( $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ )
3. Applicable to V2 Devices operating at  $V_{CCI} \geq V_{CC}$ .
4.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
5.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges

## Summary of I/O Timing Characteristics – Default I/O Software Settings

**Table 2-28 • Summary of AC Measuring Points**

Standard	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
3.3 V VCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
1.2 V LVCMOS Wide Range	0.60 V
3.3 V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3 V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

**Table 2-29 • I/O AC Parameter Definitions**

Parameter	Parameter Definition
$t_{DP}$	Data to Pad delay through the Output Buffer
$t_{PY}$	Pad to Data delay through the Input Buffer
$t_{DOUT}$	Data to Output Buffer delay through the I/O interface
$t_{EOUT}$	Enable to Output Buffer Tristate Control delay through the I/O interface
$t_{DIN}$	Input Buffer to Data delay through the I/O interface
$t_{HZ}$	Enable to Pad delay through the Output Buffer—High to Z
$t_{ZH}$	Enable to Pad delay through the Output Buffer—Z to High
$t_{LZ}$	Enable to Pad delay through the Output Buffer—Low to Z
$t_{ZL}$	Enable to Pad delay through the Output Buffer—Z to Low
$t_{ZHS}$	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
$t_{ZLS}$	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

**Table 2-30 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard)**  
**Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup> (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{pOUT}$ (ns)	$t_{pP}$ (ns)	$t_{pDIN}$ (ns)	$t_{pY}$ (ns)	$t_{pOUT}$ (ns)	$t_{zL}$ (ns)	$t_{zH}$ (ns)	$t_{zL}$ (ns)	$t_{zH}$ (ns)	$t_{zLS}$ (ns)	$t_{zHS}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25 <sup>2</sup>	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 <sup>2</sup>	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

**Notes:**

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-79](#) for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard)**  
**Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup> (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{\text{pOUT}}$ (ns)	$t_{\text{pP}}$ (ns)	$t_{\text{pIN}}$ (ns)	$t_{\text{pY}}$ (ns)	$t_{\text{EOUT}}$ (ns)	$t_{\text{ZL}}$ (ns)	$t_{\text{ZH}}$ (ns)	$t_{\text{LZ}}$ (ns)	$t_{\text{HZ}}$ (ns)	$t_{\text{ZLS}}$ (ns)	$t_{\text{ZHS}}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	12	High	5	–	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	1.75	0.18	1.08	0.66	1.79	1.52	2.38	2.70	5.39	5.11	ns
1.8 V LVCMOS	8 mA	8	High	5	–	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
1.5 V LVCMOS	4 mA	4	High	5	–	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns
3.3 V PCI	Per PCI spec	–	High	10	25 <sup>2</sup>	0.97	1.97	0.18	0.73	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 <sup>2</sup>	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

**Notes:**

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-79](#) for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI}$  (per standard)**  
**Applicable to Standard I/O Banks**

I/O Standard	Drive Strength)	Equivalent Software Default Drive Strength Option <sup>1</sup> (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{\text{DOUT}}$ (ns)	$t_{\text{DP}}$ (ns)	$t_{\text{DIN}}$ (ns)	$t_{\text{PY}}$ (ns)	$t_{\text{EOUT}}$ (ns)	$t_{\text{ZL}}$ (ns)	$t_{\text{ZH}}$ (ns)	$t_{\text{LZ}}$ (ns)	$t_{\text{HZ}}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8	High	5	–	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	8	High	5	–	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	ns
2.5 V LVCMOS	8 mA	8	High	5	–	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns
1.8 V LVCMOS	4 mA	4	High	5	–	0.97	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	ns
1.5 V LVCMOS	2 mA	2	High	5	–	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

**Notes:**

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-33 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard)**  
**Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{pOUT}$ (ns)	$t_{pP}$ (ns)	$t_{pIN}$ (ns)	$t_{pY}$ (ns)	$t_{EOUT}$ (ns)	$t_{zL}$ (ns)	$t_{zH}$ (ns)	$t_{zLZ}$ (ns)	$t_{zHZ}$ (ns)	$t_{zLS}$ (ns)	$t_{zHS}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	–	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	12 mA	High	5	–	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
2.5 V LVCMOS	12 mA	12 mA	High	5	–	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
1.8 V LVCMOS	12 mA	12 mA	High	5	–	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
1.5 V LVCMOS	12 mA	12 mA	High	5	–	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
1.2 V LVCMOS	2 mA	2 mA	High	5	–	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns
1.2 V LVCMOS Wide Range <sup>3</sup>	100 $\mu\text{A}$	2 mA	High	5	–	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns
3.3 V PCI	Per PCI spec	–	High	10	25 <sup>2</sup>	1.55	2.91	0.26	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 <sup>2</sup>	1.55	2.91	0.25	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns
LVDS	24 mA	–	High	–	–	1.55	2.27	0.25	1.57	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	1.55	2.24	0.25	1.38	–	–	–	–	–	–	–	ns

**Notes:**

- Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
- All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
- Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-79](#) for connectivity. This resistor is not required during normal operation.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-34 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard)**  
**Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup> (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	t <sub>DOU</sub> (ns)	t <sub>DP</sub> (ns)	t <sub>DIN</sub> (ns)	t <sub>PY</sub> (ns)	t <sub>EOU</sub> (ns)	t <sub>ZL</sub> (ns)	t <sub>ZH</sub> (ns)	t <sub>LZ</sub> (ns)	t <sub>HZ</sub> (ns)	t <sub>ZLS</sub> (ns)	t <sub>ZHS</sub> (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	12	High	5	–	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
2.5 V LVCMOS	12 mA	12	High	5	–	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns
1.8 V LVCMOS	8 mA	8	High	5	–	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
1.5 V LVCMOS	4 mA	4	High	5	–	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns
1.2 V LVCMOS	2 mA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
1.2 V LVCMOS Wide Range <sup>3</sup>	100 $\mu\text{A}$	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
3.3 V PCI	Per PCI spec	–	High	10	25 <sup>2</sup>	1.55	2.53	0.26	0.84	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 <sup>2</sup>	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

**Notes:**

- Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
- All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.
- Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-12 on page 2-79](#) for connectivity. This resistor is not required during normal operation.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-35 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ , Worst-Case  $V_{CCI}$  (per standard)**  
**Applicable to Standard I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup> (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DIN}$ (ns)	$t_{PY}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8	High	5	–	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
3.3 V LVCMOS Wide Range <sup>3</sup>	100 $\mu\text{A}$	8	High	5	–	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
2.5 V LVCMOS	8 mA	8	High	5	–	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns
1.8 V LVCMOS	4 mA	4	High	5	–	1.55	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	ns
1.5 V LVCMOS	2 mA	2	High	5	–	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns
1.2 V LVCMOS	1 mA	1	High	5	–	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns
1.2 V LVCMOS Wide Range <sup>3</sup>	100 $\mu\text{A}$	1	High	5	–	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

**Notes:**

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification
4. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.



## Detailed I/O DC Characteristics

**Table 2-36 • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
$C_{IN}$	Input capacitance	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0 \text{ MHz}$		8	pF

**Table 2-37 • I/O Output Buffer Maximum Resistances<sup>1</sup>  
Applicable to Advanced I/O Banks**

Standard	Drive Strength	$R_{PULL-DOWN}$ ( $\Omega$ ) <sup>2</sup>	$R_{PULL-UP}$ ( $\Omega$ ) <sup>3</sup>
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS <sup>4</sup>	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range <sup>4</sup>	100 $\mu$ A	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on  $V_{CCI}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3.  $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$
4. Applicable to IGLOO V2 Devices operating at  $V_{CCI} \geq V_{CC}$

**Table 2-38 • I/O Output Buffer Maximum Resistances<sup>1</sup>**  
**Applicable to Standard Plus I/O Banks**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (Ω) <sup>2</sup>	R <sub>PULL-UP</sub> (Ω) <sup>3</sup>
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 μA	TBD	TBD
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS <sup>4</sup>	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range <sup>4</sup>	100 μA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3.  $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{OH_{spec}}$
4. Applicable to IGLOO V2 Devices operating at  $VCCI \geq VCC$

**Table 2-39 • I/O Output Buffer Maximum Resistances<sup>1</sup>**  
**Applicable to Standard I/O Banks**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (Ω) <sup>2</sup>	R <sub>PULL-UP</sub> (Ω) <sup>3</sup>
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 μA	TBD	TBD
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS	1 mA	TBD	TBD
1.2 V LVCMOS Wide Range <sup>4</sup>	100 μA	TBD	TBD

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3.  $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

**Table 2-40 • I/O Weak Pull-Up/Pull-Down Resistances**  
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

VCCI	R <sub>(WEAK PULL-UP)</sub> <sup>1</sup> (Ω)		R <sub>(WEAK PULL-DOWN)</sub> <sup>2</sup> (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 K	45 K	10 K	45 K
3.3 V Wide Range I/Os	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V Wide Range I/Os	19 K	110 K	19 K	150 K

**Notes:**

1.  $R_{(WEAK PULL-UP-MAX)} = (V_{OLspec}) / I_{(WEAK PULL-UP-MIN)}$
2.  $R_{(WEAK PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK PULL-UP-MIN)}$

**Table 2-41 • I/O Short Currents  $I_{OSH}/I_{OSL}$   
Applicable to Advanced I/O Banks**

	Drive Strength	$I_{OSL}$ (mA)*	$I_{OSH}$ (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

 \*  $T_J = 100^\circ\text{C}$

**Table 2-42 • I/O Short Currents  $I_{OSH}/I_{OSL}$   
Applicable to Standard Plus I/O Banks**

	Drive Strength	$I_{OSL}$ (mA)*	$I_{OSH}$ (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
3.3 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2 V LVCMOS	2 mA	TBD	TBD
1.2 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

\*  $T_J = 100^\circ\text{C}$

**Table 2-43 • I/O Short Currents  $I_{OSH}/I_{OSL}$   
Applicable to Standard I/O Banks**

	Drive Strength	$I_{OSL}$ (mA)*	$I_{OSH}$ (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
3.3 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16
1.2 V LVCMOS	1 mA	TBD	TBD
1.2 V LVCMOS Wide Range	100 $\mu$ A	TBD	TBD

\*  $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand  $I_{OSH}/I_{OSL}$  events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

**Table 2-44 • Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
-40°C	> 20 years
-20°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

**Table 2-45 • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

\* The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

## Single-Ended I/O Characteristics

### 3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

**Table 2-46 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IosL	IosH	IIL <sup>1</sup>	IIH <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-47 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IosL	IosH	IIL <sup>1</sup>	IIH <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

**Notes:**

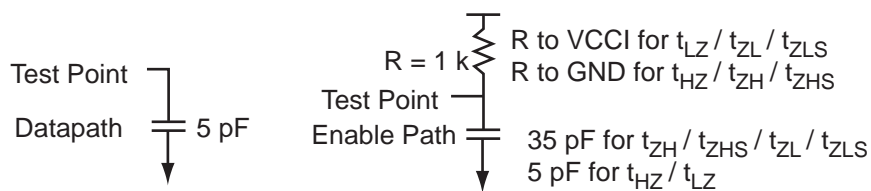
1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-48 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VO <sub>L</sub>	VO <sub>H</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.


**Figure 2-7 • AC Loading**
**Table 2-49 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	3.3	1.4	5

\* Measuring point =  $V_{trip}$ . See Table 2-28 on page 2-28 for a complete table of trip points.



## Timing Characteristics

Applies to 1.5 V DC Core Voltage

**Table 2-50 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
6 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
8 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
12 mA	Std.	0.97	3.23	0.18	0.85	0.66	3.30	2.98	2.66	2.91	6.89	6.57	ns
16 mA	Std.	0.97	3.08	0.18	0.85	0.66	3.14	2.89	2.70	2.99	6.74	6.48	ns
24 mA	Std.	0.97	3.00	0.18	0.85	0.66	3.06	2.91	2.74	3.27	6.66	6.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
6 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
8 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
12 mA	Std.	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
16 mA	Std.	0.97	2.05	0.18	0.85	0.66	2.10	1.64	2.70	3.12	5.69	5.24	ns
24 mA	Std.	0.97	2.07	0.18	0.85	0.66	2.12	1.60	2.75	3.41	5.71	5.20	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
6 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
8 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
12 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns
16 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-53 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
6 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
8 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
12 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
16 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-54 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
4 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
6 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns
8 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-55 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
4 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
6 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
8 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Applies to 1.2 V DC Core Voltage**

**Table 2-56 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**  
**Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
6 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
8 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
12 mA	Std.	1.55	3.85	0.26	0.98	1.10	3.91	3.53	3.24	3.77	9.69	9.32	ns
16 mA	Std.	1.55	3.69	0.26	0.98	1.10	3.75	3.44	3.28	3.84	9.54	9.23	ns
24 mA	Std.	1.55	3.61	0.26	0.98	1.10	3.67	3.46	3.33	4.13	9.45	9.24	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-57 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**  
**Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
6 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
8 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
12 mA	Std.	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
16 mA	Std.	1.55	2.63	0.26	0.98	1.10	2.67	2.14	3.28	4.01	8.45	7.93	ns
24 mA	Std.	1.55	2.65	0.26	0.98	1.10	2.69	2.10	3.33	4.31	8.47	7.89	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-58 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
6 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
8 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
12 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns
16 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-59 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
6 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
8 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
12 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
16 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-60 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
4 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
6 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns
8 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-61 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
4 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
6 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
8 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

### 3.3 V LVCMOS Wide Range

**Table 2-62 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range**  
Applicable to Advanced I/O Banks

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	IIH <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10
100 μA	8 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10
100 μA	12 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10
100 μA	16 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10
100 μA	24 mA	-0.3	0.8	2	3.6	0.2	$V_{DD} - 0.2$	100	100	TBD	TBD	10	10

**Notes:**

- Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
- $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 85°C junction temperature.
- Software default selection highlighted in gray.

**Table 2-63 • Minimum and Maximum DC Input and Output Levels for LVC MOS 3.3 V Wide Range  
Applicable to Standard Plus I/O Banks**

3.3 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IosL	IosH	IIL <sup>2</sup>	IiH <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	V <sub>DD</sub> - 0.2	100	100	TBD	TBD	10	10
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	V <sub>DD</sub> - 0.2	100	100	TBD	TBD	10	10
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	V <sub>DD</sub> - 0.2	100	100	TBD	TBD	10	10
100 μA	8 mA	-0.3	0.8	2	3.6	0.2	V <sub>DD</sub> - 0.2	100	100	TBD	TBD	10	10
100 μA	12 mA	-0.3	0.8	2	3.6	0.2	V <sub>DD</sub> - 0.2	100	100	TBD	TBD	10	10
100 μA	16 mA	-0.3	0.8	2	3.6	0.2	V <sub>DD</sub> - 0.2	100	100	TBD	TBD	10	10

**Notes:**

1. Note that 3.3 V LVC MOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V<sub>IN</sub> < V<sub>IL</sub>.
3. I<sub>iH</sub> is the input leakage current per I/O pin over recommended operating conditions V<sub>IH</sub> < V<sub>IN</sub> < V<sub>CCI</sub>. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

**Table 2-64 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range  
Applicable to Standard I/O Banks**

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	I <sub>IH</sub> <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	μA	μA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	TBD	TBD	10	10
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	TBD	TBD	10	10
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	TBD	TBD	10	10
100 μA	8 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	TBD	TBD	10	10

**Notes:**

1. Note that 3.3 V LVCMOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only
2.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
3.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

**Table 2-65 • 3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	3.3	1.4	5

\* Measuring point =  $V_{trip}$ . See Table 2-28 on page 2-28 for a complete table of trip points.

### Timing Characteristics

Applies to 1.5 V DC Core Voltage

**Table 2-66 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V  
 Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
100 $\mu\text{A}$	4 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 $\mu\text{A}$	6 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 $\mu\text{A}$	8 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 $\mu\text{A}$	12 mA	Std.	0.97	4.69	0.18	1.19	0.66	4.71	4.25	3.80	4.10	8.31	7.85	ns
100 $\mu\text{A}$	16 mA	Std.	0.97	4.46	0.18	1.19	0.66	4.48	4.11	3.86	4.21	8.07	7.71	ns
100 $\mu\text{A}$	24 mA	Std.	0.97	4.34	0.18	1.19	0.66	4.36	4.14	3.93	4.64	7.95	7.74	ns

**Notes:**

- Note that 3.3 V LVC MOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-67 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V  
 Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
100 $\mu\text{A}$	4 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 $\mu\text{A}$	6 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 $\mu\text{A}$	8 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 $\mu\text{A}$	12 mA	Std.	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
100 $\mu\text{A}$	16 mA	Std.	0.97	2.87	0.18	1.19	0.66	2.89	2.22	3.86	4.41	6.49	5.82	ns
100 $\mu\text{A}$	24 mA	Std.	0.97	2.90	0.18	1.19	0.66	2.92	2.16	3.94	4.86	6.51	5.75	ns

**Notes:**

- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
- Software default selection highlighted in gray.
- Note that 3.3 V LVC MOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.



**Table 2-68 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	4 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 $\mu\text{A}$	6 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 $\mu\text{A}$	8 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 $\mu\text{A}$	12 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns
100 $\mu\text{A}$	16 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns

**Notes:**

- Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-69 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	4 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 $\mu\text{A}$	6 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 $\mu\text{A}$	8 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 $\mu\text{A}$	12 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
100 $\mu\text{A}$	16 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns

**Notes:**

- Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
- Software default selection highlighted in gray.

**Table 2-70 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V  
 Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	2 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 $\mu\text{A}$	4 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 $\mu\text{A}$	6 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns
100 $\mu\text{A}$	8 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns

*Notes:*

1. Note that 3.3 V LVC MOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-71 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V  
 Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	2 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 $\mu\text{A}$	4 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 $\mu\text{A}$	6 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns
100 $\mu\text{A}$	8 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns

*Notes:*

1. Note that 3.3 V LVC MOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
3. Software default selection highlighted in gray.

*Applies to 1.2 V DC Core Voltage*

**Table 2-72 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ , Worst-Case  $V_{CCI} = 2.7\text{ V}$   
 Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	4 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 $\mu\text{A}$	12 mA	Std.	1.55	5.55	0.26	1.32	1.10	5.55	4.96	4.50	5.18	11.34	10.75	ns
100 $\mu\text{A}$	16 mA	Std.	1.55	5.32	0.26	1.32	1.10	5.32	4.82	4.56	5.29	11.10	10.61	ns
100 $\mu\text{A}$	24 mA	Std.	1.55	5.19	0.26	1.32	1.10	5.19	4.85	4.63	5.74	10.98	10.63	ns

Notes:

- Note that 3.3 V LVC MOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) on [page 2-7](#) for derating values.

**Table 2-73 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ , Worst-Case  $V_{CCI} = 2.7$   
 Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	4 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 $\mu\text{A}$	12 mA	Std.	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
100 $\mu\text{A}$	16 mA	Std.	1.55	3.67	0.26	1.32	1.10	3.67	2.85	4.57	5.55	9.46	8.64	ns
100 $\mu\text{A}$	24 mA	Std.	1.55	3.70	0.26	1.32	1.10	3.70	2.79	4.65	6.01	9.49	8.58	ns

Notes:

- Note that 3.3 V LVC MOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6](#) on [page 2-7](#) for derating values.
- Software default selection highlighted in gray.

**Table 2-74 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7  
 Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
100 $\mu\text{A}$	4 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 $\mu\text{A}$	12 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns
100 $\mu\text{A}$	16 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns

*Notes:*

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-75 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7  
 Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
100 $\mu\text{A}$	4 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 $\mu\text{A}$	12 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
100 $\mu\text{A}$	16 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns

*Notes:*

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
3. Software default selection highlighted in gray.

**Table 2-76 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7**  
**Applicable to Standard Banks**

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	2 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 $\mu\text{A}$	4 mA	Std.	1.55	6.44	0.26	1.29	1.10	6.44	5.64	2.99	3.28	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	5.41	0.26	1.29	1.10	5.41	4.91	3.35	3.89	ns

*Notes:*

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-77 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7**  
**Applicable to Standard Banks**

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	2 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 $\mu\text{A}$	4 mA	Std.	1.55	3.89	0.26	1.29	1.10	3.89	3.13	2.99	3.45	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	3.33	0.26	1.29	1.10	3.33	2.62	3.34	4.07	ns

*Notes:*

1. Note that 3.3 V LVCMOS wide range is applicable to 100  $\mu\text{A}$  drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
3. Software default selection highlighted in gray.

## 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V-tolerant input buffer and push-pull output buffer.

**Table 2-78 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

**Notes:**

1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-79 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

**Notes:**

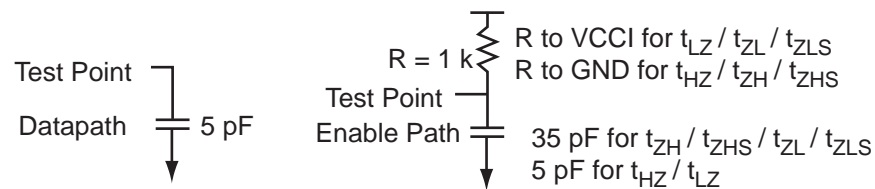
1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-80 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.


**Figure 2-8 • AC Loading**
**Table 2-81 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	2.5	1.2	5

\* Measuring point =  $V_{trip}$ . See Table 2-28 on page 2-28 for a complete table of trip points.

### Timing Characteristics

Applies to 1.5 V DC Core Voltage

**Table 2-82 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-83 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-84 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.



**Table 2-85 • 2.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.97	2.36	0.18	1.08	0.66	2.41	2.21	1.96	1.92	6.01	5.81	ns
6 mA	Std.	0.97	1.97	0.18	1.08	0.66	2.01	1.75	2.21	2.40	5.61	5.34	ns
8 mA	Std.	0.97	1.97	0.18	1.08	0.66	2.01	1.75	2.21	2.40	5.61	5.34	ns
12 mA	Std.	0.97	1.75	0.18	1.08	0.66	1.79	1.52	2.38	2.70	5.39	5.11	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-86 • 2.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	4.27	0.18	1.04	0.66	4.36	4.06	1.71	1.62	ns
4 mA	Std.	0.97	4.27	0.18	1.04	0.66	4.36	4.06	1.71	1.62	ns
6 mA	Std.	0.97	3.54	0.18	1.04	0.66	3.61	3.48	1.95	2.08	ns
8 mA	Std.	0.97	3.54	0.18	1.04	0.66	3.61	3.48	1.95	2.08	ns

**Note:** For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-87 • 2.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	2.24	0.18	1.04	0.66	2.29	2.09	1.71	1.68	ns
4 mA	Std.	0.97	2.24	0.18	1.04	0.66	2.29	2.09	1.71	1.68	ns
6 mA	Std.	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns
8 mA	Std.	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Applies to 1.2 V Core Voltage**

**Table 2-88 • 2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-89 • 2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-90 • 2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-91 • 2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
6 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
8 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
12 mA	Std.	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-92 • 2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
4 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
6 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns
8 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns

**Note:** For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-93 • 2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
4 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
6 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns
8 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

### 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

**Table 2-94 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	9	11	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	17	22	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	35	44	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	45	51	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12	91	74	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	16	16	91	74	10	10

**Notes:**

1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V<sub>IN</sub> < V<sub>IL</sub>.
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions V<sub>IH</sub> < V<sub>IN</sub> < V<sub>CCI</sub>. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-95 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	9	11	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	17	22	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	35	44	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	35	44	10	10

**Notes:**

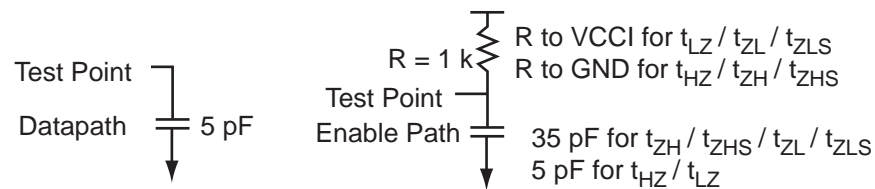
1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V<sub>IN</sub> < V<sub>IL</sub>.
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions V<sub>IH</sub> < V<sub>IN</sub> < V<sub>CCI</sub>. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-96 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	mA <sup>3</sup>	mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	2	2	9	11	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4	17	22	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.


**Figure 2-9 • AC Loading**
**Table 2-97 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.8	0.9	5

\* Measuring point =  $V_{trip}$ . See Table 2-28 on page 2-28 for a complete table of trip points.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-98 • 1.8 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-99 • 1.8 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.97	3.25	0.18	1.01	0.66	3.21	3.25	2.33	1.61	6.80	6.85	ns
4 mA	Std.	0.97	2.62	0.18	1.01	0.66	2.68	2.51	2.66	2.46	6.27	6.11	ns
6 mA	Std.	0.97	2.31	0.18	1.01	0.66	2.36	2.15	2.90	2.87	5.95	5.75	ns
8 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.08	2.95	2.98	5.89	5.68	ns
12 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
16 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-100 • 1.8 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.97	5.78	0.18	1.01	0.66	5.90	5.32	1.95	1.47	9.49	8.91	ns
4 mA	Std.	0.97	4.75	0.18	1.01	0.66	4.85	4.54	2.25	2.21	8.44	8.13	ns
6 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns
8 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-101 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	2.76	0.18	1.01	0.66	2.79	2.76	1.94	1.51	6.39	6.35	ns
4 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.09	2.24	2.29	5.89	5.69	ns
6 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
8 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-102 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	5.63	0.18	0.98	0.66	5.74	5.30	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.18	0.98	0.66	4.79	4.52	1.97	1.98	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-103 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	2.62	0.18	0.98	0.66	2.67	2.59	1.67	1.29	2.62	ns
4 mA	Std.	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	2.18	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**1.2 V DC Core Voltage**
**Table 2-104 • 1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	6.97	0.26	1.11	1.10	7.08	6.48	2.87	2.29	12.87	12.27	ns
4 mA	Std.	1.55	5.91	0.26	1.11	1.10	6.01	5.57	3.21	3.14	11.79	11.36	ns
6 mA	Std.	1.55	5.16	0.26	1.11	1.10	5.24	4.95	3.45	3.55	11.03	10.74	ns
8 mA	Std.	1.55	4.90	0.26	1.11	1.10	4.98	4.81	3.50	3.66	10.77	10.60	ns
12 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns
16 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-105 • 1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	3.73	0.26	1.11	1.10	3.71	3.73	2.86	2.34	9.49	9.51	ns
4 mA	Std.	1.55	3.12	0.26	1.11	1.10	3.16	2.97	3.21	3.22	8.95	8.75	ns
6 mA	Std.	1.55	2.79	0.26	1.11	1.10	2.83	2.59	3.45	3.65	8.62	8.38	ns
8 mA	Std.	1.55	2.73	0.26	1.11	1.10	2.77	2.52	3.50	3.75	8.56	8.30	ns
12 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
16 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-106 • 1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	6.32	0.26	1.11	1.10	6.43	5.81	2.47	2.16	12.22	11.60	ns
4 mA	Std.	1.55	5.27	0.26	1.11	1.10	5.35	5.01	2.78	2.92	11.14	10.79	ns
6 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns
8 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.



**Table 2-107 • 1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	1.55	3.22	0.26	1.11	1.10	3.26	3.18	2.47	2.20	9.05	8.97	ns
4 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.75	2.50	2.78	3.01	8.54	8.29	ns
6 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
8 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-108 • 1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.08	1.78	ns
4 mA	Std.	1.55	5.17	0.26	1.08	1.10	5.26	4.98	2.38	2.54	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-109 • 1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	3.06	0.26	1.08	1.10	3.10	3.01	2.08	1.83	3.06	ns
4 mA	Std.	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	2.60	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-110 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-111 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

**Notes:**

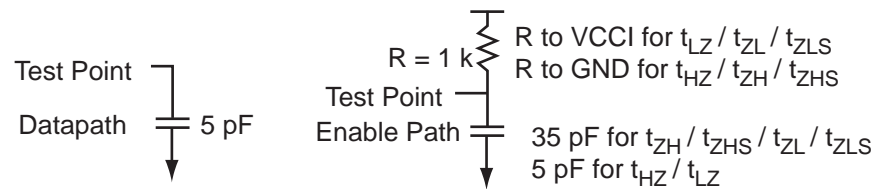
1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-112 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard I/O Banks

1.5 V LVCMOS Drive Strength	VIL		VIH		VOL	VOH	I <sub>oL</sub>	I <sub>oH</sub>	I <sub>oSH</sub>	I <sub>oSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

**Notes:**

1.  $I_{IL}$  is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2.  $I_{IH}$  is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.


**Figure 2-10 • AC Loading**
**Table 2-113 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.5	0.75	5

\* Measuring point =  $V_{trip}$ . See [Table 2-28](#) on page 2-28 for a complete table of trip points.

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-114 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-115 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-116 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-117 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-118 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	5.88	0.18	1.14	0.66	6.00	5.45	2.00	1.94	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-119 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
2 mA	Std.	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

## 1.2 V DC Core Voltage

**Table 2-120 • 1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	7.17	0.26	1.27	1.10	7.29	6.60	3.33	3.03	13.07	12.39	ns
4 mA	Std.	1.55	6.27	0.26	1.27	1.10	6.37	5.86	3.61	3.51	12.16	11.64	ns
6 mA	Std.	1.55	5.94	0.26	1.27	1.10	6.04	5.70	3.67	3.64	11.82	11.48	ns
8 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns
12 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-121 • 1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	3.44	0.26	1.27	1.10	3.49	3.35	3.32	3.12	9.28	9.14	ns
4 mA	Std.	1.55	3.06	0.26	1.27	1.10	3.10	2.89	3.60	3.61	8.89	8.67	ns
6 mA	Std.	1.55	2.98	0.26	1.27	1.10	3.02	2.80	3.66	3.74	8.81	8.58	ns
8 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
12 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-122 • 1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	6.43	0.26	1.27	1.10	6.54	5.95	2.82	2.83	12.32	11.74	ns
4 mA	Std.	1.55	5.59	0.26	1.27	1.10	5.68	5.27	3.07	3.27	11.47	11.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-123 • 1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	3.02	0.26	1.27	1.10	3.07	2.81	2.82	2.92	8.85	8.59	ns
4 mA	Std.	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-124 • 1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{\text{DOUT}}$	$t_{\text{DP}}$	$t_{\text{DIN}}$	$t_{\text{PY}}$	$t_{\text{EOUT}}$	$t_{\text{ZL}}$	$t_{\text{ZH}}$	$t_{\text{LZ}}$	$t_{\text{HZ}}$	Units
2 mA	Std.	1.55	6.35	0.26	1.22	1.10	6.46	5.93	2.40	2.46	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

**Table 2-125 • 1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**  
**Applicable to Standard Banks**

Drive Strength	Speed Grade	$t_{\text{DOUT}}$	$t_{\text{DP}}$	$t_{\text{DIN}}$	$t_{\text{PY}}$	$t_{\text{EOUT}}$	$t_{\text{ZL}}$	$t_{\text{ZH}}$	$t_{\text{LZ}}$	$t_{\text{HZ}}$	Units
2 mA	Std.	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

### 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2V wide range as specified in the JESD8-12A specification.

**Table 2-126 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

1.2 V LVCMOS	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.26	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	2	2	TBD	TBD	10	10

**Notes:**

1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-127 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

1.2 V LVCMOS	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.26	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	2	2	TBD	TBD	10	10

**Notes:**

1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

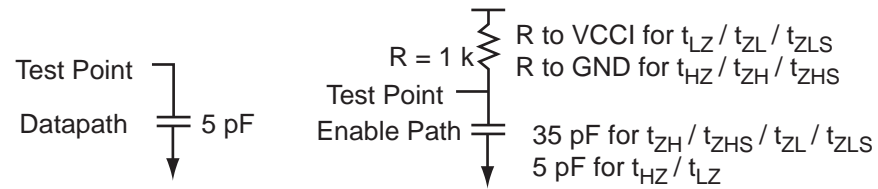
**Table 2-128 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard I/O Banks

1.2 V LVCMOS	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub>	I <sub>OSL</sub>	I <sub>IL</sub> <sup>1</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	3.6	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	1	1	TBD	TBD	10	10

**Notes:**

1. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.




**Figure 2-11 • AC Loading**
**Table 2-129 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	$C_{LOAD}$ (pF)
0	1.2	0.6	5

\* Measuring point =  $V_{trip}$ . See [Table 2-28](#) on [page 2-28](#) for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-130 • 1.2 V LVC MOS Low Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	8.37	0.26	1.60	1.10	8.04	7.17	3.94	3.52	13.82	12.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-131 • 1.2 V LVC MOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V  
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-132 • 1.2 V LVC MOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V  
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	7.59	0.26	1.59	1.10	7.29	6.54	3.30	3.35	13.08	12.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-133 • 1.2 V LVC MOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V  
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-134 • 1.2 V LVC MOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V  
Applicable to Standard Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
1 mA	Std.	1.55	8.57	0.26	1.53	1.10	8.23	7.38	2.51	2.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-135 • 1.2 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V  
Applicable to Standard Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	Units
1 mA	Std.	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## 1.2 V LCMOS Wide Range

**Table 2-136 • Minimum and Maximum DC Input and Output Levels for LVC MOS 1.2 V Wide Range**  
Applicable to Advanced I/O Banks

1.2 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	I <sub>IH</sub> <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 μA	2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	TBD	TBD	10	10

**Notes:**

- Note that 1.2 V LVC MOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
- I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 85°C junction temperature.
- Software default selection highlighted in gray.

**Table 2-137 • Minimum and Maximum DC Input and Output Levels for LVC MOS 1.2 V Wide Range**  
Applicable to Standard Plus I/O Banks

1.2 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	I <sub>IH</sub> <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 μA	2mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	TBD	TBD	10	10

**Notes:**

- Note that 1.2 V LVC MOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
- I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
- I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 85°C junction temperature.
- Software default selection highlighted in gray.

**Table 2-138 • Minimum and Maximum DC Input and Output Levels for LVC MOS 1.2 V Wide Range  
Applicable to Standard I/O Banks**

1.2 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub> <sup>2</sup>	I <sub>IH</sub> <sup>3</sup>
Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>4</sup>	Max. mA <sup>4</sup>	μA <sup>5</sup>	μA <sup>5</sup>
100 μA	1 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	TBD	TBD	10	10

**Notes:**

1. Note that 1.2 V LVC MOS wide range is applicable to 100 μA drive strength only. The configuration will not operate at the equivalent software default drive strength. These values are for normal ranges only.
2. I<sub>IL</sub> is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < V<sub>IN</sub> < VIL.
3. I<sub>IH</sub> is the input leakage current per I/O pin over recommended operating conditions V<sub>IH</sub> < V<sub>IN</sub> < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

**Table 2-139 • 1.2 V LVC MOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.2	0.6	5

\* Measuring point = V<sub>trip</sub>. See Table 2-28 on page 2-28 for a complete table of trip points.

**Timing Characteristics**

Refer to LVC MOS 1.2 V (normal range) "Timing Characteristics" on page 2-76 for worst-case timing.

### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

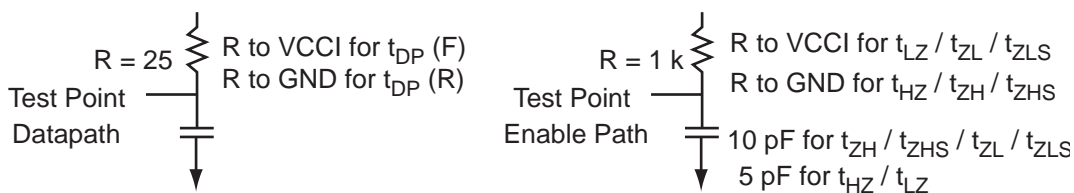
**Table 2-140 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced and Standard Plus I/Os

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IO <sub>L</sub>	IO <sub>H</sub>	IOSH	IOSL	IIL	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
Per PCI specification	Per PCI curves										10	10

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in [Figure 2-12](#).



**Figure 2-12 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in [Table 2-141](#).

**Table 2-141 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	3.3	0.285 * VCCI for t <sub>DP(R)</sub> 0.615 * VCCI for t <sub>DP(F)</sub>	10

\* Measuring point = Vtrip. See [Table 2-28 on page 2-28](#) for a complete table of trip points.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-142 • 3.3 V PCI/PCI-X**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
Applicable to Advanced I/O Banks

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
Std.	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-143 • 3.3 V PCI/PCI-X**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
Applicable to Standard Plus I/O Banks

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
Std.	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

#### 1.2 V DC Core Voltage

**Table 2-144 • 3.3 V PCI/PCI-X**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
Applicable to Advanced I/O Banks

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
Std.	1.55	2.91	0.25	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-145 • 3.3 V PCI/PCI-X**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
Applicable to Standard Plus I/O Banks

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
Std.	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## Differential I/O Characteristics

### Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

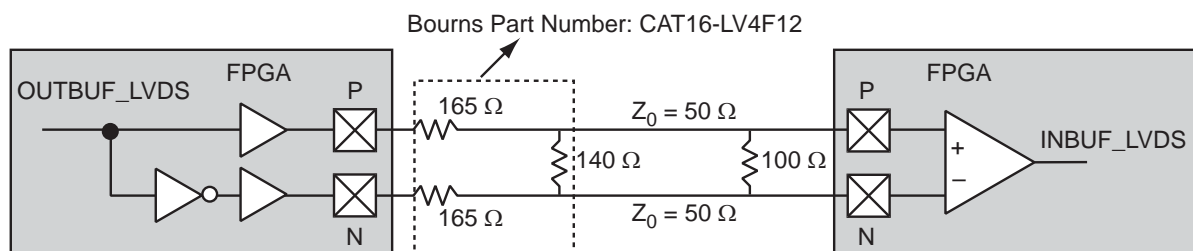
Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

### LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-13](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOO also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).



**Figure 2-13 • LVDS Circuit Diagram and Board-Level Implementation**

**Table 2-146 • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
I <sub>OL</sub> <sup>4</sup>	Output Lower Current	0.65	0.91	1.16	mA
I <sub>OH</sub> <sup>4</sup>	Output High Current	0.65	0.91	1.16	mA
V <sub>I</sub>	Input Voltage	0		2.925	V
I <sub>IH</sub> <sup>3</sup>	Input High Leakage Current			10	μA
I <sub>IL</sub> <sup>3</sup>	Input Low Leakage Current			10	μA
V <sub>ODIFF</sub>	Differential Output Voltage	250	350	450	mV
V <sub>OCM</sub>	Output Common-Mode Voltage	1.125	1.25	1.375	V
V <sub>ICM</sub>	Input Common-Mode Voltage	0.05	1.25	2.35	V
V <sub>IDIFF</sub>	Input Differential Voltage	100	350		mV

**Notes:**

1. ± 5%
2. Differential input voltage = ±350 mV.
3. Currents are measured at 85°C junction temperature.
4. I<sub>OL</sub>/I<sub>OH</sub> is defined by V<sub>ODIFF</sub>/(resistor network).

**Table 2-147 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

\* Measuring point = V<sub>trip</sub>. See Table 2-28 on page 2-28 for a complete table of trip points.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-148 • LVDS – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
Applicable to Standard Banks

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	Units
Std.	0.97	1.67	0.19	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

#### 1.2 V DC Core Voltage

**Table 2-149 • LVDS – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V  
Applicable to Standard Banks

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	Units
Std.	1.55	2.19	0.25	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.



## B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF\_LVDS and BIBUF\_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-14. The input and output buffer delays are available in the LVDS section in Table 2-148 on page 2-82 and Table 2-149 on page 2-82.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver:  $R_S = 60 \Omega$  and  $R_T = 70 \Omega$ , given  $Z_0 = 50 \Omega$  (2") and  $Z_{stubs} = 50 \Omega$  (~1.5").

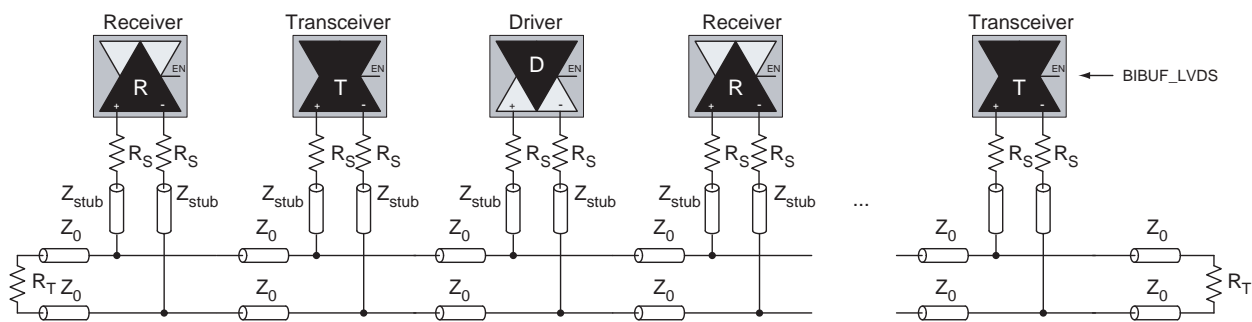


Figure 2-14 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-15. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

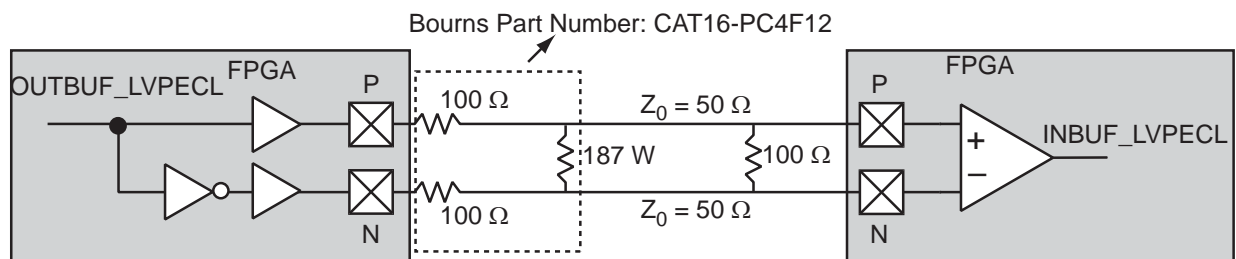


Figure 2-15 • LVPECL Circuit Diagram and Board-Level Implementation

**Table 2-150 • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.3	0	3.6	0	3.9	V
V <sub>ODIFF</sub>	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V <sub>OCM</sub>	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V <sub>ICM</sub>	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V <sub>IDIFF</sub>	Input Differential Voltage	300		300		300		mV

**Table 2-151 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

\* Measuring point =  $V_{trip}$ . See [Table 2-28 on page 2-104](#) for a complete table of trip points.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-152 • LVPECL – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
Applicable to Standard Banks

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	Units
Std.	0.97	1.67	0.19	1.16	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

#### 1.2 V DC Core Voltage

**Table 2-153 • LVPECL – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
Applicable to Standard Banks

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	Units
Std.	1.55	2.24	0.25	1.37	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

## I/O Register Specifications

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

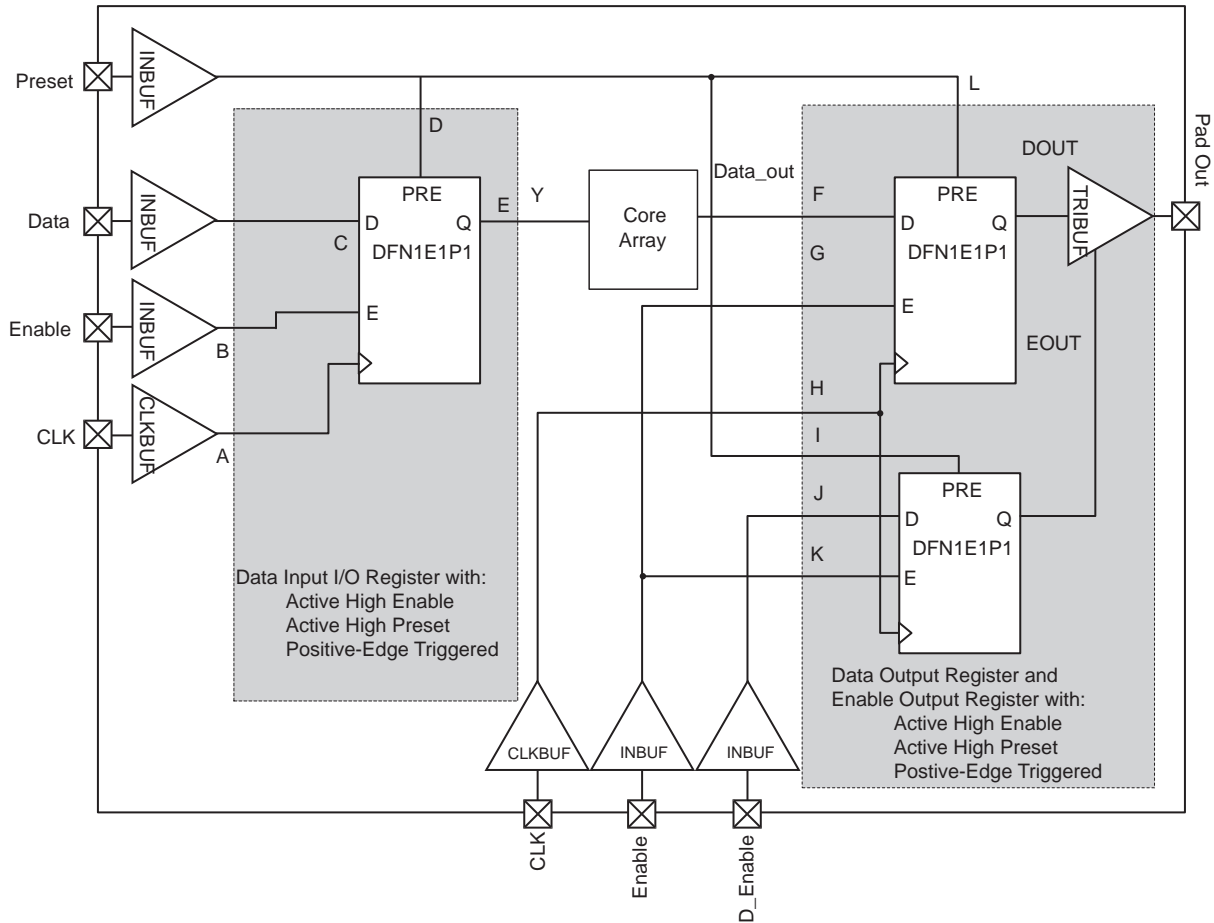


Figure 2-16 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

**Table 2-154 • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	H, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	F, H
$t_{OHD}$	Data Hold Time for the Output Data Register	F, H
$t_{OSUE}$	Enable Setup Time for the Output Data Register	G, H
$t_{OHE}$	Enable Hold Time for the Output Data Register	G, H
$t_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	H, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	J, H
$t_{OEHD}$	Data Hold Time for the Output Enable Register	J, H
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	K, H
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
$t_{ICLKQ}$	Clock-to-Q of the Input Data Register	A, E
$t_{ISUD}$	Data Setup Time for the Input Data Register	C, A
$t_{IHD}$	Data Hold Time for the Input Data Register	C, A
$t_{ISUE}$	Enable Setup Time for the Input Data Register	B, A
$t_{IHE}$	Enable Hold Time for the Input Data Register	B, A
$t_{IPRE2Q}$	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: \*See Figure 2-16 on page 2-85 for more information.

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

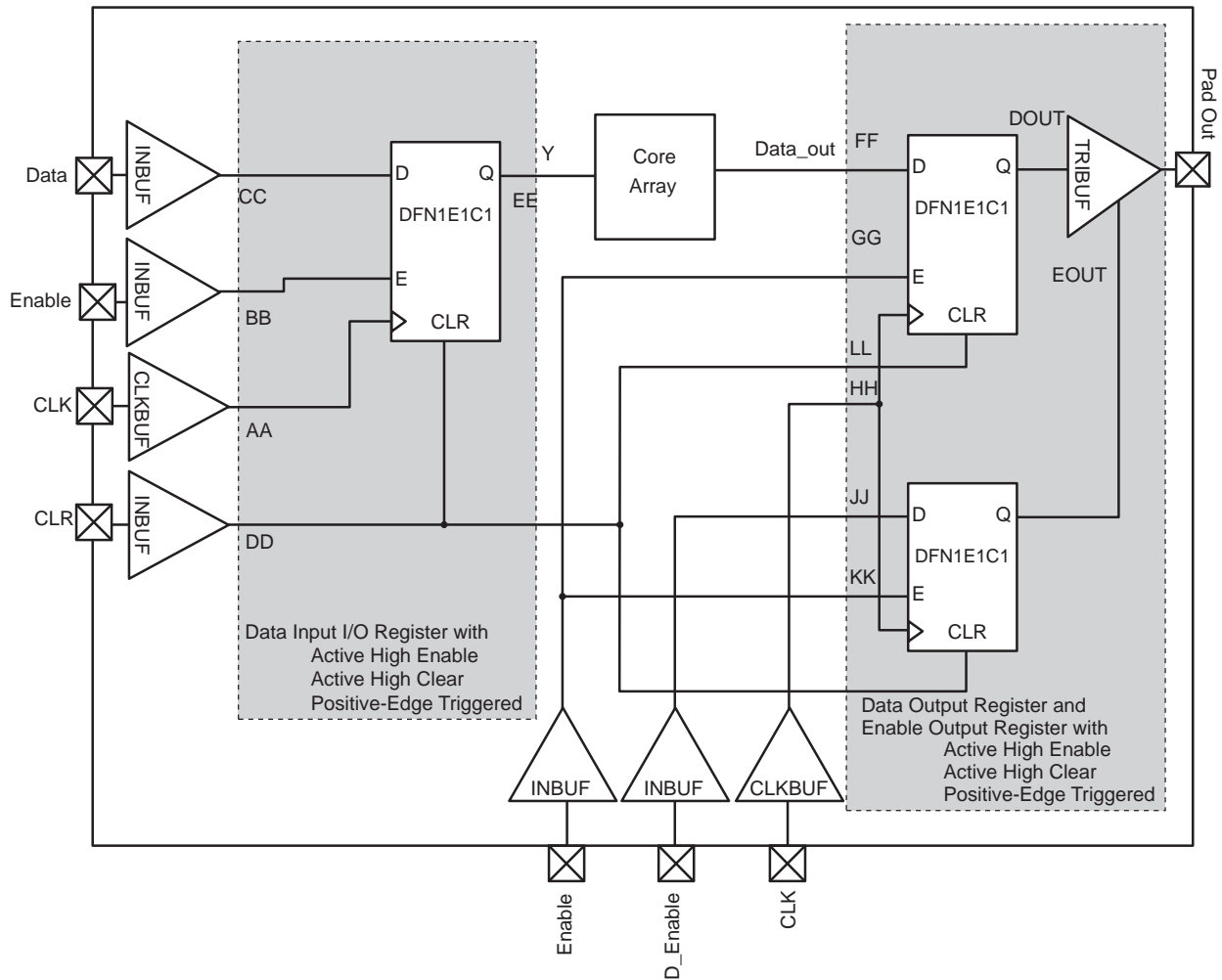


Figure 2-17 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

**Table 2-155 • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	HH, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	FF, HH
$t_{OHD}$	Data Hold Time for the Output Data Register	FF, HH
$t_{OSUE}$	Enable Setup Time for the Output Data Register	GG, HH
$t_{OHE}$	Enable Hold Time for the Output Data Register	GG, HH
$t_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	HH, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	JJ, HH
$t_{OEHD}$	Data Hold Time for the Output Enable Register	JJ, HH
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	KK, HH
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
$t_{ICLKQ}$	Clock-to-Q of the Input Data Register	AA, EE
$t_{ISUD}$	Data Setup Time for the Input Data Register	CC, AA
$t_{IHD}$	Data Hold Time for the Input Data Register	CC, AA
$t_{ISUE}$	Enable Setup Time for the Input Data Register	BB, AA
$t_{IHE}$	Enable Hold Time for the Input Data Register	BB, AA
$t_{ICLR2Q}$	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: \*See Figure 2-17 on page 2-87 for more information.

## Input Register

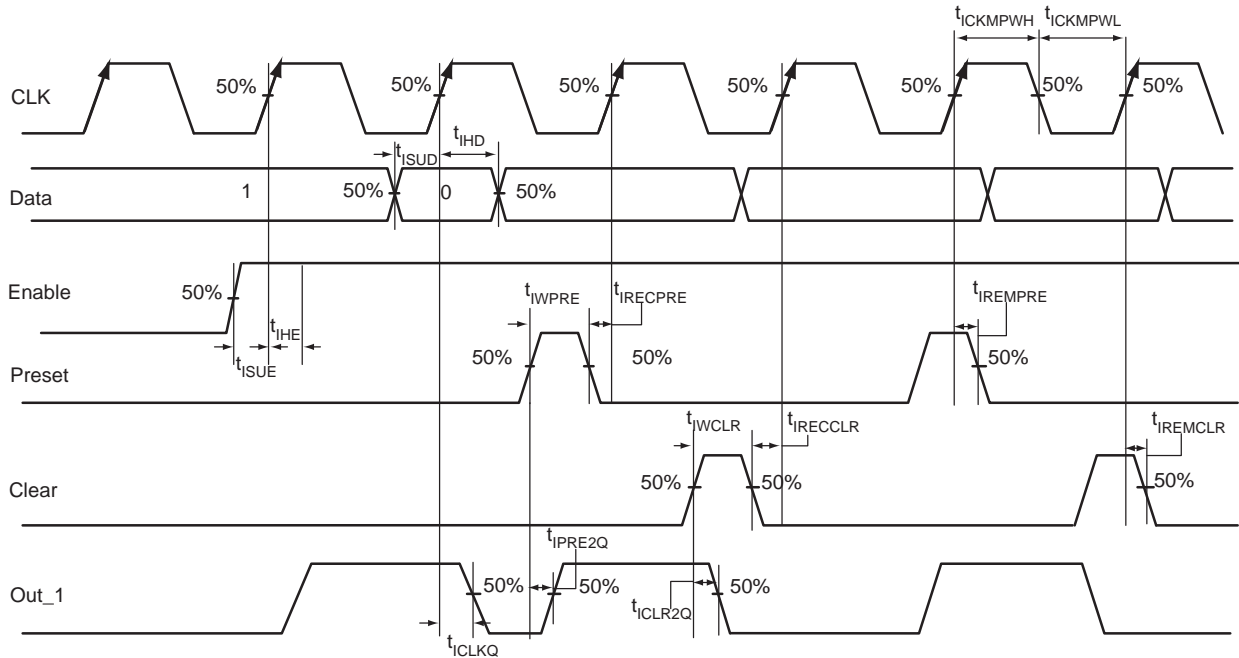


Figure 2-18 • Input Register Timing Diagram

### Timing Characteristics

#### 1.5 V DC Core Voltage

Table 2-156 • Input Data Register Propagation Delays

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

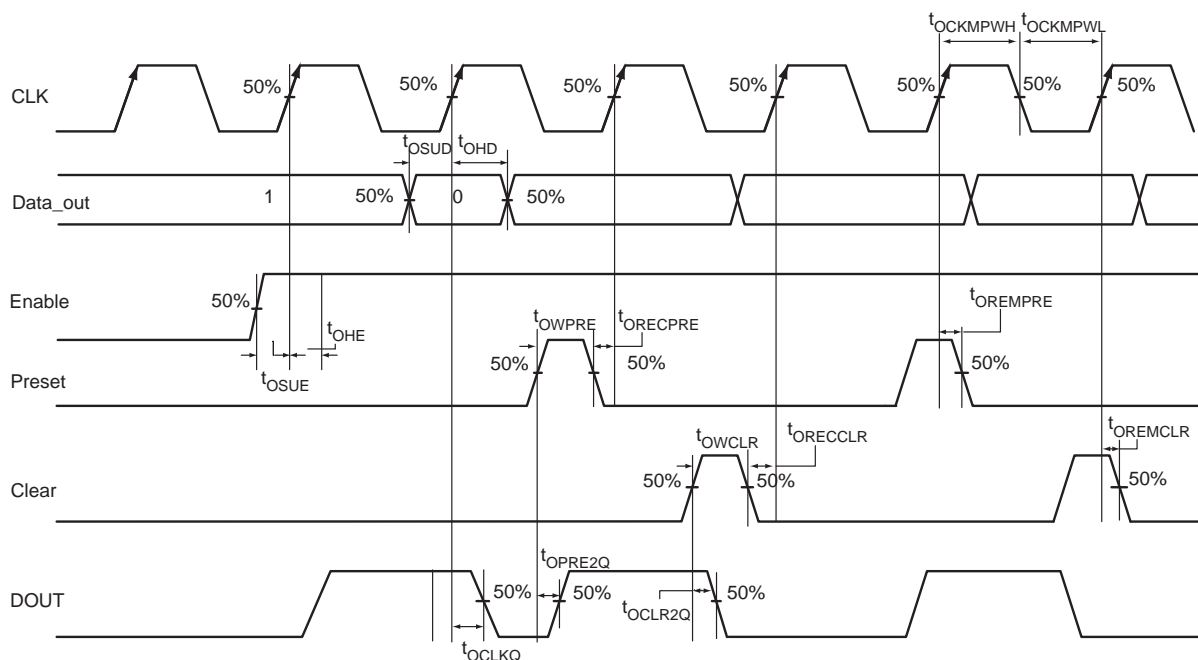
Parameter	Description	Std.	Units
$t_{ICLKQ}$	Clock-to-Q of the Input Data Register	0.42	ns
$t_{ISUD}$	Data Setup Time for the Input Data Register	0.47	ns
$t_{IHD}$	Data Hold Time for the Input Data Register	0.00	ns
$t_{ISUE}$	Enable Setup Time for the Input Data Register	0.67	ns
$t_{IHE}$	Enable Hold Time for the Input Data Register	0.00	ns
$t_{ICLR2Q}$	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
$t_{IPRE2Q}$	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
$t_{IWCLR}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{IWPRE}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**1.2 V DC Core Voltage**
**Table 2-157 • Input Data Register Propagation Delays**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Input Data Register	0.68	ns
$t_{\text{SUD}}$	Data Setup Time for the Input Data Register	0.97	ns
$t_{\text{HD}}$	Data Hold Time for the Input Data Register	0.00	ns
$t_{\text{SUE}}$	Enable Setup Time for the Input Data Register	1.02	ns
$t_{\text{IHE}}$	Enable Hold Time for the Input Data Register	0.00	ns
$t_{\text{CLR2Q}}$	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
$t_{\text{PRE2Q}}$	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{\text{REMCLR}}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{\text{RECCLR}}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{\text{REMPRE}}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{\text{RECPRE}}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
$t_{\text{WCLR}}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{\text{WPRE}}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{\text{CKMPWH}}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{\text{CKMPWL}}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Output Register**

**Figure 2-19 • Output Register Timing Diagram**



## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-158 • Output Data Register Propagation Delays**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
$t_{\text{OCLKQ}}$	Clock-to-Q of the Output Data Register	1.00	ns
$t_{\text{OSUD}}$	Data Setup Time for the Output Data Register	0.51	ns
$t_{\text{OHD}}$	Data Hold Time for the Output Data Register	0.00	ns
$t_{\text{OSUE}}$	Enable Setup Time for the Output Data Register	0.70	ns
$t_{\text{OHE}}$	Enable Hold Time for the Output Data Register	0.00	ns
$t_{\text{OCLR2Q}}$	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
$t_{\text{OPRE2Q}}$	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{\text{OREMCLR}}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{\text{ORECCLR}}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{\text{OREMPRE}}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{\text{ORECPRE}}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
$t_{\text{OWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{\text{OWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{\text{OCKMPWH}}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{\text{OCKMPWL}}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

### 1.2 V DC Core Voltage

**Table 2-159 • Output Data Register Propagation Delays**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
$t_{\text{OCLKQ}}$	Clock-to-Q of the Output Data Register	1.52	ns
$t_{\text{OSUD}}$	Data Setup Time for the Output Data Register	1.15	ns
$t_{\text{OHD}}$	Data Hold Time for the Output Data Register	0.00	ns
$t_{\text{OSUE}}$	Enable Setup Time for the Output Data Register	1.11	ns
$t_{\text{OHE}}$	Enable Hold Time for the Output Data Register	0.00	ns
$t_{\text{OCLR2Q}}$	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
$t_{\text{OPRE2Q}}$	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{\text{OREMCLR}}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{\text{ORECCLR}}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{\text{OREMPRE}}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{\text{ORECPRE}}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
$t_{\text{OWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{\text{OWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{\text{OCKMPWH}}$	Clock Minimum Pulse Width High for the Output Data Register	0.31	ns
$t_{\text{OCKMPWL}}$	Clock Minimum Pulse Width Low for the Output Data Register	0.28	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

## Output Enable Register

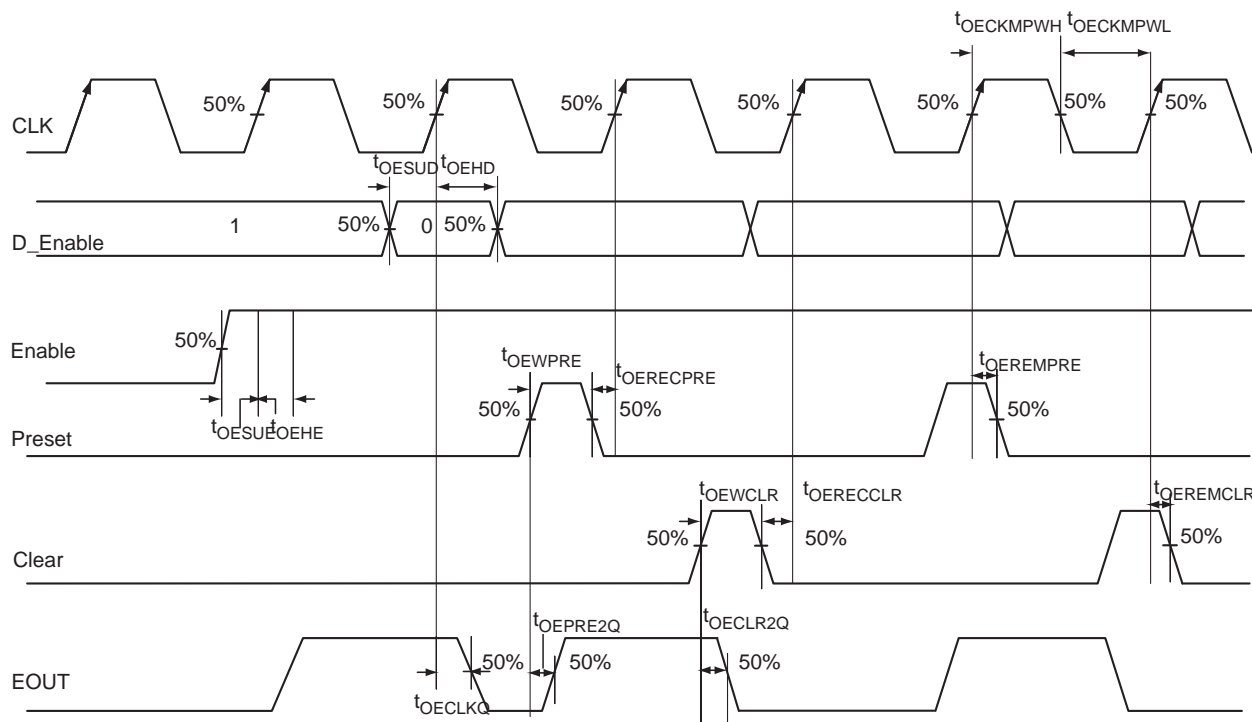


Figure 2-20 • Output Enable Register Timing Diagram

### Timing Characteristics

#### 1.5 V DC Core Voltage

Table 2-160 • Output Enable Register Propagation Delays

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	0.75	ns
$t_{OESUD}$	Data Setup Time for the Output Enable Register	0.51	ns
$t_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	0.73	ns
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRES}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

## 1.2 V DC Core Voltage

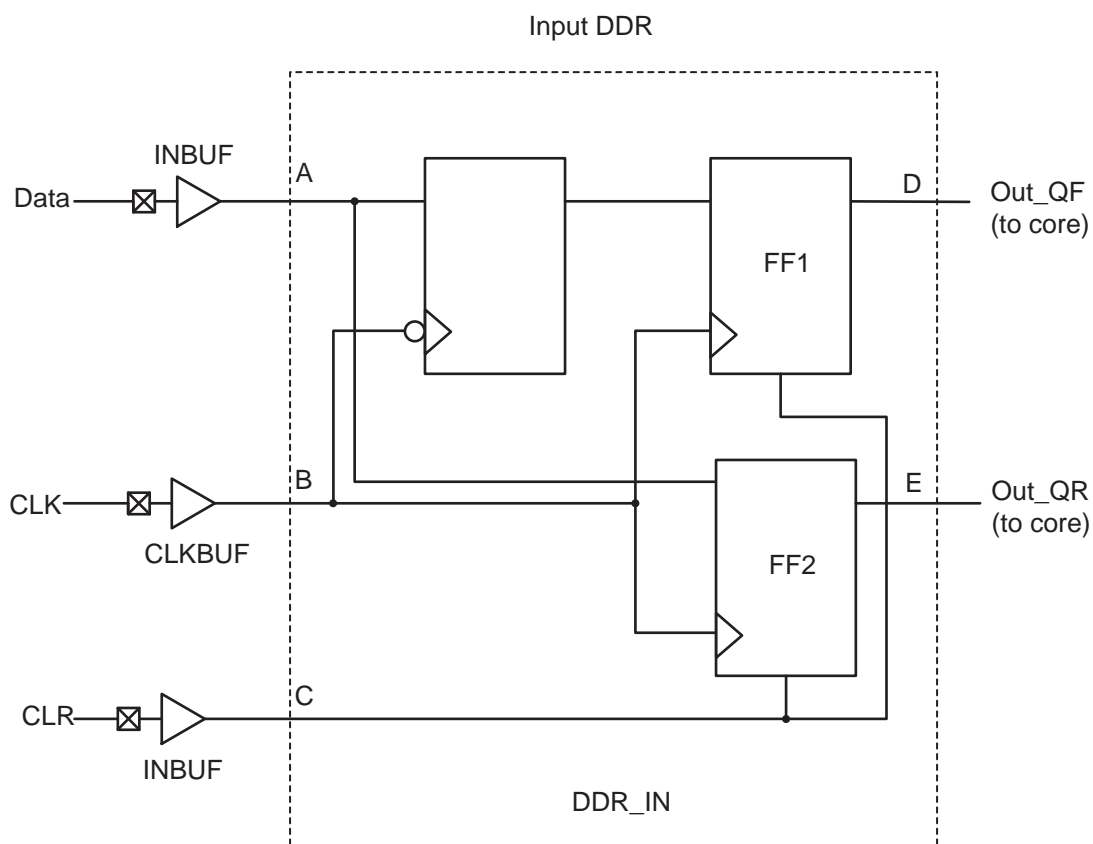
**Table 2-161 • Output Enable Register Propagation Delays**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	1.10	ns
$t_{OESUD}$	Data Setup Time for the Output Enable Register	1.15	ns
$t_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	ns
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	1.22	ns
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

## DDR Module Specifications

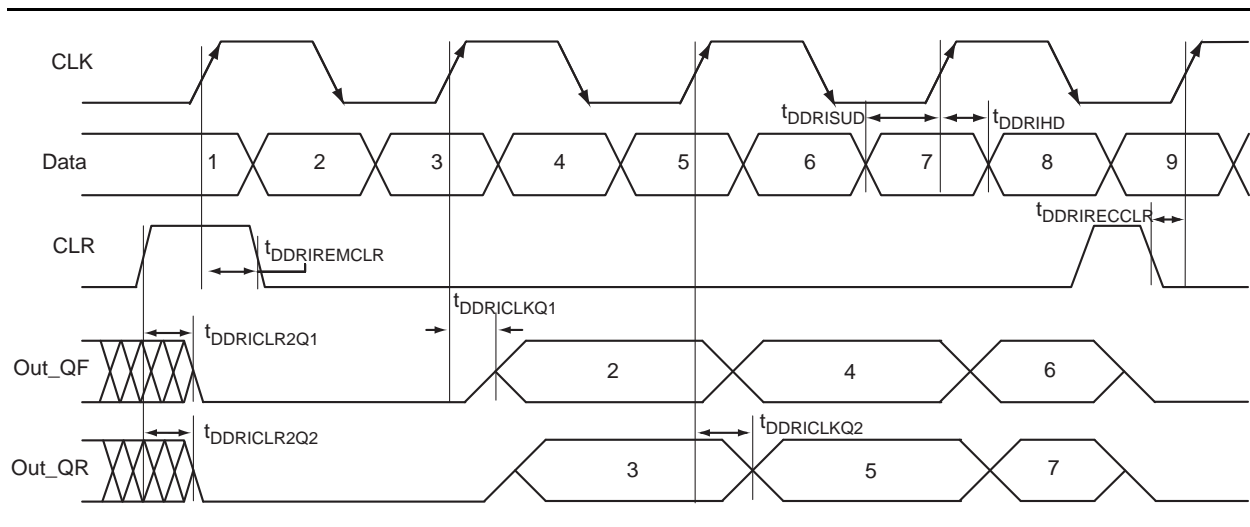
### Input DDR Module



**Figure 2-21 • Input DDR Timing Model**

**Table 2-162 • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{\text{DDRICKLQ1}}$	Clock-to-Out Out_QR	B, D
$t_{\text{DDRICKLQ2}}$	Clock-to-Out Out_QF	B, E
$t_{\text{DDRISUD}}$	Data Setup Time of DDR input	A, B
$t_{\text{DDRIHD}}$	Data Hold Time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B


**Figure 2-22 • Input DDR Timing Diagram**

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-163 • Input DDR Propagation Delays**
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	Std.	Units
$t_{\text{DDRICKQ1}}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{\text{DDRICKQ2}}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{\text{DDRISUD1}}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{\text{DDRISUD2}}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{\text{DDRHD1}}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{\text{DDRHD2}}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{\text{DDRWCLR}}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{\text{DDRIMAX}}$	Maximum Frequency for Input DDR	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7](#) on page 2-7 for derating values.

## 1.2 V DC Core Voltage

**Table 2-164 • Input DDR Propagation Delays**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
$t_{\text{DDRICKQ1}}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{\text{DDRICKQ2}}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{\text{DDRISUD1}}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{\text{DDRISUD2}}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{\text{DDRILD1}}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{\text{DDRILD2}}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{\text{DDRIRECLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{\text{DDRWCCLR}}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{\text{DDRIMAX}}$	Maximum Frequency for Input DDR	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

## Output DDR Module

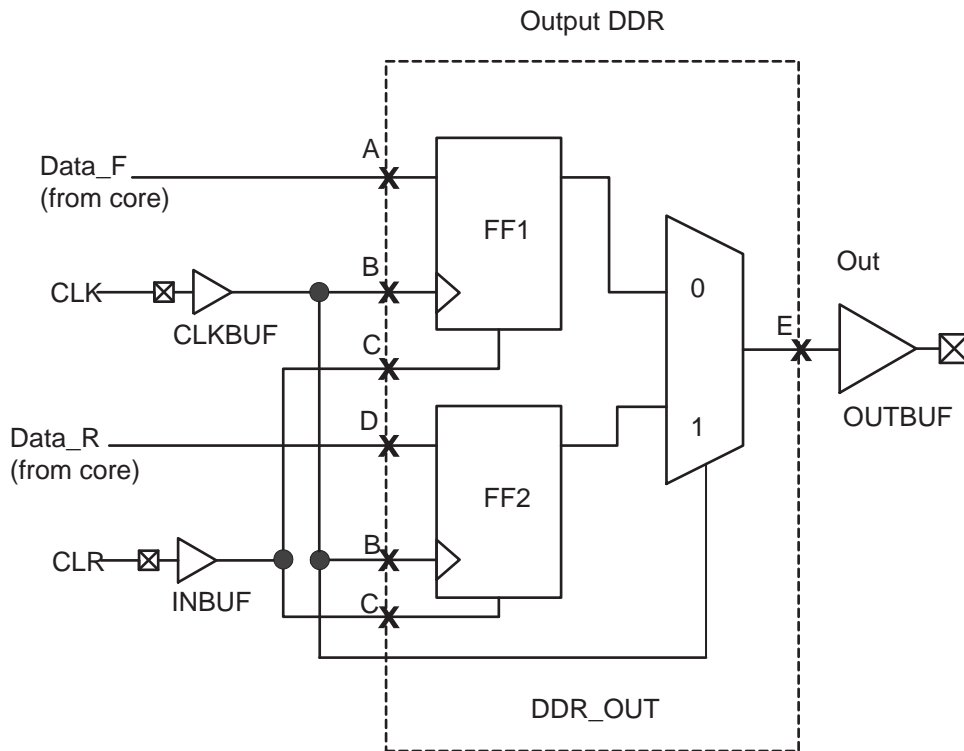
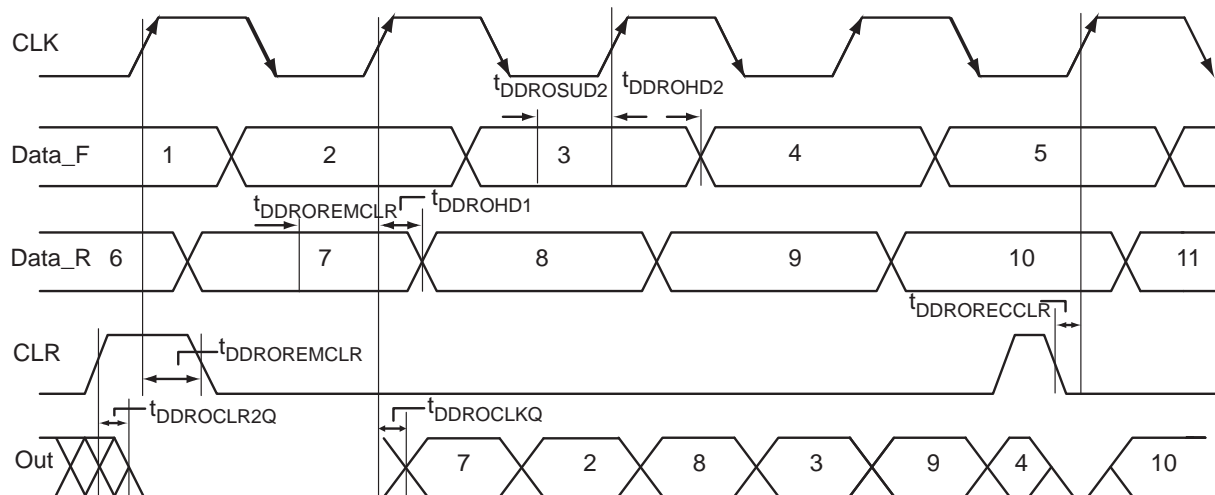


Figure 2-23 • Output DDR Timing Model

Table 2-165 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B


**Figure 2-24 • Output DDR Timing Diagram**

### Timing Characteristics

1.5 V DC Core Voltage

**Table 2-166 • Output DDR Propagation Delays**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
$t_{\text{DDROCLKQ}}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{\text{DDROSUD1}}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{\text{DDROSUD2}}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{\text{DDROHD1}}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{\text{DDROHD2}}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{\text{DDROEMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
$F_{\text{DDOMAX}}$	Maximum Frequency for the Output DDR	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.



## 1.2 V DC Core Voltage

Table 2-167 • Output DDR Propagation Delays

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.	Units
$t_{\text{DDROCLKQ}}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{\text{DDROSUD1}}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{\text{DDROSUD2}}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{\text{DDROHD1}}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{\text{DDROHD2}}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
$F_{\text{DDOMAX}}$	Maximum Frequency for the Output DDR	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## VersaTile Characteristics

### VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

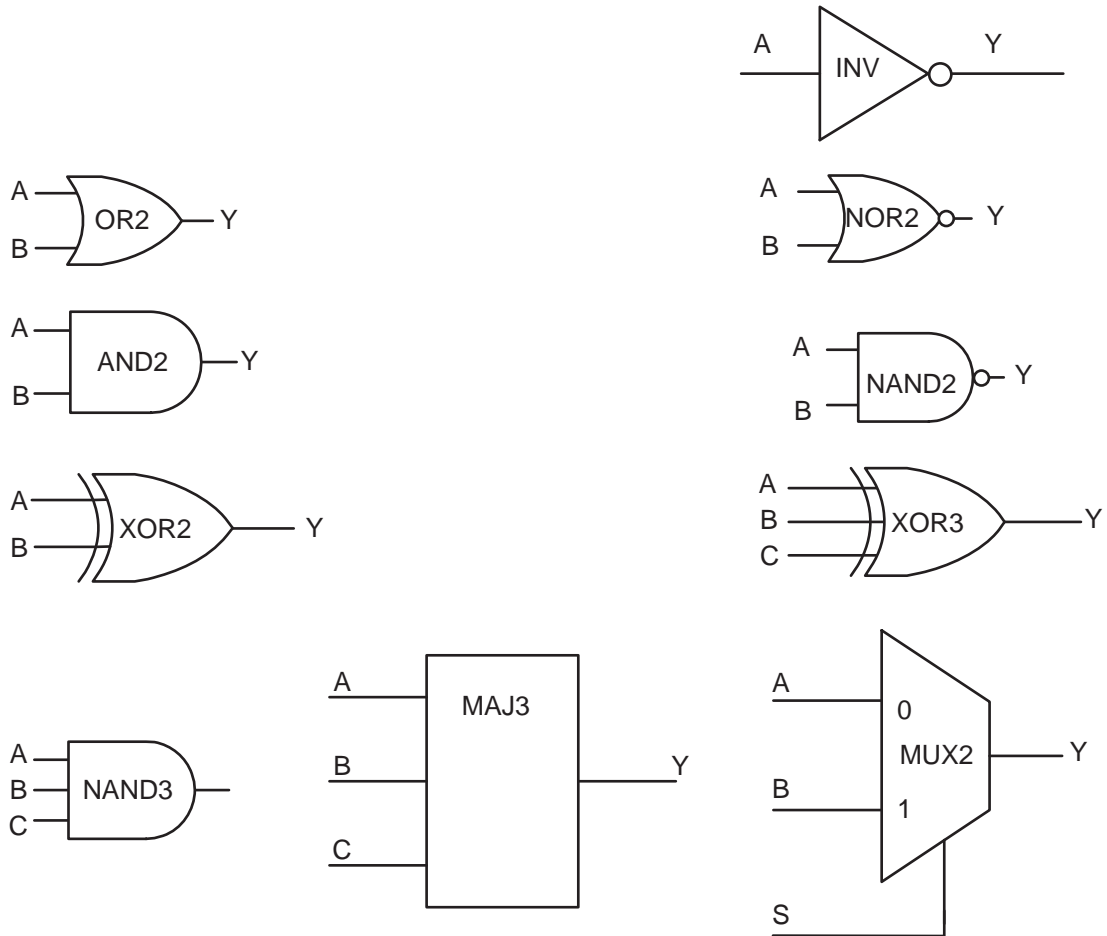


Figure 2-25 • Sample of Combinatorial Cells

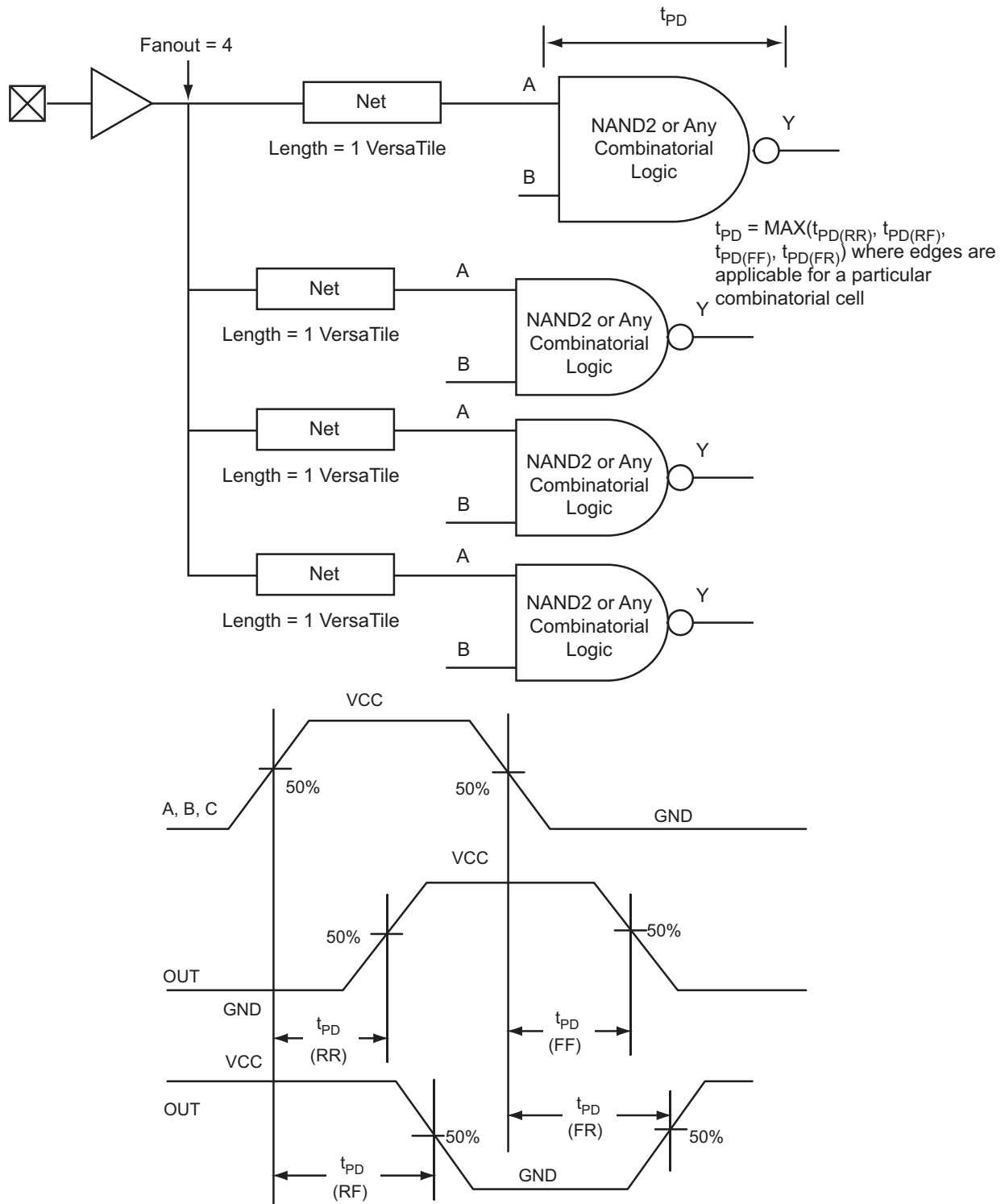


Figure 2-26 • Timing Model and Waveforms

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-168 • Combinatorial Cell Propagation Delays**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	$t_{PD}$	0.80	ns
AND2	$Y = A \cdot B$	$t_{PD}$	0.84	ns
NAND2	$Y = !(A \cdot B)$	$t_{PD}$	0.90	ns
OR2	$Y = A + B$	$t_{PD}$	1.19	ns
NOR2	$Y = !(A + B)$	$t_{PD}$	1.10	ns
XOR2	$Y = A \oplus B$	$t_{PD}$	1.37	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	$t_{PD}$	1.33	ns
XOR3	$Y = A \oplus B \oplus C$	$t_{PD}$	1.79	ns
MUX2	$Y = A !S + B S$	$t_{PD}$	1.48	ns
AND3	$Y = A \cdot B \cdot C$	$t_{PD}$	1.21	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

### 1.2 V DC Core Voltage

**Table 2-169 • Combinatorial Cell Propagation Delays**  
Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	$t_{PD}$	1.34	ns
AND2	$Y = A \cdot B$	$t_{PD}$	1.43	ns
NAND2	$Y = !(A \cdot B)$	$t_{PD}$	1.59	ns
OR2	$Y = A + B$	$t_{PD}$	2.30	ns
NOR2	$Y = !(A + B)$	$t_{PD}$	2.07	ns
XOR2	$Y = A \oplus B$	$t_{PD}$	2.46	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	$t_{PD}$	2.46	ns
XOR3	$Y = A \oplus B \oplus C$	$t_{PD}$	3.12	ns
MUX2	$Y = A !S + B S$	$t_{PD}$	2.83	ns
AND3	$Y = A \cdot B \cdot C$	$t_{PD}$	2.28	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

## VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

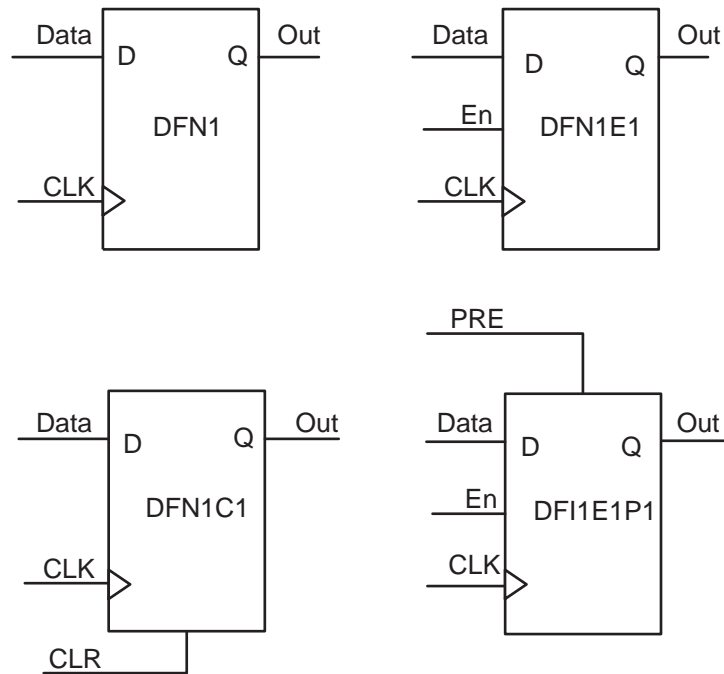
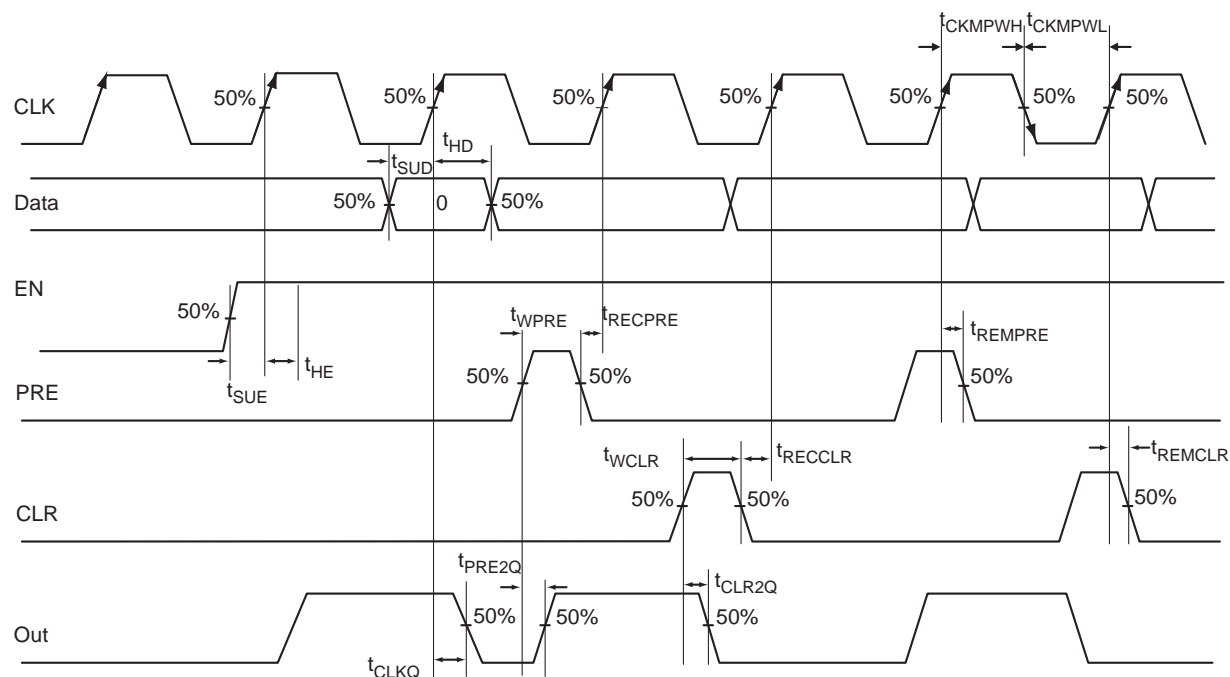


Figure 2-27 • Sample of Sequential Cells


**Figure 2-28 • Timing Model and Waveforms**

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-170 • Register Delays**

 Commercial-Case Conditions:  $T_j = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ 

Parameter	Description	Std.	Units
$t_{CLKQ}$	Clock-to-Q of the Core Register	0.89	ns
$t_{SUD}$	Data Setup Time for the Core Register	0.81	ns
$t_{HD}$	Data Hold Time for the Core Register	0.00	ns
$t_{SUE}$	Enable Setup Time for the Core Register	0.73	ns
$t_{HE}$	Enable Hold Time for the Core Register	0.00	ns
$t_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.60	ns
$t_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.62	ns
$t_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	ns
$t_{RECCLR}$	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
$t_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	ns
$t_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
$t_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
$t_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
$t_{CKMPWH}$	Clock Minimum Pulse Width High for the Core Register	0.56	ns
$t_{CKMPWL}$	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

## 1.2 V DC Core Voltage

**Table 2-171 • Register Delays**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Core Register	1.61	ns
$t_{\text{SUD}}$	Data Setup Time for the Core Register	1.17	ns
$t_{\text{HD}}$	Data Hold Time for the Core Register	0.00	ns
$t_{\text{SUE}}$	Enable Setup Time for the Core Register	1.29	ns
$t_{\text{HE}}$	Enable Hold Time for the Core Register	0.00	ns
$t_{\text{CLR2Q}}$	Asynchronous Clear-to-Q of the Core Register	0.87	ns
$t_{\text{PRE2Q}}$	Asynchronous Preset-to-Q of the Core Register	0.89	ns
$t_{\text{REMCLR}}$	Asynchronous Clear Removal Time for the Core Register	0.00	ns
$t_{\text{RECCLR}}$	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
$t_{\text{REMPRE}}$	Asynchronous Preset Removal Time for the Core Register	0.00	ns
$t_{\text{RECPRE}}$	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
$t_{\text{WCLR}}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
$t_{\text{WPRE}}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
$t_{\text{CKMPWH}}$	Clock Minimum Pulse Width High for the Core Register	0.95	ns
$t_{\text{CKMPWL}}$	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

## Global Resource Characteristics

### AGL250 Clock Tree Topology

Clock delays are device-specific. Figure 2-29 is an example of a global tree used for clock routing. The global tree presented in Figure 2-29 is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

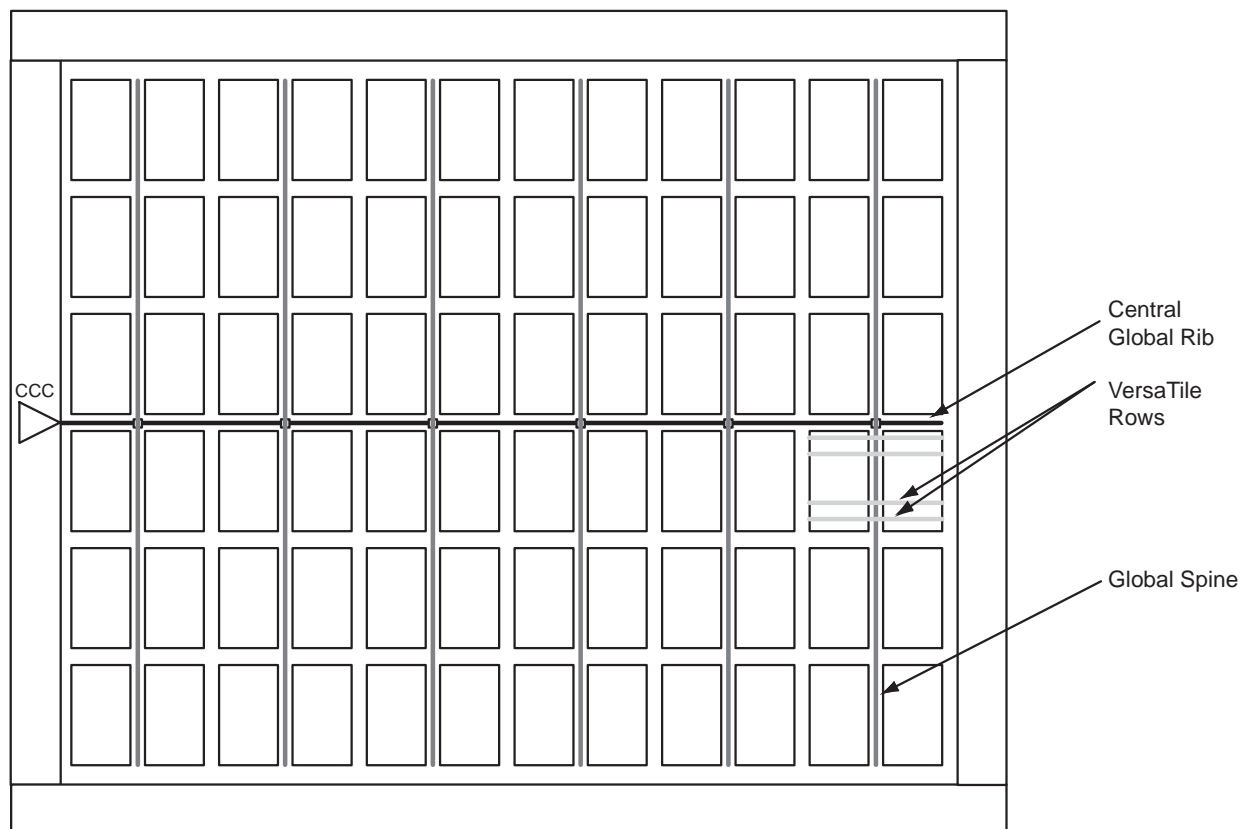


Figure 2-29 • Example of Global Tree Use in an AGL250 Device for Clock Routing



## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-172 to Table 2-187 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-172 • AGL015 Global Resource**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.21	1.42	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

#### Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-173 • AGL030 Global Resource**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.21	1.42	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

#### Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-174 • AGL060 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.33	1.55	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.35	1.62	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-175 • AGL125 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.36	1.71	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.43	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-176 • AGL250 Global Resource****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.39	1.73	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.43	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-177 • AGL400 Global Resource****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.45	1.79	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.48	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.43	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-178 • AGL600 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.48	1.82	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.42	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-179 • AGL1000 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.55	1.89	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.60	2.02	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.42	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

### 1.2 V DC Core Voltage

**Table 2-180 • AGL015 Global Resource**

 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.79	2.09	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.87	2.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.39	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-181 • AGL030 Global Resource**

 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.80	2.09	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.39	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-182 • AGL060 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.04	2.33	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.10	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.40	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-183 • AGL125 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.08	2.54	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.62	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-184 • AGL250 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.11	2.57	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.62	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-185 • AGL400 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.18	2.64	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.27	2.89	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.62	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-186 • AGL600 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.22	2.67	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.61	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-187 • AGL1000 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.31	2.76	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock			ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.61	ns
$F_{RMAX}$	Maximum Frequency for Global Clock			MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.



## Clock Conditioning Circuits

### CCC Electrical Specifications

#### Timing Characteristics

**Table 2-188 • IGLOO CCC/PLL Specification**  
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$	0.75		250	MHz
Delay Increments in Programmable Delay Blocks <sup>1, 2</sup>		360		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL <sup>3</sup>			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$	Maximum Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 250 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1, 2, 4</sup>	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 <sup>1, 2, 4</sup>	0.469		15.65	ns
Delay Range in Block: Fixed Delay <sup>1, 2, 4</sup>		3.5		ns

#### Notes:

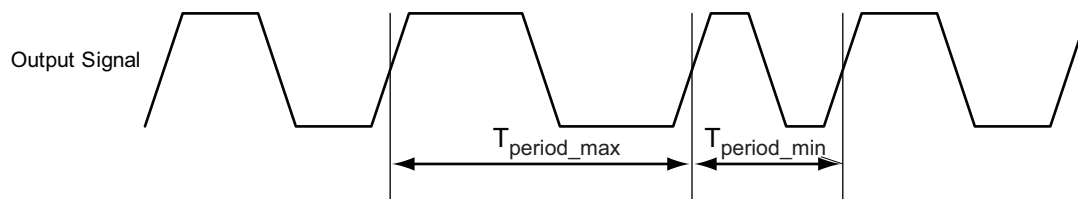
1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-7](#) and [Table 2-7 on page 2-7](#) for deratings.
2.  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 1.5\text{ V}$
3. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
4. For the definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the [IGLOO FPGA Fabric User's Guide](#).
5. The AGL030 device does not support PLL.
6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.

**Table 2-189 • IGLOO CCC/PLL Specification**  
**For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$	0.75		160	MHz
Delay Increments in Programmable Delay Blocks <sup>1, 2</sup>		580		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL <sup>3</sup>			60	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$	Maximum Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 160 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
	LockControl = 0		300	μs
	LockControl = 1		6.0	ms
Tracking Jitter				
	LockControl = 0		4	ns
	LockControl = 1		3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1, 2, 4</sup>	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 <sup>1, 2, 4</sup>	0.863		20.86	ns
Delay Range in Block: Fixed Delay <sup>1, 2, 4</sup>		5.7		ns

**Notes:**

1. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-7](#) and [Table 2-7 on page 2-7](#) for deratings.
2.  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 1.5\text{ V}$
3. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
4. For the definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the Clock Conditioning Circuits in IGLOO and ProASIC3 Devices chapter of the [IGLOO FPGA Fabric User's Guide](#).
5. The AGL030 device does not support PLL.
6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.



*Note:* Peak-to-peak jitter measurements are defined by  $T_{\text{peak-to-peak}} = T_{\text{period\_max}} - T_{\text{period\_min}}$ .

**Figure 2-30 • Peak-to-Peak Jitter Definition**

## Embedded SRAM and FIFO Characteristics

### SRAM

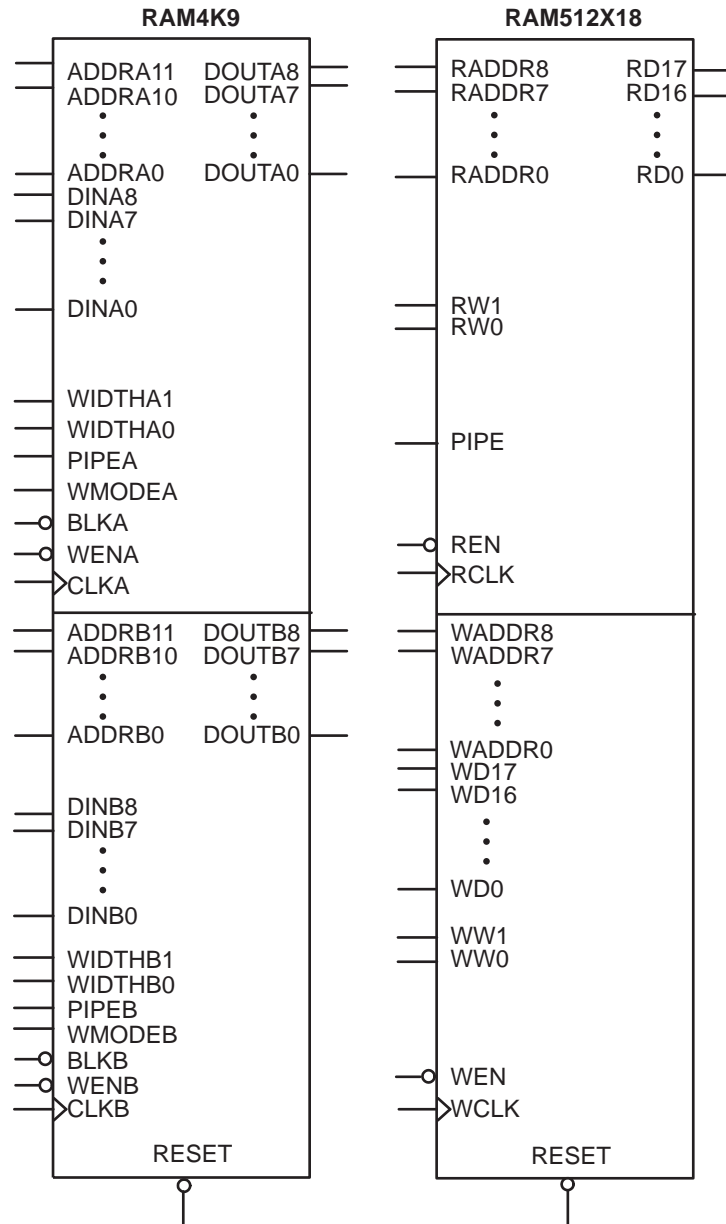


Figure 2-31 • RAM Models

## Timing Waveforms

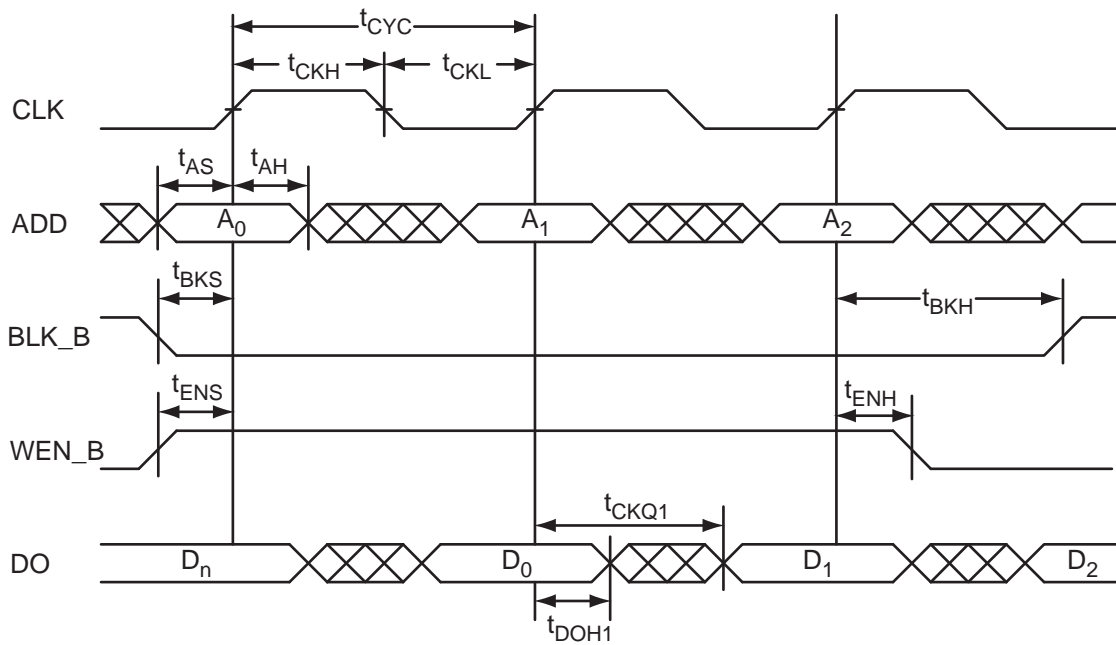


Figure 2-32 • RAM Read for Pass-Through Output

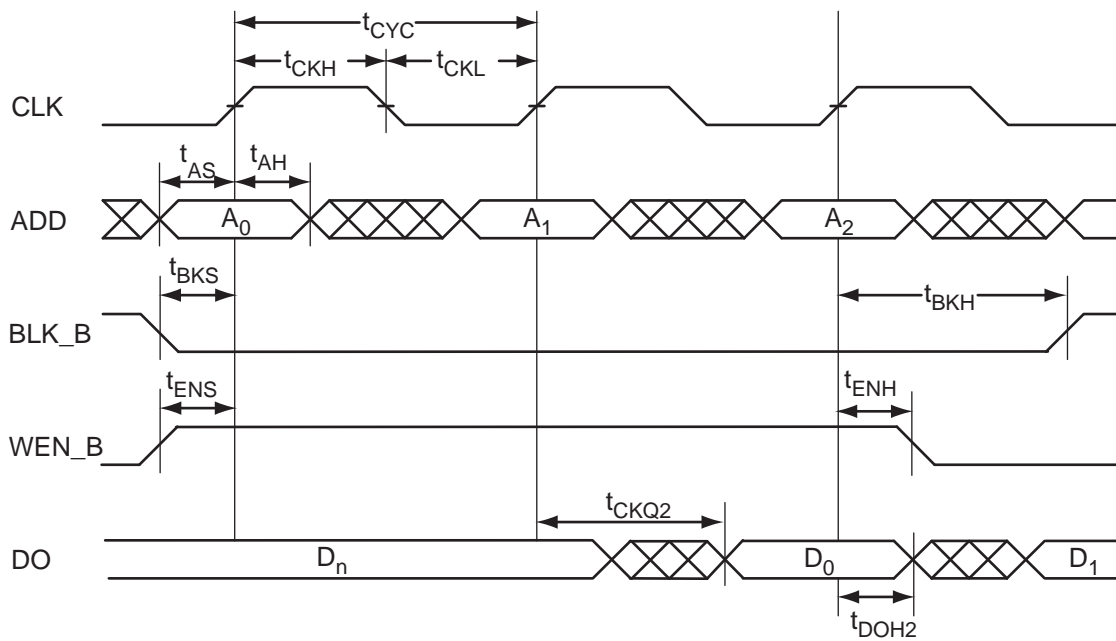
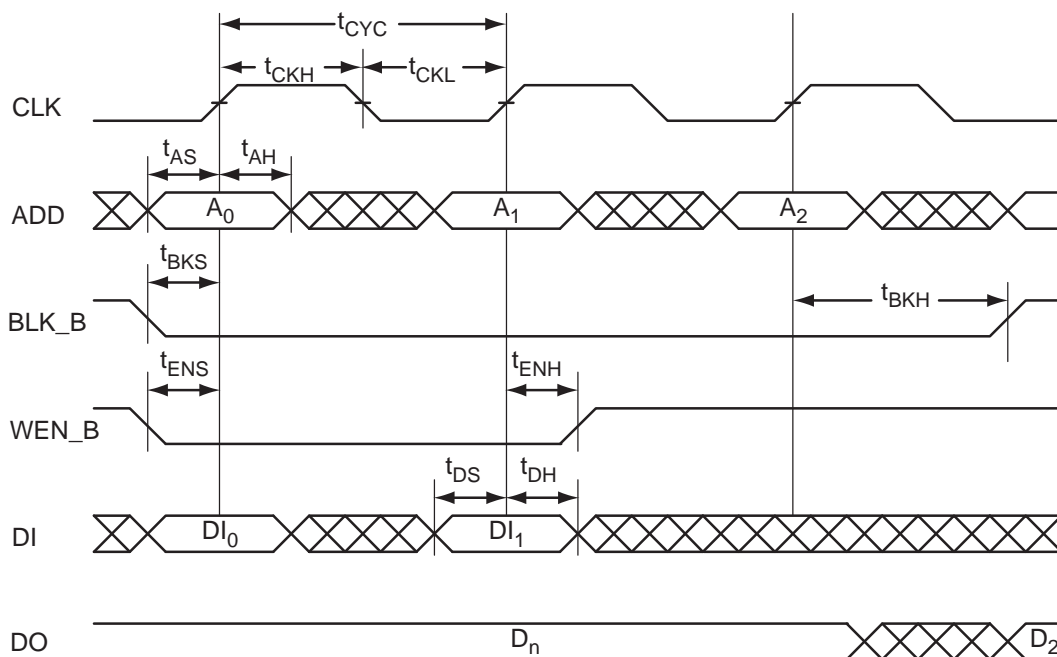
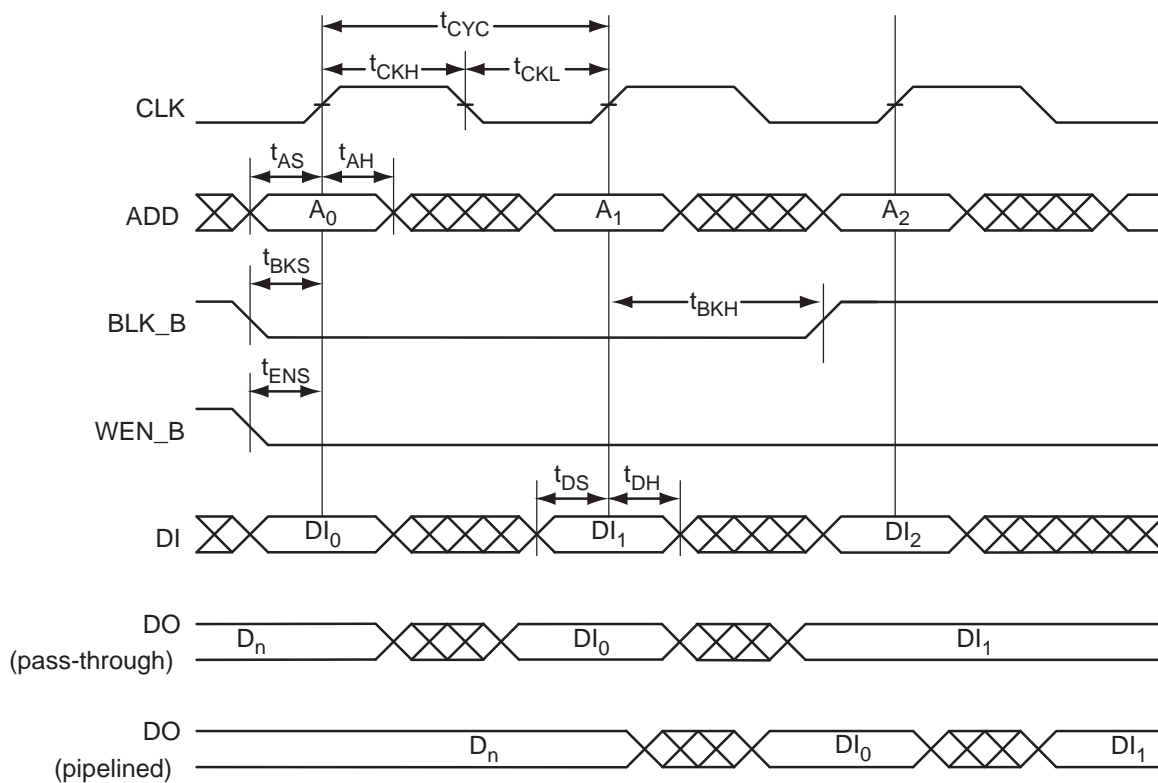


Figure 2-33 • RAM Read for Pipelined Output


**Figure 2-34 • RAM Write, Output Retained (WMODE = 0)**

**Figure 2-35 • RAM Write, Output as Write Data (WMODE = 1)**

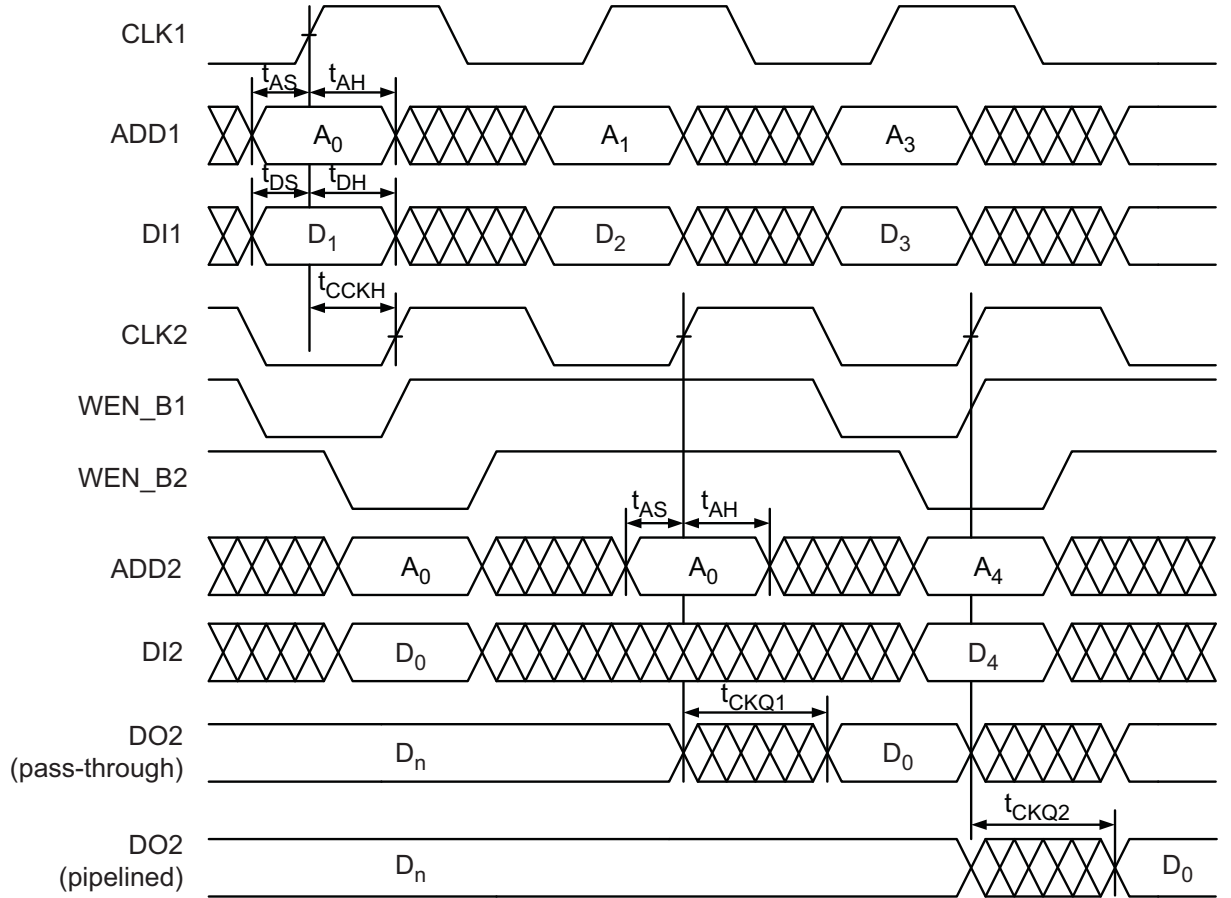
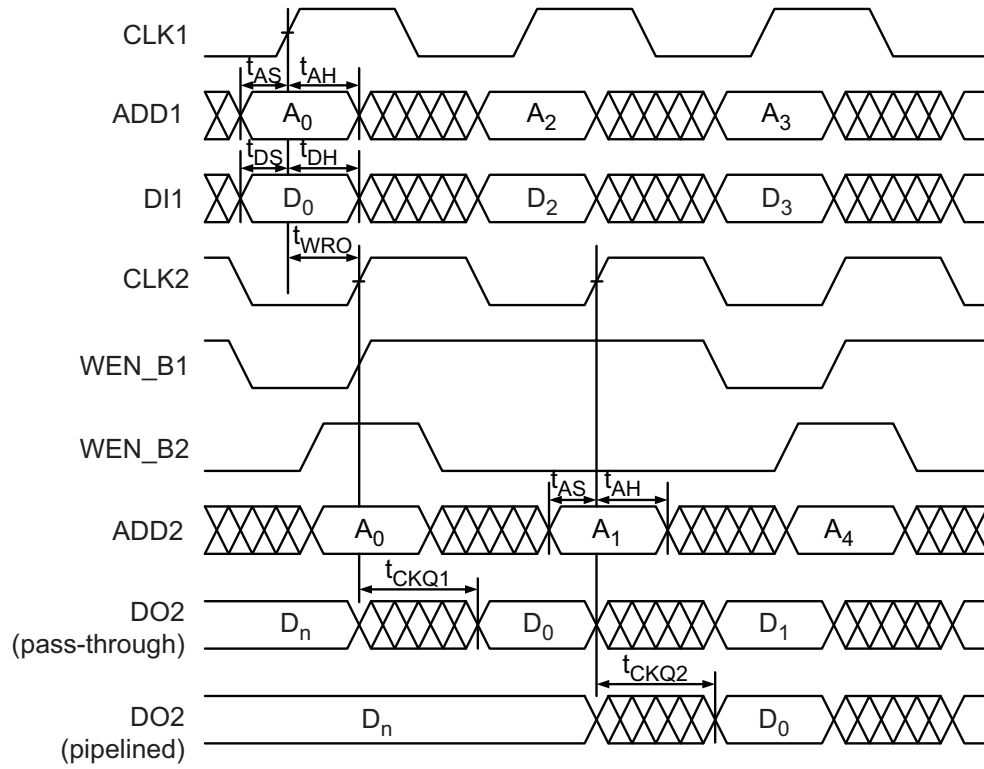


Figure 2-36 • Write Access after Write onto Same Address



**Figure 2-37 • Read Access after Write onto Same Address**



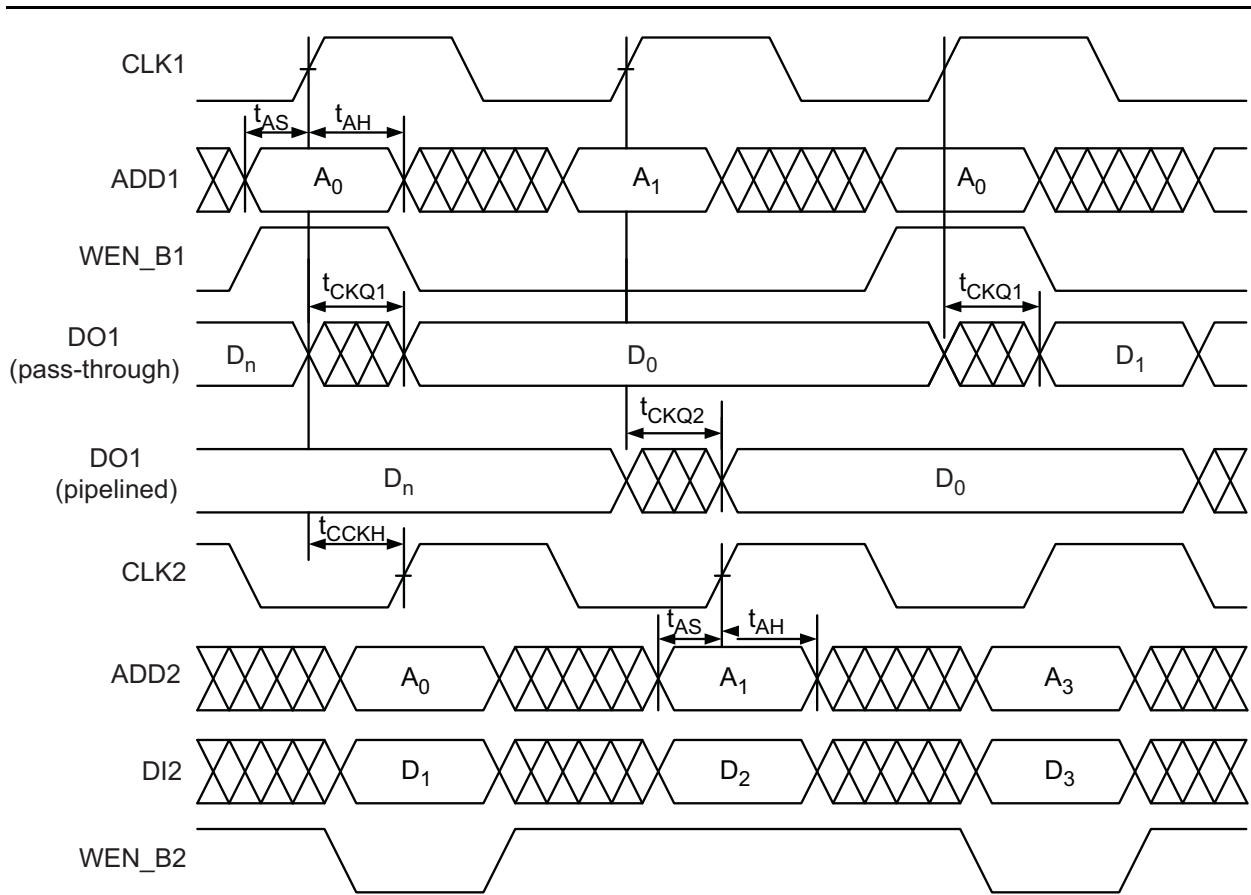


Figure 2-38 • Write Access after Read onto Same Address

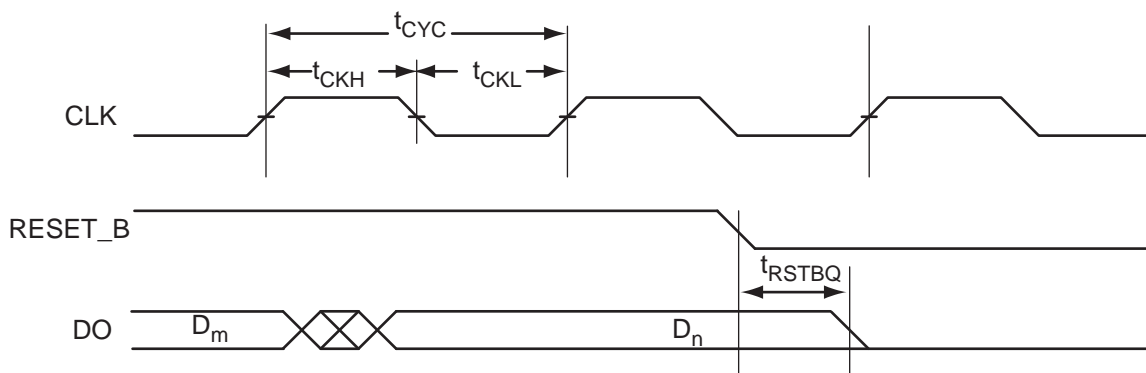


Figure 2-39 • RAM Reset

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-190 • RAM4K9**

**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.	Units
$t_{AS}$	Address setup time	0.83	ns
$t_{AH}$	Address hold time	0.16	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.81	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.16	ns
$t_{BKS}$	BLK_B setup time	1.65	ns
$t_{BKH}$	BLK_B hold time	0.16	ns
$t_{DS}$	Input data (DI) setup time	0.71	ns
$t_{DH}$	Input data (DI) hold time	0.36	ns
$t_{CKQ1}$	Clock High to new data valid on DO (output retained, WMODE = 0)	3.53	ns
	Clock High to new data valid on DO (flow-through, WMODE = 1)	3.06	ns
$t_{CKQ2}$	Clock High to new data valid on DO (pipelined)	1.81	ns
$t_{C2CWWL}$	Address collision clk-to-clk delay for reliable write after write on same address - Applicable to Closing Edge	0.23	ns
$t_{C2CRWL}$	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.35	ns
$t_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	0.41	ns
$t_{RSTBQ}$	RESET_B Low to data out Low on DO (flow-through)	2.06	ns
	RESET_B Low to data out Low on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B removal	0.61	ns
$t_{RECRSTB}$	RESET_B recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.68	ns
$t_{CYC}$	Clock cycle time	6.24	ns
$F_{MAX}$	Maximum frequency	160	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

**Table 2-191 • RAM512X18****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	Std.	Units
$t_{AS}$	Address setup time	0.83	ns
$t_{AH}$	Address hold time	0.16	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.73	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.08	ns
$t_{DS}$	Input data (DI) setup time	0.71	ns
$t_{DH}$	Input data (DI) hold time	0.36	ns
$t_{CKQ1}$	Clock High to new data valid on DO (output retained, WMODE = 0)	4.21	ns
$t_{CKQ2}$	Clock High to new data valid on DO (pipelined)	1.71	ns
$t_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.35	ns
$t_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	0.42	ns
$t_{RSTBQ}$	RESET_B Low to data out Low on DO (flow-through)	2.06	ns
	RESET_B Low to data out Low on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B removal	0.61	ns
$t_{RECRSTB}$	RESET_B recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.68	ns
$t_{CYC}$	Clock cycle time	6.24	ns
$F_{MAX}$	Maximum frequency	160	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

### 1.2 V DC Core Voltage

**Table 2-192 • RAM4K9**
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$** 

Parameter	Description	Std.	Units
$t_{AS}$	Address setup time	1.53	ns
$t_{AH}$	Address hold time	0.29	ns
$t_{ENS}$	REN_B, WEN_B setup time	1.50	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.29	ns
$t_{BKS}$	BLK_B setup time	3.05	ns
$t_{BKH}$	BLK_B hold time	0.29	ns
$t_{DS}$	Input data (DI) setup time	1.33	ns
$t_{DH}$	Input data (DI) hold time	0.66	ns
$t_{CKQ1}$	Clock High to new data valid on DO (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DO (flow-through, WMODE = 1)	5.72	ns
$t_{CKQ2}$	Clock High to new data valid on DO (pipelined)	3.38	ns
$t_{C2CWWL}$	Address collision clk-to-clk delay for reliable write after write on same address - Applicable to Closing Edge	0.30	ns
$t_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.89	ns
$t_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	1.01	ns
$t_{RSTBQ}$	RESET_B Low to data out Low on DO (flow-through)	3.86	ns
	RESET_B Low to data out Low on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B removal	1.12	ns
$t_{RECRSTB}$	RESET_B recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	1.18	ns
$t_{CYC}$	Clock cycle time	10.90	ns
$F_{MAX}$	Maximum frequency	92	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-193 • RAM512X18

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.	Units
$t_{AS}$	Address setup time	1.53	ns
$t_{AH}$	Address hold time	0.29	ns
$t_{ENS}$	REN_B, WEN_B setup time	1.36	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.15	ns
$t_{DS}$	Input data (DI) setup time	1.33	ns
$t_{DH}$	Input data (DI) hold time	0.66	ns
$t_{CKQ1}$	Clock High to new data valid on DO (output retained, WMODE = 0)	7.88	ns
$t_{CKQ2}$	Clock High to new data valid on DO (pipelined)	3.20	ns
$t_{C2CRWH}$	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.87	ns
$t_{C2CWRH}$	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	1.04	ns
$t_{RSTBQ}$	RESET_B Low to data out Low on DO (flow through)	3.86	ns
	RESET_B Low to data out Low on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B removal	1.12	ns
$t_{RECRSTB}$	RESET_B recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	1.18	ns
$t_{CYC}$	Clock cycle time	10.90	ns
$F_{MAX}$	Maximum frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## FIFO

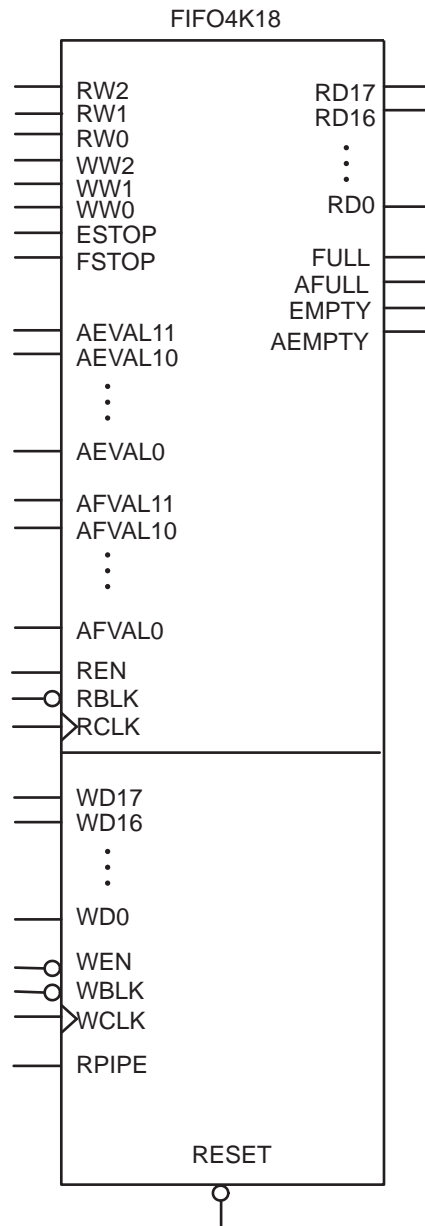


Figure 2-40 • FIFO Model

## Timing Waveforms

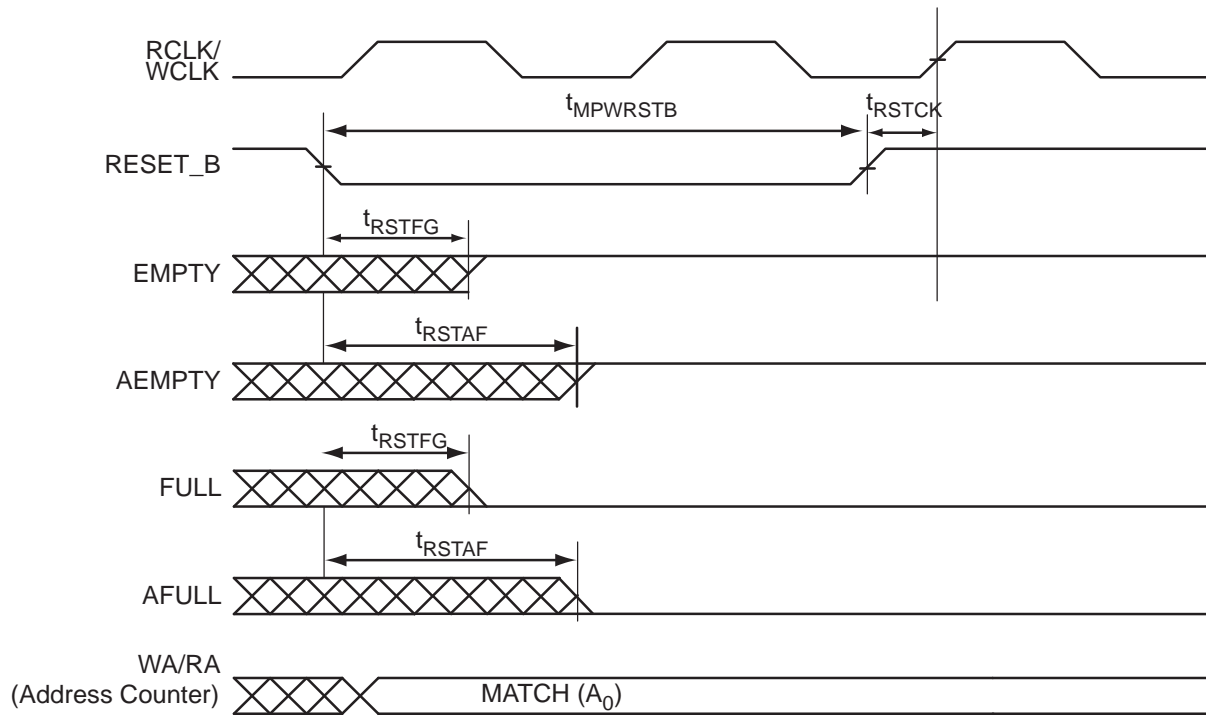


Figure 2-41 • FIFO Reset

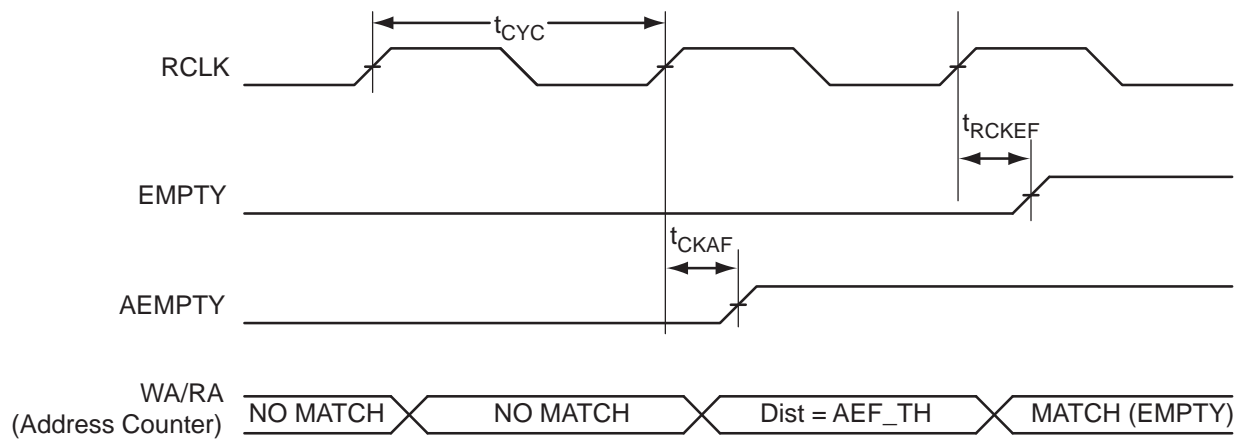


Figure 2-42 • FIFO EMPTY Flag and AEMPTY Flag Assertion

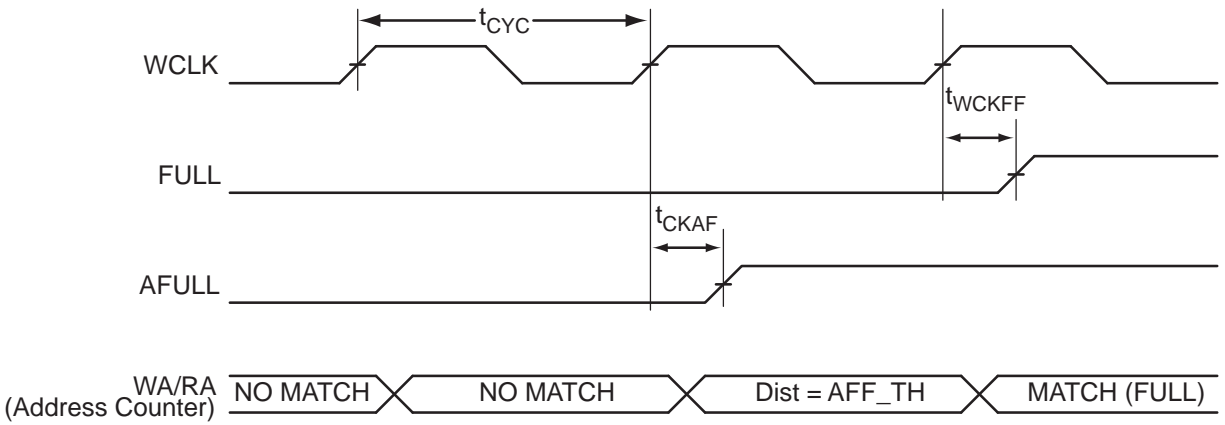


Figure 2-43 • FIFO FULL Flag and AFULL Flag Assertion

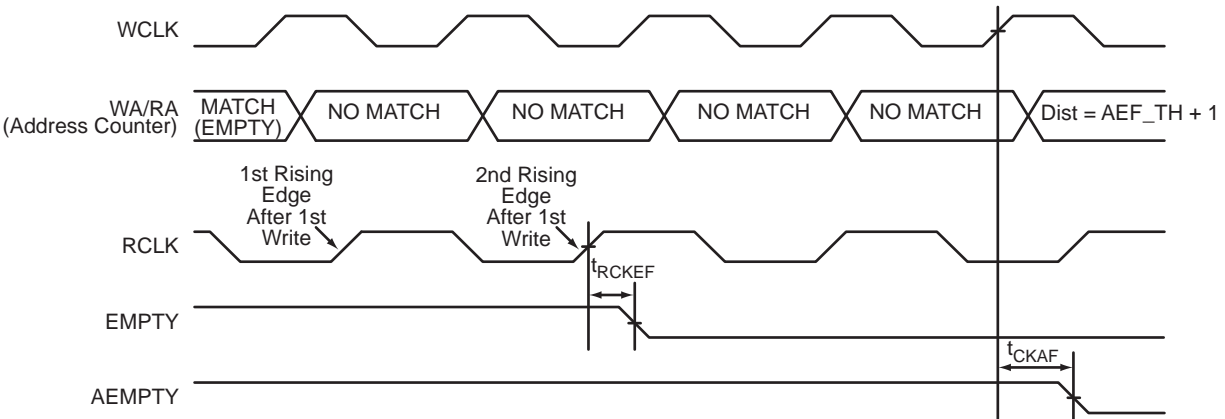


Figure 2-44 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

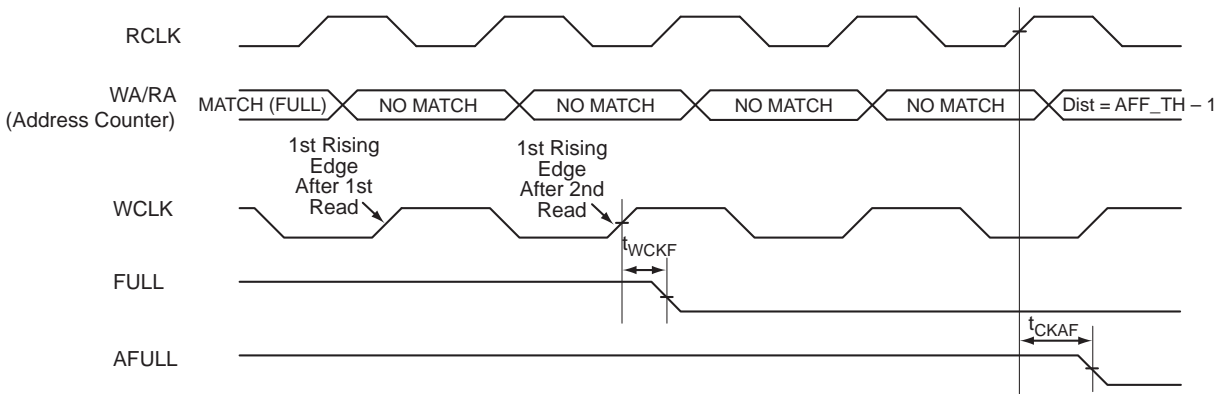


Figure 2-45 • FIFO FULL Flag and AFULL Flag Deassertion



## Timing Characteristics

### 1.5 V DC Core Voltage

Table 2-194 • FIFO

Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
$t_{ENS}$	REN_B, WEN_B Setup Time	1.99	ns
$t_{ENH}$	REN_B, WEN_B Hold Time	0.16	ns
$t_{BKS}$	BLK_B Setup Time	0.30	ns
$t_{BKH}$	BLK_B Hold Time	0.00	ns
$t_{DS}$	Input Data (DI) Setup Time	0.76	ns
$t_{DH}$	Input Data (DI) Hold Time	0.25	ns
$t_{CKQ1}$	Clock High to New Data Valid on DO (flow-through)	3.33	ns
$t_{CKQ2}$	Clock High to New Data Valid on DO (pipelined)	1.80	ns
$t_{RCKEF}$	RCLK High to Empty Flag Valid	3.53	ns
$t_{WCKFF}$	WCLK High to Full Flag Valid	3.35	ns
$t_{CKAF}$	Clock High to Almost Empty/Full Flag Valid	12.85	ns
$t_{RSTFG}$	RESET_B Low to Empty/Full Flag Valid	3.48	ns
$t_{RSTAF}$	RESET_B Low to Almost Empty/Full Flag Valid	12.72	ns
$t_{RSTBQ}$	RESET_B Low to Data Out Low on DO (flow-through)	2.02	ns
	RESET_B Low to Data Out Low on DO (pipelined)	2.02	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.68	ns
$t_{CYC}$	Clock Cycle Time	6.24	ns
$F_{MAX}$	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

## 1.2 V DC Core Voltage

Table 2-195 • FIFO

Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$ 

Parameter	Description	Std.	Units
$t_{ENS}$	REN_B, WEN_B Setup Time	4.13	ns
$t_{ENH}$	REN_B, WEN_B Hold Time	0.31	ns
$t_{BKS}$	BLK_B Setup Time	0.47	ns
$t_{BKH}$	BLK_B Hold Time	0.00	ns
$t_{DS}$	Input Data (DI) Setup Time	1.56	ns
$t_{DH}$	Input Data (DI) Hold Time	0.49	ns
$t_{CKQ1}$	Clock High to New Data Valid on DO (flow-through)	6.80	ns
$t_{CKQ2}$	Clock High to New Data Valid on DO (pipelined)	3.62	ns
$t_{RCKEF}$	RCLK High to Empty Flag Valid	7.23	ns
$t_{WCKFF}$	WCLK High to Full Flag Valid	6.85	ns
$t_{CKAF}$	Clock High to Almost Empty/Full Flag Valid	26.61	ns
$t_{RSTFG}$	RESET_B Low to Empty/Full Flag Valid	7.12	ns
$t_{RSTAF}$	RESET_B Low to Almost Empty/Full Flag Valid	26.33	ns
$t_{RSTBQ}$	RESET_B Low to Data Out Low on DO (flow-through)	4.09	ns
	RESET_B Low to Data Out Low on DO (pipelined)	4.09	ns
$t_{REMRSTB}$	RESET_B Removal	1.23	ns
$t_{RECRSTB}$	RESET_B Recovery	6.58	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.18	ns
$t_{CYC}$	Clock Cycle Time	10.90	ns
$F_{MAX}$	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## Embedded FlashROM Characteristics

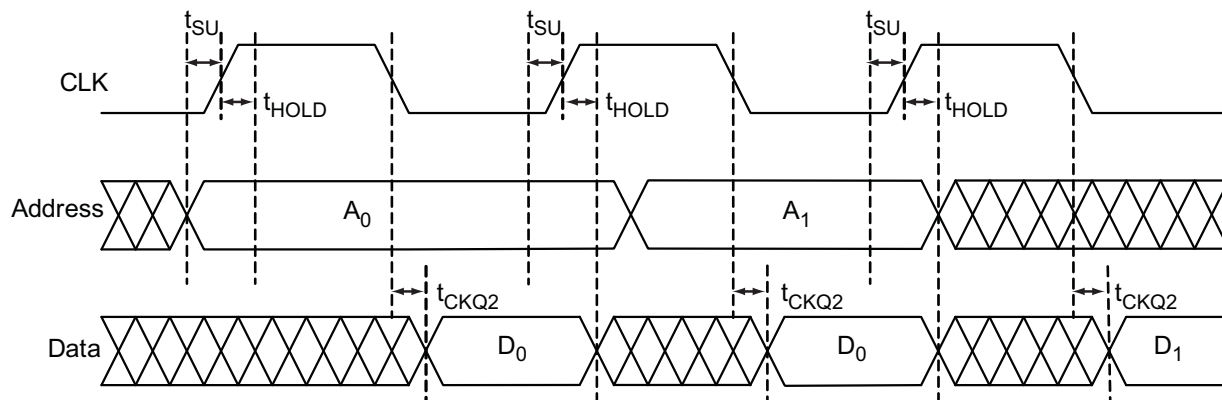


Figure 2-46 • Timing Diagram

### Timing Characteristics

#### 1.5 V DC Core Voltage

Table 2-196 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
$t_{SU}$	Address Setup Time	0.57	ns
$t_{HOLD}$	Address Hold Time	0.00	ns
$t_{CKQ2}$	Clock to Out	34.14	ns
$F_{MAX}$	Maximum Clock Frequency	15	MHz

#### 1.2 V DC Core Voltage

Table 2-197 • Embedded FlashROM Access Time

Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
$t_{SU}$	Address Setup Time	0.59	ns
$t_{HOLD}$	Address Hold Time	0.00	ns
$t_{CKQ2}$	Clock to Out	52.90	ns
$F_{MAX}$	Maximum Clock Frequency	10	MHz

## JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

### Timing Characteristics

**Table 2-198 • JTAG 1532**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{\text{DISU}}$	Test Data Input Setup Time	1.00	ns
$t_{\text{DIHD}}$	Test Data Input Hold Time	2.00	ns
$t_{\text{TMSU}}$	Test Mode Select Setup Time	1.00	ns
$t_{\text{TMDHD}}$	Test Mode Select Hold Time	2.00	ns
$t_{\text{TCK2Q}}$	Clock to Q (data out)	8.00	ns
$t_{\text{RSTB2Q}}$	Reset to Q (data out)	25.00	ns
$F_{\text{TCKMAX}}$	TCK Maximum Frequency	15	MHz
$t_{\text{TRSTREM}}$	ResetB Removal Time	0.58	ns
$t_{\text{TRSTREC}}$	ResetB Recovery Time	0.00	ns
$t_{\text{TRSTMPW}}$	ResetB Minimum Pulse	TBD	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-199 • JTAG 1532**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{\text{DISU}}$	Test Data Input Setup Time	1.50	ns
$t_{\text{DIHD}}$	Test Data Input Hold Time	3.00	ns
$t_{\text{TMSU}}$	Test Mode Select Setup Time	1.50	ns
$t_{\text{TMDHD}}$	Test Mode Select Hold Time	3.00	ns
$t_{\text{TCK2Q}}$	Clock to Q (data out)	11.00	ns
$t_{\text{RSTB2Q}}$	Reset to Q (data out)	30.00	ns
$F_{\text{TCKMAX}}$	TCK Maximum Frequency	9.00	MHz
$t_{\text{TRSTREM}}$	ResetB Removal Time	1.18	ns
$t_{\text{TRSTREC}}$	ResetB Recovery Time	0.00	ns
$t_{\text{TRSTMPW}}$	ResetB Minimum Pulse	TBD	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

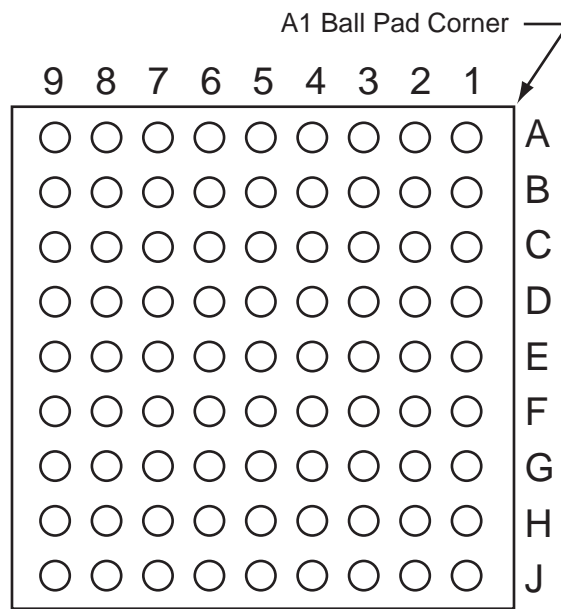
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## 3 – Package Pin Assignments

### 81-Pin $\mu$ CSP



*Note:* This is the bottom view of the package.

#### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

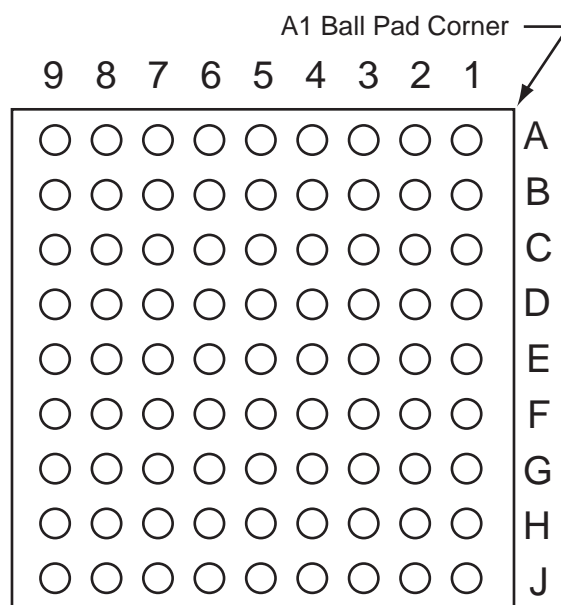
81-Pin $\mu$ CSP	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

81-Pin $\mu$ CSP	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

81-Pin $\mu$ CSP	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP



## 81-Pin CSP



*Note:* This is the bottom view of the package.

### Note

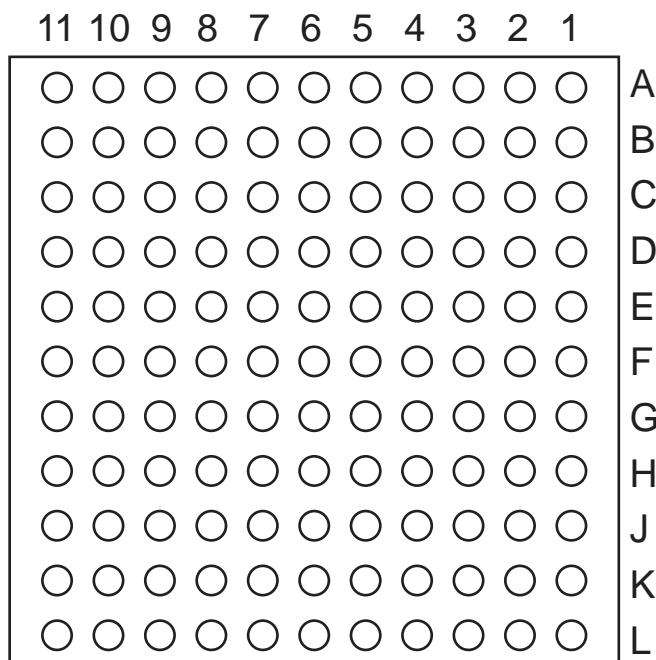
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81-Pin CSP	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

81-Pin CSP	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

81-Pin CSP	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

## 121-Pin CSP



*Note:* This is the bottom view of the package.

### Note

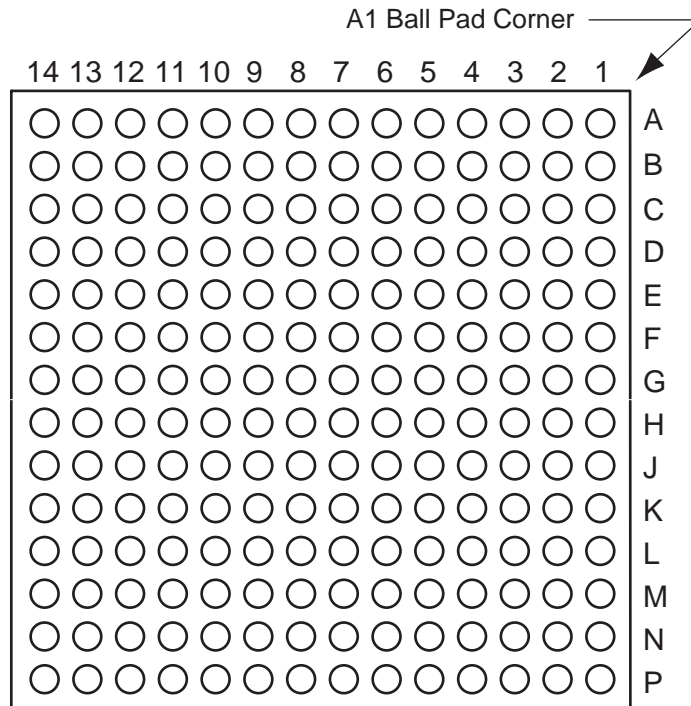
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

121-Pin CSP		121-Pin CSP		121-Pin CSP	
Pin Number	AGL060 Function	Pin Number	AGL060 Function	Pin Number	AGL060 Function
A1	GNDQ	D4	IO10RSB0	G7	VCC
A2	IO01RSB0	D5	IO11RSB0	G8	GDC0/IO46RSB0
A3	GAA1/IO03RSB0	D6	IO18RSB0	G9	GDA1/IO49RSB0
A4	GAC1/IO07RSB0	D7	IO32RSB0	G10	GDB0/IO48RSB0
A5	IO15RSB0	D8	IO31RSB0	G11	GCA0/IO40RSB0
A6	IO13RSB0	D9	GCA2/IO41RSB0	H1	IO75RSB1
A7	IO17RSB0	D10	IO30RSB0	H2	IO76RSB1
A8	GBB1/IO22RSB0	D11	IO33RSB0	H3	GFC2/IO78RSB1
A9	GBA1/IO24RSB0	E1	IO87RSB1	H4	GFA2/IO80RSB1
A10	GNDQ	E2	GFC0/IO85RSB1	H5	IO77RSB1
A11	VMV0	E3	IO92RSB1	H6	GEC2/IO66RSB1
B1	GAA2/IO95RSB1	E4	IO94RSB1	H7	IO54RSB1
B2	IO00RSB0	E5	VCC	H8	GDC2/IO53RSB1
B3	GAA0/IO02RSB0	E6	VCCIB0	H9	VJTAG
B4	GAC0/IO06RSB0	E7	GND	H10	TRST
B5	IO08RSB0	E8	GCC0/IO36RSB0	H11	IO44RSB0
B6	IO12RSB0	E9	IO34RSB0	J1	GEC1/IO74RSB1
B7	IO16RSB0	E10	GCB1/IO37RSB0	J2	GEC0/IO73RSB1
B8	GBC1/IO20RSB0	E11	GCC1/IO35RSB0	J3	GEB1/IO72RSB1
B9	GBB0/IO21RSB0	F1*	VCOMPLF	J4	GEA0/IO69RSB1
B10	GBB2/IO27RSB0	F2	GFB0/IO83RSB1	J5	FF/GEB2/IO67RSB1
B11	GBA2/IO25RSB0	F3	GFA0/IO82RSB1	J6	IO62RSB1
C1	IO89RSB1	F4	GFC1/IO86RSB1	J7	GDA2/IO51RSB1
C2	GAC2/IO91RSB1	F5	VCCIB1	J8	GDB2/IO52RSB1
C3	GAB1/IO05RSB0	F6	VCC	J9	TDI
C4	GAB0/IO04RSB0	F7	VCCIB0	J10	TDO
C5	IO09RSB0	F8	GCB2/IO42RSB0	J11	GDC1/IO45RSB0
C6	IO14RSB0	F9	GCC2/IO43RSB0	K1	GEB0/IO71RSB1
C7	GBA0/IO23RSB0	F10	GCB0/IO38RSB0	K2	GEA1/IO70RSB1
C8	GBC0/IO19RSB0	F11	GCA1/IO39RSB0	K3	GEA2/IO68RSB1
C9	IO26RSB0	G1*	VCCPLF	K4	IO64RSB1
C10	IO28RSB0	G2	GFB2/IO79RSB1	K5	IO60RSB1
C11	GBC2/IO29RSB0	G3	GFA1/IO81RSB1	K6	IO59RSB1
D1	IO88RSB1	G4	GFB1/IO84RSB1	K7	IO56RSB1
D2	IO90RSB1	G5	GND	K8	TCK
D3	GAB2/IO93RSB1	G6	VCCIB1	K9	TMS

\* Pin numbers F1 and G1 must be connected to ground because a PLL is not supported for AGL060-CS/G121.

121-Pin CSP	
Pin Number	AGL060 Function
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1

## 196-Pin CSP



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL125 Function	Pin Number	AGL125 Function	Pin Number	AGL125 Function
A1	GND	C9	IO23RSB0	F3	IO113RSB1
A2	GAA0/IO00RSB0	C10	IO29RSB0	F4	IO112RSB1
A3	GAC0/IO04RSB0	C11	VCCIB0	F5	IO111RSB1
A4	GAC1/IO05RSB0	C12	IO42RSB0	F6	NC
A5	IO09RSB0	C13	GNDQ	F7	VCC
A6	IO15RSB0	C14	IO44RSB0	F8	VCC
A7	IO18RSB0	D1	IO127RSB1	F9	NC
A8	IO22RSB0	D2	IO129RSB1	F10	IO07RSB0
A9	IO27RSB0	D3	GAA2/IO132RSB1	F11	IO25RSB0
A10	GBC0/IO35RSB0	D4	IO126RSB1	F12	IO10RSB0
A11	GBB0/IO37RSB0	D5	IO06RSB0	F13	IO33RSB0
A12	GBB1/IO38RSB0	D6	IO13RSB0	F14	IO47RSB0
A13	GBA1/IO40RSB0	D7	IO19RSB0	G1	GFB1/IO121RSB1
A14	GND	D8	IO21RSB0	G2	GFA0/IO119RSB1
B1	VCCIB1	D9	IO26RSB0	G3	GFA2/IO117RSB1
B2	VMV0	D10	IO31RSB0	G4	VCOMPLF
B3	GAA1/IO01RSB0	D11	IO30RSB0	G5	GFC0/IO122RSB1
B4	GAB1/IO03RSB0	D12	VMV0	G6	VCC
B5	GND	D13	IO46RSB0	G7	GND
B6	IO16RSB0	D14	GBC2/IO45RSB0	G8	GND
B7	IO20RSB0	E1	IO125RSB1	G9	VCC
B8	IO24RSB0	E2	GND	G10	GCC0/IO52RSB0
B9	IO28RSB0	E3	IO131RSB1	G11	GCB1/IO53RSB0
B10	GND	E4	VCCIB1	G12	GCA0/IO56RSB0
B11	GBC1/IO36RSB0	E5	NC	G13	IO48RSB0
B12	GBA0/IO39RSB0	E6	IO08RSB0	G14	GCC2/IO59RSB0
B13	GBA2/IO41RSB0	E7	IO17RSB0	H1	GFB0/IO120RSB1
B14	GBB2/IO43RSB0	E8	IO12RSB0	H2	GFA1/IO118RSB1
C1	GAC2/IO128RSB1	E9	IO11RSB0	H3	VCCPLF
C2	GAB2/IO130RSB1	E10	NC	H4	GFB2/IO116RSB1
C3	GNDQ	E11	VCCIB0	H5	GFC1/IO123RSB1
C4	VCCIB0	E12	IO32RSB0	H6	VCC
C5	GAB0/IO02RSB0	E13	GND	H7	GND
C6	IO14RSB0	E14	IO34RSB0	H8	GND
C7	VCCIB0	F1	IO124RSB1	H9	VCC
C8	NC	F2	IO114RSB1	H10	GCC1/IO51RSB0

196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL125 Function	Pin Number	AGL125 Function	Pin Number	AGL125 Function
H11	GCB0/IO54RSB0	L5	IO91RSB1	N13	GNDQ
H12	GCA1/IO55RSB0	L6	IO90RSB1	N14	TDO
H13	IO49RSB0	L7	IO83RSB1	P1	GND
H14	GCA2/IO57RSB0	L8	IO81RSB1	P2	GEA2/IO103RSB1
J1	GFC2/IO115RSB1	L9	IO71RSB1	P3	FF/GEB2/IO102RSB1
J2	IO110RSB1	L10	IO70RSB1	P4	IO98RSB1
J3	IO94RSB1	L11	VPUMP	P5	IO97RSB1
J4	IO93RSB1	L12	VJTAG	P6	IO85RSB1
J5	IO89RSB1	L13	GDA0/IO66RSB0	P7	IO84RSB1
J6	NC	L14	GDB0/IO64RSB0	P8	IO79RSB1
J7	VCC	M1	GEB0/IO106RSB1	P9	IO77RSB1
J8	VCC	M2	GEA1/IO105RSB1	P10	IO75RSB1
J9	NC	M3	GNDQ	P11	GDC2/IO69RSB1
J10	IO60RSB0	M4	VCCIB1	P12	GDA2/IO67RSB1
J11	GCB2/IO58RSB0	M5	IO92RSB1	P13	TMS
J12	IO50RSB0	M6	IO88RSB1	P14	GND
J13	GDC1/IO61RSB0	M7	NC		
J14	GDC0/IO62RSB0	M8	VCCIB1		
K1	IO99RSB1	M9	IO76RSB1		
K2	GND	M10	GDB2/IO68RSB1		
K3	IO95RSB1	M11	VCCIB1		
K4	VCCIB1	M12	VMV1		
K5	NC	M13	TRST		
K6	IO86RSB1	M14	VCCIB0		
K7	IO80RSB1	N1	GEA0/IO104RSB1		
K8	IO74RSB1	N2	VMV1		
K9	IO72RSB1	N3	GEC2/IO101RSB1		
K10	NC	N4	IO100RSB1		
K11	VCCIB0	N5	GND		
K12	GDA1/IO65RSB0	N6	IO87RSB1		
K13	GND	N7	IO82RSB1		
K14	GDB1/IO63RSB0	N8	IO78RSB1		
L1	GEB1/IO107RSB1	N9	IO73RSB1		
L2	GEC1/IO109RSB1	N10	GND		
L3	GEC0/IO108RSB1	N11	TCK		
L4	IO96RSB1	N12	TDI		



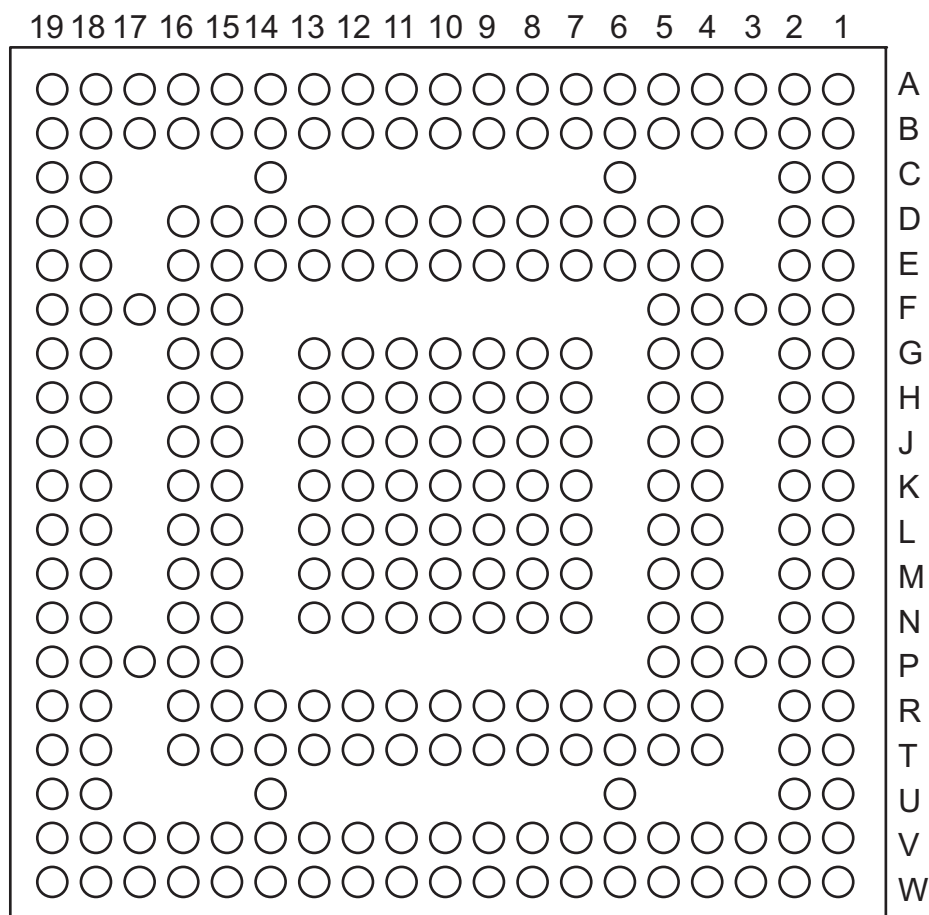
196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
A1	GND	C9	IO30RSB0	F3	IO111PDB3
A2	GAA0/IO00RSB0	C10	IO33RSB0	F4	IO111NDB3
A3	GAC0/IO04RSB0	C11	VCCIB0	F5	IO113NPB3
A4	GAC1/IO05RSB0	C12	IO41NPB1	F6	IO06RSB0
A5	IO10RSB0	C13	GNDQ	F7	VCC
A6	IO13RSB0	C14	IO42NDB1	F8	VCC
A7	IO17RSB0	D1	IO116VDB3	F9	IO28RSB0
A8	IO19RSB0	D2	IO117VDB3	F10	IO54PDB1
A9	IO23RSB0	D3	GAA2/IO118UDB3	F11	IO54NDB1
A10	GBC0/IO35RSB0	D4	IO113PPB3	F12	IO47NDB1
A11	GBB0/IO37RSB0	D5	IO08RSB0	F13	IO47PDB1
A12	GBB1/IO38RSB0	D6	IO14RSB0	F14	IO45NDB1
A13	GBA1/IO40RSB0	D7	IO15RSB0	G1	GFB1/IO109PDB3
A14	GND	D8	IO18RSB0	G2	GFA0/IO108NDB3
B1	VCCIB3	D9	IO25RSB0	G3	GFA2/IO107PPB3
B2	VMV0	D10	IO32RSB0	G4	VCOMPLF
B3	GAA1/IO01RSB0	D11	IO44PPB1	G5	GFC0/IO110NDB3
B4	GAB1/IO03RSB0	D12	VMV1	G6	VCC
B5	GND	D13	IO43NDB1	G7	GND
B6	IO12RSB0	D14	GBC2/IO43PDB1	G8	GND
B7	IO16RSB0	E1	IO112PDB3	G9	VCC
B8	IO22RSB0	E2	GND	G10	GCC0/IO48NDB1
B9	IO24RSB0	E3	IO118VDB3	G11	GCB1/IO49PDB1
B10	GND	E4	VCCIB3	G12	GCA0/IO50NDB1
B11	GBC1/IO36RSB0	E5	IO114USB3	G13	IO53NDB1
B12	GBA0/IO39RSB0	E6	IO07RSB0	G14	GCC2/IO53PDB1
B13	GBA2/IO41PPB1	E7	IO09RSB0	H1	GFB0/IO109NDB3
B14	GBB2/IO42PDB1	E8	IO21RSB0	H2	GFA1/IO108PDB3
C1	GAC2/IO116UDB3	E9	IO31RSB0	H3	VCCPLF
C2	GAB2/IO117UDB3	E10	IO34RSB0	H4	GFB2/IO106PPB3
C3	GNDQ	E11	VCCIB1	H5	GFC1/IO110PDB3
C4	VCCIB0	E12	IO44NPB1	H6	VCC
C5	GAB0/IO02RSB0	E13	GND	H7	GND
C6	IO11RSB0	E14	IO45PDB1	H8	GND
C7	VCCIB0	F1	IO112NDB3	H9	VCC
C8	IO20RSB0	F2	IO107NPB3	H10	GCC1/IO48PDB1

196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
H11	GCB0/IO49NDB1	L5	IO89RSB2	N13	GNDQ
H12	GCA1/IO50PDB1	L6	IO92RSB2	N14	TDO
H13	IO51NDB1	L7	IO75RSB2	P1	GND
H14	GCA2/IO51PDB1	L8	IO66RSB2	P2	GEA2/IO97RSB2
J1	GFC2/IO105PDB3	L9	IO65RSB2	P3	GEB2/IO96RSB2
J2	IO104PPB3	L10	IO71RSB2	P4	IO90RSB2
J3	IO106NPB3	L11	VPUMP	P5	IO85RSB2
J4	IO103PDB3	L12	VJTAG	P6	IO83RSB2
J5	IO103NDB3	L13	GDA0/IO60VPB1	P7	IO79RSB2
J6	IO80RSB2	L14	GDB0/IO59VDB1	P8	IO76RSB2
J7	VCC	M1	GEB0/IO99NDB3	P9	IO72RSB2
J8	VCC	M2	GEA1/IO98PPB3	P10	IO68RSB2
J9	IO64RSB2	M3	GNDQ	P11	GDC2/IO63RSB2
J10	IO56PDB1	M4	VCCIB2	P12	GDA2/IO61RSB2
J11	GCB2/IO52PDB1	M5	IO88RSB2	P13	TMS
J12	IO52NDB1	M6	IO87RSB2	P14	GND
J13	GDC1/IO58UDB1	M7	IO82RSB2		
J14	GDC0/IO58VDB1	M8	VCCIB2		
K1	IO105NDB3	M9	IO67RSB2		
K2	GND	M10	GDB2/IO62RSB2		
K3	IO104NPB3	M11	VCCIB2		
K4	VCCIB3	M12	VMV2		
K5	IO101PPB3	M13	TRST		
K6	IO91RSB2	M14	VCCIB1		
K7	IO81RSB2	N1	GEA0/IO98NPB3		
K8	IO73RSB2	N2	VMV3		
K9	IO77RSB2	N3	GEC2/IO95RSB2		
K10	IO56NDB1	N4	IO94RSB2		
K11	VCCIB1	N5	GND		
K12	GDA1/IO60UPB1	N6	IO86RSB2		
K13	GND	N7	IO78RSB2		
K14	GDB1/IO59UDB1	N8	IO74RSB2		
L1	GEB1/IO99PDB3	N9	IO69RSB2		
L2	GEC1/IO100PDB3	N10	GND		
L3	GEC0/IO100NDB3	N11	TCK		
L4	IO101NPB3	N12	TDI		

196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GND	C8	IO31RSB0	F2	IO144NPB3
A2	GAA0/IO00RSB0	C9	IO44RSB0	F3	IO148PDB3
A3	GAC0/IO04RSB0	C10	IO49RSB0	F4	IO148NDB3
A4	GAC1/IO05RSB0	C11	VCCIB0	F5	IO150NPB3
A5	IO14RSB0	C12	IO60NPB1	F6	IO07RSB0
A6	IO18RSB0	C13	GNDQ	F7	VCC
A7	IO26RSB0	C14	IO61NDB1	F8	VCC
A8	IO29RSB0	D1	IO153VDB3	F9	IO43RSB0
A9	IO36RSB0	D2	IO154VDB3	F10	IO73PDB1
A10	GBC0/IO54RSB0	D3	GAA2/IO155UDB3	F11	IO73NDB1
A11	GBB0/IO56RSB0	D4	IO150PPB3	F12	IO66NDB1
A12	GBB1/IO57RSB0	D5	IO11RSB0	F13	IO66PDB1
A13	GBA1/IO59RSB0	D6	IO20RSB0	F14	IO64NDB1
A14	GND	D7	IO23RSB0	G1	GFB1/IO146PDB3
B1	VCCIB3	D8	IO28RSB0	G2	GFA0/IO145NDB3
B2	VMV0	D9	IO41RSB0	G3	GFA2/IO144PPB3
B2	VMV0	D10	IO47RSB0	G4	VCOMPLF
B3	GAA1/IO01RSB0	D11	IO63PPB1	G5	GFC0/IO147NDB3
B4	GAB1/IO03RSB0	D12	VMV1	G6	VCC
B5	GND	D13	IO62NDB1	G7	GND
B6	IO17RSB0	D14	GBC2/IO62PDB1	G8	GND
B7	IO25RSB0	E1	IO149PDB3	G9	VCC
B8	IO34RSB0	E2	GND	G10	GCC0/IO67NDB1
B9	IO39RSB0	E3	IO155VDB3	G11	GCB1/IO68PDB1
B10	GND	E4	VCCIB3	G12	GCA0/IO69NDB1
B11	GBC1/IO55RSB0	E5	IO151USB3	G13	IO72NDB1
B12	GBA0/IO58RSB0	E6	IO09RSB0	G14	GCC2/IO72PDB1
B13	GBA2/IO60PPB1	E7	IO12RSB0	H1	GFB0/IO146NDB3
B14	GBB2/IO61PDB1	E8	IO32RSB0	H2	GFA1/IO145PDB3
C1	GAC2/IO153UDB3	E9	IO46RSB0	H3	VCCPLF
C2	GAB2/IO154UDB3	E10	IO51RSB0	H4	GFB2/IO143PPB3
C3	GNDQ	E11	VCCIB1	H5	GFC1/IO147PDB3
C4	VCCIB0	E12	IO63NPB1	H6	VCC
C5	GAB0/IO02RSB0	E13	GND	H7	GND
C6	IO15RSB0	E14	IO64PDB1	H8	GND
C7	VCCIB0	F1	IO149NDB3	H9	VCC

196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
H10	GCC1/IO67PDB1	L4	IO138NPB3	N11	TCK
H11	GCB0/IO68NDB1	L5	IO122RSB2	N12	TDI
H12	GCA1/IO69PDB1	L6	IO128RSB2	N13	GNDQ
H13	IO70NDB1	L7	IO101RSB2	N14	TDO
H14	GCA2/IO70PDB1	L8	IO88RSB2	P1	GND
J1	GFC2/IO142PDB3	L9	IO86RSB2	P2	GEA2/IO134RSB2
J2	IO141PPB3	L10	IO94RSB2	P3	FF/GEB2/IO133RSB2
J3	IO143NPB3	L11	VPUMP	P4	IO123RSB2
J4	IO140PDB3	L12	VJTAG	P5	IO116RSB2
J5	IO140NDB3	L13	GDA0/IO79VPB1	P6	IO114RSB2
J6	IO109RSB2	L14	GDB0/IO78VDB1	P7	IO107RSB2
J7	VCC	M1	GEB0/IO136NDB3	P8	IO103RSB2
J8	VCC	M2	GEA1/IO135PPB3	P9	IO95RSB2
J9	IO84RSB2	M3	GNDQ	P10	IO91RSB2
J10	IO75PDB1	M4	VCCIB2	P11	GDC2/IO82RSB2
J11	GCB2/IO71PDB1	M5	IO120RSB2	P12	GDA2/IO80RSB2
J12	IO71NDB1	M6	IO119RSB2	P13	TMS
J13	GDC1/IO77UDB1	M7	IO112RSB2	P14	GND
J14	GDC0/IO77VDB1	M8	VCCIB2		
K1	IO142NDB3	M9	IO89RSB2		
K2	GND	M10	GDB2/IO81RSB2		
K3	IO141NPB3	M11	VCCIB2		
K4	VCCIB3	M12	VMV2		
K5	IO138PPB3	M12	VMV2		
K6	IO125RSB2	M13	TRST		
K7	IO110RSB2	M14	VCCIB1		
K8	IO98RSB2	N1	GEA0/IO135NPB3		
K9	IO104RSB2	N2	VMV3		
K10	IO75NDB1	N3	GEC2/IO132RSB2		
K11	VCCIB1	N4	IO130RSB2		
K12	GDA1/IO79UPB1	N5	GND		
K13	GND	N6	IO117RSB2		
K14	GDB1/IO78UDB1	N7	IO106RSB2		
L1	GEB1/IO136PDB3	N8	IO100RSB2		
L2	GEC1/IO137PDB3	N9	IO92RSB2		
L3	GEC0/IO137NDB3	N10	GND		

## 281-Pin CSP



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
A1	GND	B18	VCCIB1	E13	IO46RSB0
A2	GAB0/IO02RSB0	B19	IO61NDB1	E14	GBB1/IO57RSB0
A3	GAC1/IO05RSB0	C1	GAB2/IO173PPB3	E15	IO62NPB1
A4	IO07RSB0	C2	IO174NPB3	E16	IO63PPB1
A5	IO10RSB0	C6	IO12RSB0	E18	IO64PPB1
A6	IO14RSB0	C14	IO50RSB0	E19	IO65NPB1
A7	IO18RSB0	C18	IO60NPB1	F1	IO168NPB3
A8	IO21RSB0	C19	GBB2/IO61PDB1	F2	GND
A9	IO22RSB0	D1	IO170PPB3	F3	IO169PPB3
A10	VCCIB0	D2	IO172NPB3	F4	IO170NPB3
A11	IO33RSB0	D4	GAA0/IO00RSB0	F5	IO173NPB3
A12	IO40RSB0	D5	GAA1/IO01RSB0	F15	IO63NPB1
A13	IO37RSB0	D6	IO09RSB0	F16	IO65PPB1
A14	IO48RSB0	D7	IO16RSB0	F17	IO64NPB1
A15	IO51RSB0	D8	IO19RSB0	F18	GND
A16	IO53RSB0	D9	IO26RSB0	F19	IO68PPB1
A17	GBC1/IO55RSB0	D10	GND	G1	IO167NPB3
A18	GBA0/IO58RSB0	D11	IO34RSB0	G2	IO165NDB3
A19	GND	D12	IO45RSB0	G4	IO168PPB3
B1	GAA2/IO174PPB3	D13	IO49RSB0	G5	IO167PPB3
B2	VCCIB0	D14	IO47RSB0	G7	GAC2/IO172PPB3
B3	GAB1/IO03RSB0	D15	GBB0/IO56RSB0	G8	VCCIB0
B4	GAC0/IO04RSB0	D16	GBA2/IO60PPB1	G9	IO28RSB0
B5	IO06RSB0	D18	GBC2/IO62PPB1	G10	IO32RSB0
B6	GND	D19	IO66NPB1	G11	IO43RSB0
B7	IO15RSB0	E1	IO169NPB3	G12	VCCIB0
B8	IO20RSB0	E2	IO171PPB3	G13	IO66PPB1
B9	IO23RSB0	E4	IO171NPB3	G15	IO67NDB1
B10	IO24RSB0	E5	IO08RSB0	G16	IO67PDB1
B11	IO36RSB0	E6	IO11RSB0	G18	GCC0/IO69NPB1
B12	IO35RSB0	E7	IO13RSB0	G19	GCB1/IO70PPB1
B13	IO44RSB0	E8	IO17RSB0	H1	GFB0/IO163NPB3
B14	GND	E9	IO25RSB0	H2	IO165PDB3
B15	IO52RSB0	E10	IO30RSB0	H4	GFC1/IO164PPB3
B16	GBC0/IO54RSB0	E11	IO41RSB0	H5	GFB1/IO163PPB3
B17	GBA1/IO59RSB0	E12	IO42RSB0	H7	VCCIB3

281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
H8	VCC	K15	IO73NPB1	N4	IO150PPB3
H9	VCCIB0	K16	GND	N5	IO148NPB3
H10	VCC	K18	IO74NPB1	N7	GEA2/IO143RSB2
H11	VCCIB0	K19	VCCIB1	N8	VCCIB2
H12	VCC	L1	GFB2/IO160PDB3	N9	IO117RSB2
H13	VCCIB1	L2	IO160NDB3	N10	IO115RSB2
H15	IO68NPB1	L4	GFC2/IO159PPB3	N11	IO114RSB2
H16	GCB0/IO70NPB1	L5	IO153PPB3	N12	VCCIB2
H18	GCA1/IO71PPB1	L7	IO153NPB3	N13	VPUMP
H19	GCA2/IO72PPB1	L8	VCCIB3	N15	IO82PPB1
J1	VCOMPLF	L9	GND	N16	IO85PPB1
J2	GFA0/IO162NDB3	L10	GND	N18	IO82NPB1
J4	VCCPLF	L11	GND	N19	IO81PPB1
J5	GFC0/IO164NPB3	L12	VCCIB1	P1	IO151PDB3
J7	GFA2/IO161PDB3	L13	IO76PPB1	P2	GND
J8	VCCIB3	L15	IO76NPB1	P3	IO151NDB3
J9	GND	L16	IO77PPB1	P4	IO149PPB3
J10	GND	L18	IO78NPB1	P5	GEA0/IO144NPB3
J11	GND	L19	IO77NPB1	P15	IO83NDB1
J12	VCCIB1	M1	IO158PDB3	P16	IO83PDB1
J13	GCC1/IO69PPB1	M2	IO158NDB3	P17	GDC1/IO86PPB1
J15	GCA0/IO71NPB1	M4	IO154NPB3	P18	GND
J16	GCB2/IO73PPB1	M5	IO152PPB3	P19	IO85NPB1
J18	IO72NPB1	M7	VCCIB3	R1	IO150NPB3
J19	IO75PSB1	M8	VCC	R2	IO149NPB3
K1	VCCIB3	M9	VCCIB2	R4	GEC1/IO146PPB3
K2	GFA1/IO162PDB3	M10	VCC	R5	GEB1/IO145PPB3
K4	GND	M11	VCCIB2	R6	IO138RSB2
K5	IO159NPB3	M12	VCC	R7	IO127RSB2
K7	IO161NDB3	M13	VCCIB1	R8	IO123RSB2
K8	VCC	M15	IO79NPB1	R9	IO118RSB2
K9	GND	M16	IO81NPB1	R10	IO111RSB2
K10	GND	M18	IO79PPB1	R11	IO106RSB2
K11	GND	M19	IO78PPB1	R12	IO103RSB2
K12	VCC	N1	IO154PPB3	R13	IO97RSB2
K13	GCC2/IO74PPB1	N2	IO152NPB3	R14	IO95RSB2

281-Pin CSP		281-Pin CSP	
Pin Number	AGL600 Function	Pin Number	AGL600 Function
R15	IO94RSB2	V10	IO112RSB2
R16	GDA1/IO88PPB1	V11	IO110RSB2
R18	GDB0/IO87NPB1	V12	IO108RSB2
R19	GDC0/IO86NPB1	V13	IO102RSB2
T1	IO148PPB3	V14	GND
T2	GEC0/IO146NPB3	V15	IO93RSB2
T4	GEB0/IO145NPB3	V16	GDA2/IO89RSB2
T5	IO132RSB2	V17	TDI
T6	IO136RSB2	V18	VCCIB2
T7	IO130RSB2	V19	TDO
T8	IO126RSB2	W1	GND
T9	IO120RSB2	W2	FF/GEB2/IO142RSB2
T10	GND	W3	IO139RSB2
T11	IO113RSB2	W4	IO137RSB2
T12	IO104RSB2	W5	IO134RSB2
T13	IO101RSB2	W6	IO133RSB2
T14	IO98RSB2	W7	IO128RSB2
T15	GDC2/IO91RSB2	W8	IO124RSB2
T16	TMS	W9	IO119RSB2
T18	VJTAG	W10	VCCIB2
T19	GDB1/IO87PPB1	W11	IO109RSB2
U1	IO147PDB3	W12	IO107RSB2
U2	GEA1/IO144PPB3	W13	IO105RSB2
U6	IO131RSB2	W14	IO100RSB2
U14	IO99RSB2	W15	IO96RSB2
U18	TRST	W16	IO92RSB2
U19	GDA0/IO88NPB1	W17	GDB2/IO90RSB2
V1	IO147NDB3	W18	TCK
V2	VCCIB3	W19	GND
V3	GEC2/IO141RSB2		
V4	IO140RSB2		
V5	IO135RSB2		
V6	GND		
V7	IO125RSB2		
V8	IO122RSB2		
V9	IO116RSB2		

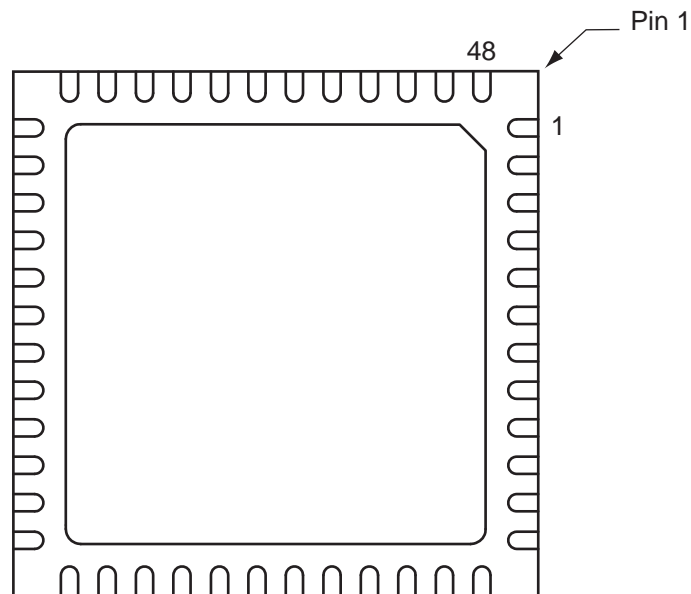


281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
A1	GND	B18	VCCIB1	E13	IO53RSB0
A2	GAB0/IO02RSB0	B19	IO79NDB1	E14	GBB1/IO75RSB0
A3	GAC1/IO05RSB0	C1	GAB2/IO224PPB3	E15	IO80NPB1
A4	IO13RSB0	C2	IO225NPB3	E16	IO85PPB1
A5	IO11RSB0	C6	IO18RSB0	E18	IO83PPB1
A6	IO16RSB0	C14	IO63RSB0	E19	IO84NPB1
A7	IO20RSB0	C18	IO78NPB1	F1	IO214NPB3
A8	IO24RSB0	C19	GBB2/IO79PDB1	F2	GND
A9	IO29RSB0	D1	IO219PPB3	F3	IO217PPB3
A10	VCCIB0	D2	IO223NPB3	F4	IO219NPB3
A11	IO39RSB0	D4	GAA0/IO00RSB0	F5	IO224NPB3
A12	IO45RSB0	D5	GAA1/IO01RSB0	F15	IO85NPB1
A13	IO48RSB0	D6	IO15RSB0	F16	IO84PPB1
A14	IO58RSB0	D7	IO19RSB0	F17	IO83NPB1
A15	IO61RSB0	D8	IO27RSB0	F18	GND
A16	IO62RSB0	D9	IO32RSB0	F19	IO90PPB1
A17	GBC1/IO73RSB0	D10	GND	G1	IO212NPB3
A18	GBA0/IO76RSB0	D11	IO38RSB0	G2	IO211NDB3
A19	GND	D12	IO44RSB0	G4	IO214PPB3
B1	GAA2/IO225PPB3	D13	IO47RSB0	G5	IO212PPB3
B2	VCCIB0	D14	IO60RSB0	G7	GAC2/IO223PPB3
B3	GAB1/IO03RSB0	D15	GBB0/IO74RSB0	G8	VCCIB0
B4	GAC0/IO04RSB0	D16	GBA2/IO78PPB1	G9	IO30RSB0
B5	IO12RSB0	D18	GBC2/IO80PPB1	G10	IO37RSB0
B6	GND	D19	IO88NPB1	G11	IO43RSB0
B7	IO21RSB0	E1	IO217NPB3	G12	VCCIB0
B8	IO26RSB0	E2	IO221PPB3	G13	IO88PPB1
B9	IO34RSB0	E4	IO221NPB3	G15	IO89NDB1
B10	IO35RSB0	E5	IO10RSB0	G16	IO89PDB1
B11	IO36RSB0	E6	IO14RSB0	G18	GCC0/IO91NPB1
B12	IO46RSB0	E7	IO25RSB0	G19	GCB1/IO92PPB1
B13	IO52RSB0	E8	IO28RSB0	H1	GFB0/IO208NPB3
B14	GND	E9	IO31RSB0	H2	IO211PDB3
B15	IO59RSB0	E10	IO33RSB0	H4	GFC1/IO209PPB3
B16	GBC0/IO72RSB0	E11	IO42RSB0	H5	GFB1/IO208PPB3
B17	GBA1/IO77RSB0	E12	IO49RSB0	H7	VCCIB3

281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
H8	VCC	K15	IO95NPB1	N4	IO196PPB3
H9	VCCIB0	K16	GND	N5	IO197NPB3
H10	VCC	K18	IO96NPB1	N7	GEA2/IO187RSB2
H11	VCCIB0	K19	VCCIB1	N8	VCCIB2
H12	VCC	L1	GFB2/IO205PDB3	N9	IO155RSB2
H13	VCCIB1	L2	IO205NDB3	N10	IO154RSB2
H15	IO90NPB1	L4	GFC2/IO204PPB3	N11	IO150RSB2
H16	GCB0/IO92NPB1	L5	IO203PPB3	N12	VCCIB2
H18	GCA1/IO93PPB1	L7	IO203NPB3	N13	VPUMP
H19	GCA2/IO94PPB1	L8	VCCIB3	N15	IO107PPB1
J1	VCOMPLF	L9	GND	N16	IO105PPB1
J2	GFA0/IO207NDB3	L10	GND	N18	IO107NPB1
J4	VCCPLF	L11	GND	N19	IO100PPB1
J5	GFC0/IO209NPB3	L12	VCCIB1	P1	IO195PDB3
J7	GFA2/IO206PDB3	L13	IO103PPB1	P2	GND
J8	VCCIB3	L15	IO103NPB1	P3	IO195NDB3
J9	GND	L16	IO97PPB1	P4	IO194PPB3
J10	GND	L18	IO98NPB1	P5	GEA0/IO188NPB3
J11	GND	L19	IO97NPB1	P15	IO108NDB1
J12	VCCIB1	M1	IO202PDB3	P16	IO108PDB1
J13	GCC1/IO91PPB1	M2	IO202NDB3	P17	GDC1/IO111PPB1
J15	GCA0/IO93NPB1	M4	IO201NPB3	P18	GND
J16	GCB2/IO95PPB1	M5	IO198PPB3	P19	IO105NPB1
J18	IO94NPB1	M7	VCCIB3	R1	IO196NPB3
J19	IO102PSB1	M8	VCC	R2	IO194NPB3
K1	VCCIB3	M9	VCCIB2	R4	GEC1/IO190PPB3
K2	GFA1/IO207PDB3	M10	VCC	R5	GEB1/IO189PPB3
K4	GND	M11	VCCIB2	R6	IO184RSB2
K5	IO204NPB3	M12	VCC	R7	IO173RSB2
K7	IO206NDB3	M13	VCCIB1	R8	IO168RSB2
K8	VCC	M15	IO104NPB1	R9	IO160RSB2
K9	GND	M16	IO100NPB1	R10	IO151RSB2
K10	GND	M18	IO104PPB1	R11	IO141RSB2
K11	GND	M19	IO98PPB1	R12	IO136RSB2
K12	VCC	N1	IO201PPB3	R13	IO127RSB2
K13	GCC2/IO96PPB1	N2	IO198NPB3	R14	IO124RSB2

281-Pin CSP		281-Pin CSP	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
R15	IO122RSB2	V10	IO145RSB2
R16	GDA1/IO113PPB1	V11	IO144RSB2
R18	GDB0/IO112NPB1	V12	IO134RSB2
R19	GDC0/IO111NPB1	V13	IO133RSB2
T1	IO197PPB3	V14	GND
T2	GEC0/IO190NPB3	V15	IO119RSB2
T4	GEB0/IO189NPB3	V16	GDA2/IO114RSB2
T5	IO181RSB2	V17	TDI
T6	IO172RSB2	V18	VCCIB2
T7	IO171RSB2	V19	TDO
T8	IO156RSB2	W1	GND
T9	IO159RSB2	W2	FF/GEB2/IO186RSB2
T10	GND	W3	IO183RSB2
T11	IO139RSB2	W4	IO176RSB2
T12	IO138RSB2	W5	IO170RSB2
T13	IO129RSB2	W6	IO162RSB2
T14	IO123RSB2	W7	IO157RSB2
T15	GDC2/IO116RSB2	W8	IO152RSB2
T16	TMS	W9	IO149RSB2
T18	VJTAG	W10	VCCIB2
T19	GDB1/IO112PPB1	W11	IO140RSB2
U1	IO193PDB3	W12	IO135RSB2
U2	GEA1/IO188PPB3	W13	IO130RSB2
U6	IO167RSB2	W14	IO125RSB2
U14	IO128RSB2	W15	IO120RSB2
U18	TRST	W16	IO118RSB2
U19	GDA0/IO113NPB1	W17	GDB2/IO115RSB2
V1	IO193NDB3	W18	TCK
V2	VCCIB3	W19	GND
V3	GEC2/IO185RSB2		
V4	IO182RSB2		
V5	IO175RSB2		
V6	GND		
V7	IO161RSB2		
V8	IO143RSB2		
V9	IO146RSB2		

## 48-Pin QFN



**Notes:**

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

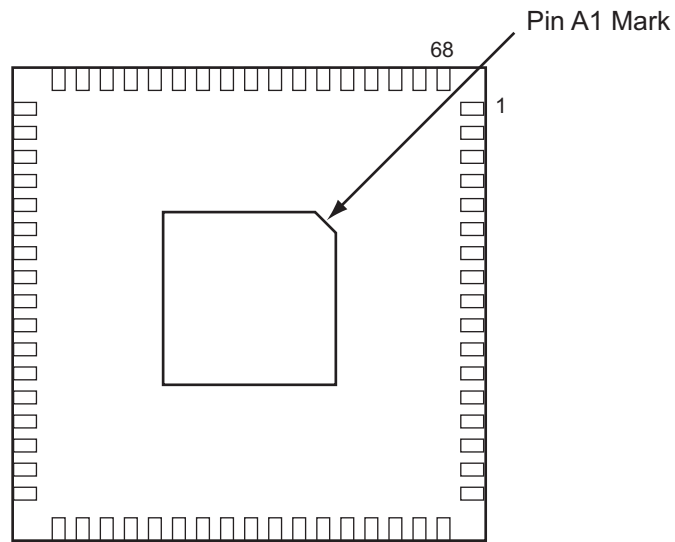
**Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

48-Pin QFP	
Pin Number	AGL030 Function
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	FF/IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0

48-Pin QFP	
Pin Number	AGL030 Function
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

## 68-Pin QFN



*Notes:*

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

**Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

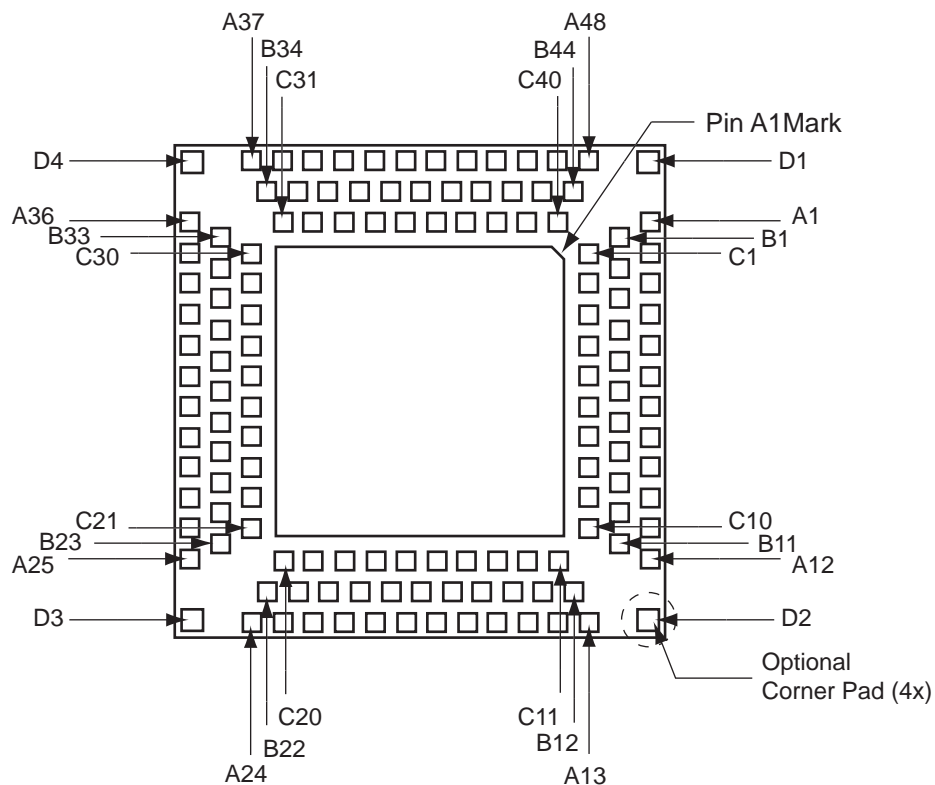
68-Pin QFN	
Pin Number	AGL015 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

68-Pin QFN	
Pin Number	AGL015 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

68-Pin QFN		68-Pin QFN	
Pin Number	AGL030 Function	Pin Number	AGL030 Function
1	IO82RSB1	37	TRST
2	IO80RSB1	38	VJTAG
3	IO78RSB1	39	IO40RSB0
4	IO76RSB1	40	IO37RSB0
5	GEC0/IO73RSB1	41	GDB0/IO34RSB0
6	GEA0/IO72RSB1	42	GDA0/IO33RSB0
7	GEB0/IO71RSB1	43	GDC0/IO32RSB0
8	VCC	44	VCCIB0
9	GND	45	GND
10	VCCIB1	46	VCC
11	IO68RSB1	47	IO31RSB0
12	IO67RSB1	48	IO29RSB0
13	IO66RSB1	49	IO28RSB0
14	IO65RSB1	50	IO27RSB0
15	IO64RSB1	51	IO25RSB0
16	IO63RSB1	52	IO24RSB0
17	IO62RSB1	53	IO22RSB0
18	FF/IO60RSB1	54	IO21RSB0
19	IO58RSB1	55	IO19RSB0
20	IO56RSB1	56	IO17RSB0
21	IO54RSB1	57	IO15RSB0
22	IO52RSB1	58	IO14RSB0
23	IO51RSB1	59	VCCIB0
24	VCC	60	GND
25	GND	61	VCC
26	VCCIB1	62	IO12RSB0
27	IO50RSB1	63	IO10RSB0
28	IO48RSB1	64	IO08RSB0
29	IO46RSB1	65	IO06RSB0
30	IO44RSB1	66	IO04RSB0
31	IO42RSB1	67	IO02RSB0
32	TCK	68	IO00RSB0
33	TDI		
34	TMS		
35	VPUMP		
36	TDO		



## 132-Pin QFN



### Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

132-Pin QFN		132-Pin QFN		132-Pin QFN	
Pin Number	AGL030 Function	Pin Number	AGL030 Function	Pin Number	AGL030 Function
A1	IO80RSB1	A37	IO22RSB0	B25	GND
A2	IO77RSB1	A38	IO19RSB0	B26	NC
A3	NC	A39	NC	B27	IO37RSB0
A4	IO76RSB1	A40	IO18RSB0	B28	GND
A5	GEC0/IO73RSB1	A41	IO16RSB0	B29	GDA0/IO33RSB0
A6	NC	A42	IO14RSB0	B30	NC
A7	GEB0/IO71RSB1	A43	VCC	B31	GND
A8	IO69RSB1	A44	IO11RSB0	B32	IO29RSB0
A9	NC	A45	IO08RSB0	B33	IO26RSB0
A10	VCC	A46	IO06RSB0	B34	IO23RSB0
A11	IO67RSB1	A47	IO05RSB0	B35	IO20RSB0
A12	IO64RSB1	A48	IO02RSB0	B36	GND
A13	IO59RSB1	B1	IO81RSB1	B37	IO17RSB0
A14	IO56RSB1	B2	IO78RSB1	B38	IO15RSB0
A15	NC	B3	GND	B39	GND
A16	IO55RSB1	B4	IO75RSB1	B40	IO12RSB0
A17	IO53RSB1	B5	NC	B41	IO09RSB0
A18	VCC	B6	GND	B42	GND
A19	IO50RSB1	B7	IO70RSB1	B43	IO04RSB0
A20	IO48RSB1	B8	NC	B44	IO01RSB0
A21	IO45RSB1	B9	GND	C1	IO82RSB1
A22	IO44RSB1	B10	IO66RSB1	C2	IO79RSB1
A23	IO43RSB1	B11	IO63RSB1	C3	NC
A24	TDI	B12	FF/IO60RSB1	C4	IO74RSB1
A25	TRST	B13	IO57RSB1	C5	GEA0/IO72RSB1
A26	IO40RSB0	B14	GND	C6	NC
A27	NC	B15	IO54RSB1	C7	NC
A28	IO39RSB0	B16	IO52RSB1	C8	VCCIB1
A29	IO38RSB0	B17	GND	C9	IO65RSB1
A30	IO36RSB0	B18	IO49RSB1	C10	IO62RSB1
A31	IO35RSB0	B19	IO46RSB1	C11	IO61RSB1
A32	GDC0/IO32RSB0	B20	GND	C12	IO58RSB1
A33	NC	B21	IO42RSB1	C13	NC
A34	VCC	B22	TMS	C14	NC
A35	IO30RSB0	B23	TDO	C15	IO51RSB1
A36	IO27RSB0	B24	IO41RSB0	C16	VCCIB1

132-Pin QFN	
Pin Number	AGL030 Function
C17	IO47RSB1
C18	NC
C19	TCK
C20	NC
C21	VPUMP
C22	VJTAG
C23	NC
C24	NC
C25	NC
C26	GDB0/IO34RSB0
C27	NC
C28	VCCIB0
C29	IO28RSB0
C30	IO25RSB0
C31	IO24RSB0
C32	IO21RSB0
C33	NC
C34	NC
C35	VCCIB0
C36	IO13RSB0
C37	IO10RSB0
C38	IO07RSB0
C39	IO03RSB0
C40	IO00RSB0
D1	GND
D2	GND
D3	GND
D4	GND

132-Pin QFN		132-Pin QFN		132-Pin QFN	
Pin Number	AGL060 Function	Pin Number	AGL060 Function	Pin Number	AGL060 Function
A1	GAB2/IO00RSB1	A37	GBB1/IO25RSB0	B25	GND
A2	IO93RSB1	A38	GBC0/IO22RSB0	B26	NC
A3	VCCIB1	A39	VCCIB0	B27	GCB2/IO45RSB0
A4	GFC1/IO89RSB1	A40	IO21RSB0	B28	GND
A5	GFB0/IO86RSB1	A41	IO18RSB0	B29	GCB0/IO41RSB0
A6	VCCPLF	A42	IO15RSB0	B30	GCC1/IO38RSB0
A7	GFA1/IO84RSB1	A43	IO14RSB0	B31	GND
A8	GFC2/IO81RSB1	A44	IO11RSB0	B32	GBB2/IO30RSB0
A9	IO78RSB1	A45	GAB1/IO08RSB0	B33	VMV0
A10	VCC	A46	NC	B34	GBA0/IO26RSB0
A11	GEB1/IO75RSB1	A47	GAB0/IO07RSB0	B35	GBC1/IO23RSB0
A12	GEA0/IO72RSB1	A48	IO04RSB0	B36	GND
A13	GEC2/IO69RSB1	B1	IO01RSB1	B37	IO20RSB0
A14	IO65RSB1	B2	GAC2/IO94RSB1	B38	IO17RSB0
A15	VCC	B3	GND	B39	GND
A16	IO64RSB1	B4	GFC0/IO88RSB1	B40	IO12RSB0
A17	IO63RSB1	B5	VCOMPLF	B41	GAC0/IO09RSB0
A18	IO62RSB1	B6	GND	B42	GND
A19	IO61RSB1	B7	GFB2/IO82RSB1	B43	GAA1/IO06RSB0
A20	IO58RSB1	B8	IO79RSB1	B44	GNDQ
A21	GDB2/IO55RSB1	B9	GND	C1	GAA2/IO02RSB1
A22	NC	B10	GEB0/IO74RSB1	C2	IO95RSB1
A23	GDA2/IO54RSB1	B11	VMV1	C3	VCC
A24	TDI	B12	FF/GEB2/IO70RSB1	C4	GFB1/IO87RSB1
A25	TRST	B13	IO67RSB1	C5	GFA0/IO85RSB1
A26	GDC1/IO48RSB0	B14	GND	C6	GFA2/IO83RSB1
A27	VCC	B15	NC	C7	IO80RSB1
A28	IO47RSB0	B16	NC	C8	VCCIB1
A29	GCC2/IO46RSB0	B17	GND	C9	GEA1/IO73RSB1
A30	GCA2/IO44RSB0	B18	IO59RSB1	C10	GNDQ
A31	GCA0/IO43RSB0	B19	GDC2/IO56RSB1	C11	GEA2/IO71RSB1
A32	GCB1/IO40RSB0	B20	GND	C12	IO68RSB1
A33	IO36RSB0	B21	GNDQ	C13	VCCIB1
A34	VCC	B22	TMS	C14	NC
A35	IO31RSB0	B23	TDO	C15	NC
A36	GBA2/IO28RSB0	B24	GDC0/IO49RSB0	C16	IO60RSB1

132-Pin QFN	
Pin Number	AGL060 Function
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

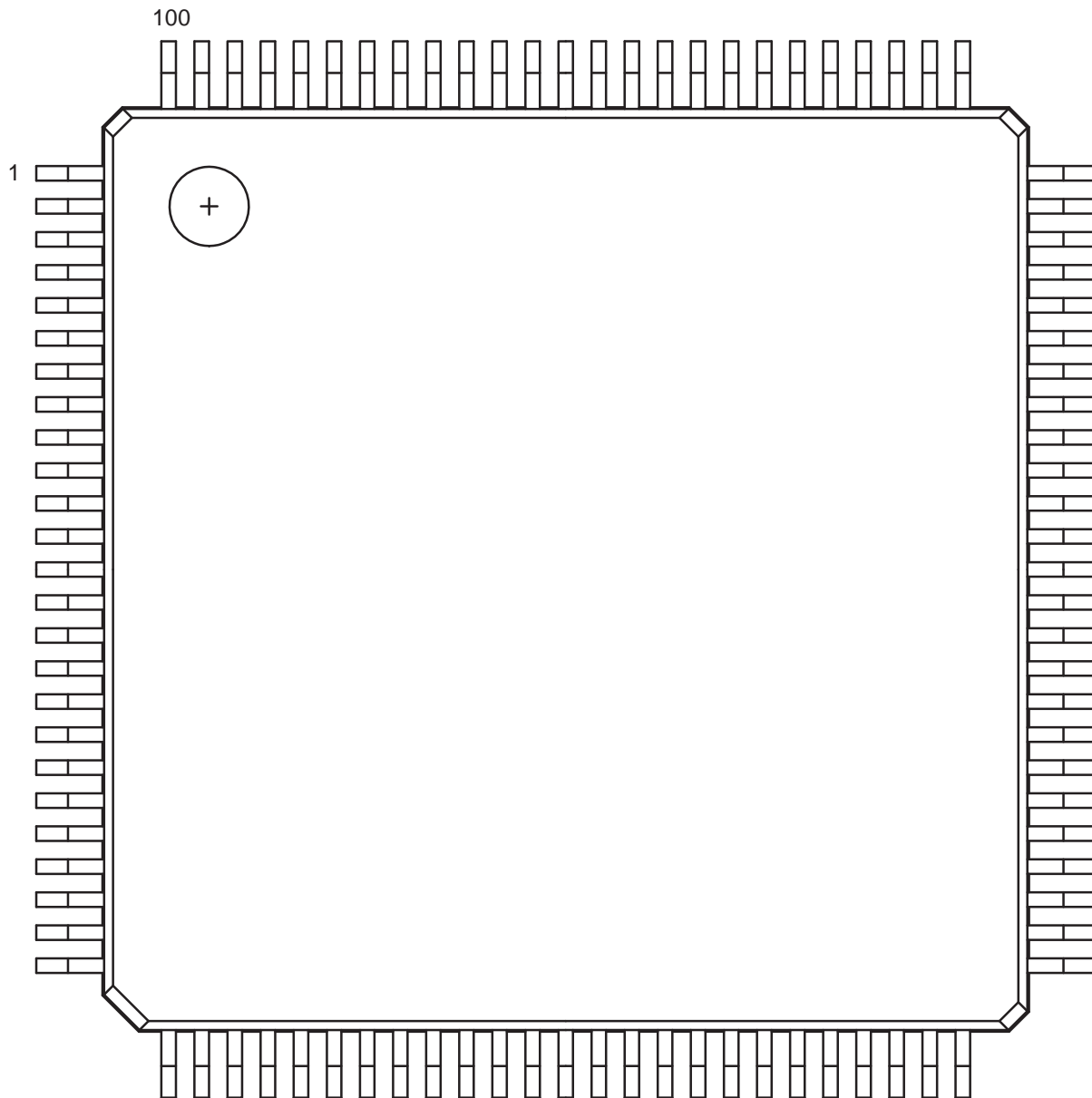
132-Pin QFN	
Pin Number	AGL125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

132-Pin QFN	
Pin Number	AGL125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO

132-Pin QFN	
Pin Number	AGL125 Function
B24	GDC0/IO62RSB0
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1

132-Pin QFN	
Pin Number	AGL125 Function
C16	IO89RSB1
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

## 100-Pin VQFP



*Note:* This is the top view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.



100-Pin VQFP		100-Pin VQFP		100-Pin VQFP	
Pin Number	AGL030 Function	Pin Number	AGL030 Function	Pin Number	AGL030 Function
1	GND	37	VCC	73	IO27RSB0
2	IO82RSB1	38	GND	74	IO26RSB0
3	IO81RSB1	39	VCCIB1	75	IO25RSB0
4	IO80RSB1	40	IO49RSB1	76	IO24RSB0
5	IO79RSB1	41	IO47RSB1	77	IO23RSB0
6	IO78RSB1	42	IO46RSB1	78	IO22RSB0
7	IO77RSB1	43	IO45RSB1	79	IO21RSB0
8	IO76RSB1	44	IO44RSB1	80	IO20RSB0
9	GND	45	IO43RSB1	81	IO19RSB0
10	IO75RSB1	46	IO42RSB1	82	IO18RSB0
11	IO74RSB1	47	TCK	83	IO17RSB0
12	GEC0/IO73RSB1	48	TDI	84	IO16RSB0
13	GEA0/IO72RSB1	49	TMS	85	IO15RSB0
14	GEB0/IO71RSB1	50	NC	86	IO14RSB0
15	IO70RSB1	51	GND	87	VCCIB0
16	IO69RSB1	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB1	54	TDO	90	IO12RSB0
19	IO68RSB1	55	TRST	91	IO10RSB0
20	IO67RSB1	56	VJTAG	92	IO08RSB0
21	IO66RSB1	57	IO41RSB0	93	IO07RSB0
22	IO65RSB1	58	IO40RSB0	94	IO06RSB0
23	IO64RSB1	59	IO39RSB0	95	IO05RSB0
24	IO63RSB1	60	IO38RSB0	96	IO04RSB0
25	IO62RSB1	61	IO37RSB0	97	IO03RSB0
26	IO61RSB1	62	IO36RSB0	98	IO02RSB0
27	FF/IO60RSB1	63	GDB0/IO34RSB0	99	IO01RSB0
28	IO59RSB1	64	GDA0/IO33RSB0	100	IO00RSB0
29	IO58RSB1	65	GDC0/IO32RSB0		
30	IO57RSB1	66	VCCIB0		
31	IO56RSB1	67	GND		
32	IO55RSB1	68	VCC		
33	IO54RSB1	69	IO31RSB0		
34	IO53RSB1	70	IO30RSB0		
35	IO52RSB1	71	IO29RSB0		
36	IO51RSB1	72	IO28RSB0		

100-Pin VQFP		100-Pin VQFP		100-Pin VQFP	
Pin Number	AGL060 Function	Pin Number	AGL060 Function	Pin Number	AGL060 Function
1	GND	37	VCC	73	GBA2/IO25RSB0
2	GAA2/IO51RSB1	38	GND	74	VMV0
3	IO52RSB1	39	VCCIB1	75	GNDQ
4	GAB2/IO53RSB1	40	IO60RSB1	76	GBA1/IO24RSB0
5	IO95RSB1	41	IO59RSB1	77	GBA0/IO23RSB0
6	GAC2/IO94RSB1	42	IO58RSB1	78	GBB1/IO22RSB0
7	IO93RSB1	43	IO57RSB1	79	GBB0/IO21RSB0
8	IO92RSB1	44	GDC2/IO56RSB1	80	GBC1/IO20RSB0
9	GND	45	GDB2/IO55RSB1	81	GBC0/IO19RSB0
10	GFB1/IO87RSB1	46	GDA2/IO54RSB1	82	IO18RSB0
11	GFB0/IO86RSB1	47	TCK	83	IO17RSB0
12	VCOMPLF	48	TDI	84	IO15RSB0
13	GFA0/IO85RSB1	49	TMS	85	IO13RSB0
14	VCCPLF	50	VMV1	86	IO11RSB0
15	GFA1/IO84RSB1	51	GND	87	VCCIB0
16	GFA2/IO83RSB1	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB1	54	TDO	90	IO10RSB0
19	GEC1/IO77RSB1	55	TRST	91	IO09RSB0
20	GEB1/IO75RSB1	56	VJTAG	92	IO08RSB0
21	GEB0/IO74RSB1	57	GDA1/IO49RSB0	93	GAC1/IO07RSB0
22	GEA1/IO73RSB1	58	GDC0/IO46RSB0	94	GAC0/IO06RSB0
23	GEA0/IO72RSB1	59	GDC1/IO45RSB0	95	GAB1/IO05RSB0
24	VMV1	60	GCC2/IO43RSB0	96	GAB0/IO04RSB0
25	GNDQ	61	GCB2/IO42RSB0	97	GAA1/IO03RSB0
26	GEA2/IO71RSB1	62	GCA0/IO40RSB0	98	GAA0/IO02RSB0
27	FF/GEB2/IO70RSB1	63	GCA1/IO39RSB0	99	IO01RSB0
28	GEC2/IO69RSB1	64	GCC0/IO36RSB0	100	IO00RSB0
29	IO68RSB1	65	GCC1/IO35RSB0		
30	IO67RSB1	66	VCCIB0		
31	IO66RSB1	67	GND		
32	IO65RSB1	68	VCC		
33	IO64RSB1	69	IO31RSB0		
34	IO63RSB1	70	GBC2/IO29RSB0		
35	IO62RSB1	71	GBB2/IO27RSB0		
36	IO61RSB1	72	IO26RSB0		

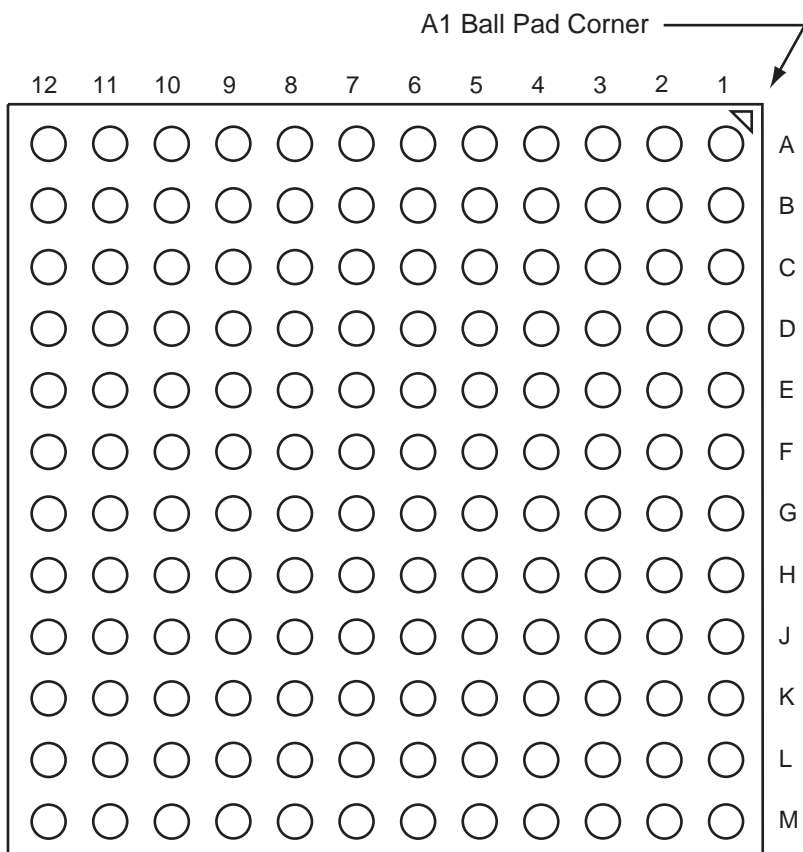
100-Pin VQFP	
Pin Number	AGL125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1

100-Pin VQFP	
Pin Number	AGL125 Function
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0

100-Pin VQFP	
Pin Number	AGL125 Function
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

100-Pin VQFP		100-Pin VQFP		100-Pin VQFP	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
1	GND	37	VCC	73	GBA2/IO41PDB1
2	GAA2/IO118UDB3	38	GND	74	VMV1
3	IO118VDB3	39	VCCIB2	75	GNDQ
4	GAB2/IO117UDB3	40	IO77RSB2	76	GBA1/IO40RSB0
5	IO117VDB3	41	IO74RSB2	77	GBA0/IO39RSB0
6	GAC2/IO116UDB3	42	IO71RSB2	78	GBB1/IO38RSB0
7	IO116VDB3	43	GDC2/IO63RSB2	79	GBB0/IO37RSB0
8	IO112PSB3	44	GDB2/IO62RSB2	80	GBC1/IO36RSB0
9	GND	45	GDA2/IO61RSB2	81	GBC0/IO35RSB0
10	GFB1/IO109PDB3	46	GNDQ	82	IO29RSB0
11	GFB0/IO109NDB3	47	TCK	83	IO27RSB0
12	VCOMPLF	48	TDI	84	IO25RSB0
13	GFA0/IO108NPB3	49	TMS	85	IO23RSB0
14	VCCPLF	50	VMV2	86	IO21RSB0
15	GFA1/IO108PPB3	51	GND	87	VCCIB0
16	GFA2/IO107PSB3	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB3	54	TDO	90	IO15RSB0
19	GFC2/IO105PSB3	55	TRST	91	IO13RSB0
20	GEC1/IO100PDB3	56	VJTAG	92	IO11RSB0
21	GEC0/IO100NDB3	57	GDA1/IO60USB1	93	GAC1/IO05RSB0
22	GEA1/IO98PDB3	58	GDC0/IO58VDB1	94	GAC0/IO04RSB0
23	GEA0/IO98NDB3	59	GDC1/IO58UDB1	95	GAB1/IO03RSB0
24	VMV3	60	IO52NDB1	96	GAB0/IO02RSB0
25	GNDQ	61	GCB2/IO52PDB1	97	GAA1/IO01RSB0
26	GEA2/IO97RSB2	62	GCA1/IO50PDB1	98	GAA0/IO00RSB0
27	FF/GE2/IO96RSB2	63	GCA0/IO50NDB1	99	GNDQ
28	GEC2/IO95RSB2	64	GCC0/IO48NDB1	100	VMV0
29	IO93RSB2	65	GCC1/IO48PDB1		
30	IO92RSB2	66	VCCIB1		
31	IO91RSB2	67	GND		
32	IO90RSB2	68	VCC		
33	IO88RSB2	69	IO43NDB1		
34	IO86RSB2	70	GBC2/IO43PDB1		
35	IO85RSB2	71	GBB2/IO42PSB1		
36	IO84RSB2	72	IO41NDB1		

## 144-Pin FBGA



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	AGL125 Function	Pin Number	AGL125 Function	Pin Number	AGL125 Function
A1	GNDQ	D1	IO128RSB1	G1	GFA1/IO121RSB1
A2	VMV0	D2	IO129RSB1	G2	GND
A3	GAB0/IO02RSB0	D3	IO130RSB1	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO67RSB1	G4	GFA0/IO122RSB1
A5	IO11RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO18RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	VCC	D8	GBC1/IO36RSB0	G8	GDC1/IO61RSB0
A9	IO25RSB0	D9	GBB2/IO43RSB0	G9	IO48RSB0
A10	GBA0/IO39RSB0	D10	IO28RSB0	G10	GCC2/IO59RSB0
A11	GBA1/IO40RSB0	D11	IO44RSB0	G11	IO47RSB0
A12	GNDQ	D12	GCB1/IO53RSB0	G12	GCB2/IO58RSB0
B1	GAB2/IO69RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO125RSB1	H2	GFB2/IO119RSB1
B3	GAA0/IO00RSB0	E3	GFC1/IO126RSB1	H3	GFC2/IO118RSB1
B4	GAA1/IO01RSB0	E4	VCCIB1	H4	GEC1/IO112RSB1
B5	IO08RSB0	E5	IO68RSB1	H5	VCC
B6	IO14RSB0	E6	VCCIB0	H6	IO50RSB0
B7	IO19RSB0	E7	VCCIB0	H7	IO60RSB0
B8	IO22RSB0	E8	GCC1/IO51RSB0	H8	GDB2/IO71RSB1
B9	GBB0/IO37RSB0	E9	VCCIB0	H9	GDC0/IO62RSB0
B10	GBB1/IO38RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO56RSB0	H11	IO49RSB0
B12	VMV0	E12	IO46RSB0	H12	VCC
C1	IO132RSB1	F1	GFB0/IO123RSB1	J1	GEB1/IO110RSB1
C2	GFA2/IO120RSB1	F2	VCOMPLF	J2	IO115RSB1
C3	GAC2/IO131RSB1	F3	GFB1/IO124RSB1	J3	VCCIB1
C4	VCC	F4	IO127RSB1	J4	GEC0/IO111RSB1
C5	IO10RSB0	F5	GND	J5	IO116RSB1
C6	IO12RSB0	F6	GND	J6	IO117RSB1
C7	IO21RSB0	F7	GND	J7	VCC
C8	IO24RSB0	F8	GCC0/IO52RSB0	J8	TCK
C9	IO27RSB0	F9	GCB0/IO54RSB0	J9	GDA2/IO70RSB1
C10	GBA2/IO41RSB0	F10	GND	J10	TDO
C11	IO42RSB0	F11	GCA1/IO55RSB0	J11	GDA1/IO65RSB0
C12	GBC2/IO45RSB0	F12	GCA2/IO57RSB0	J12	GDB1/IO63RSB0

144-Pin FBGA	
Pin Number	AGL125 Function
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	FF/GEB2/IO105RSB 1
L4	IO102RSB1
L5	VCCIB1
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	VCCIB1

144-Pin FBGA	
Pin Number	AGL125 Function
M11	VPUMP
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
A1	GNDQ	D1	IO112NDB3	G1	GFA1/IO108PPB3
A2	VMV0	D2	IO112PDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO116VDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO118UPB3	G4	GFA0/IO108NPB3
A5	IO16RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO29RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	VCC	D8	GBC1/IO36RSB0	G8	GDC1/IO58UPB1
A9	IO33RSB0	D9	GBB2/IO42PDB1	G9	IO53NDB1
A10	GBA0/IO39RSB0	D10	IO42NDB1	G10	GCC2/IO53PDB1
A11	GBA1/IO40RSB0	D11	IO43NPB1	G11	IO52NDB1
A12	GNDQ	D12	GCB1/IO49PPB1	G12	GCB2/IO52PDB1
B1	GAB2/IO117UDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO110NDB3	H2	GFB2/IO106PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO110PDB3	H3	GFC2/IO105PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO100PDB3
B5	IO14RSB0	E5	IO118VPB3	H5	VCC
B6	IO19RSB0	E6	VCCIB0	H6	IO79RSB2
B7	IO22RSB0	E7	VCCIB0	H7	IO65RSB2
B8	IO30RSB0	E8	GCC1/IO48PDB1	H8	GDB2/IO62RSB2
B9	GBB0/IO37RSB0	E9	VCCIB1	H9	GDC0/IO58VPB1
B10	GBB1/IO38RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO50NDB1	H11	IO54PSB1
B12	VMV1	E12	IO51NDB1	H12	VCC
C1	IO117VDB3	F1	GFB0/IO109NPB3	J1	GEB1/IO99PDB3
C2	GFA2/IO107PPB3	F2	VCOMPLF	J2	IO106NDB3
C3	GAC2/IO116UDB3	F3	GFB1/IO109PPB3	J3	VCCIB3
C4	VCC	F4	IO107NPB3	J4	GEC0/IO100NDB3
C5	IO12RSB0	F5	GND	J5	IO88RSB2
C6	IO17RSB0	F6	GND	J6	IO81RSB2
C7	IO24RSB0	F7	GND	J7	VCC
C8	IO31RSB0	F8	GCC0/IO48NDB1	J8	TCK
C9	IO34RSB0	F9	GCB0/IO49NPB1	J9	GDA2/IO61RSB2
C10	GBA2/IO41PDB1	F10	GND	J10	TDO
C11	IO41NDB1	F11	GCA1/IO50PDB1	J11	GDA1/IO60UDB1
C12	GBC2/IO43PPB1	F12	GCA2/IO51PDB1	J12	GDB1/IO59UDB1



144-Pin FBGA	
Pin Number	AGL250 Function
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GNDQ	D1	IO149NDB3	G1	GFA1/IO145PPB3
A2	VMV0	D2	IO149PDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO153VDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO155UPB3	G4	GFA0/IO145NPB3
A5	IO16RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO30RSB0	D7	GBC0/IO54RSB0	G7	GND
A8	VCC	D8	GBC1/IO55RSB0	G8	GDC1/IO77UPB1
A9	IO34RSB0	D9	GBB2/IO61PDB1	G9	IO72NDB1
A10	GBA0/IO58RSB0	D10	IO61NDB1	G10	GCC2/IO72PDB1
A11	GBA1/IO59RSB0	D11	IO62NPB1	G11	IO71NDB1
A12	GNDQ	D12	GCB1/IO68PPB1	G12	GCB2/IO71PDB1
B1	GAB2/IO154UDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO147NDB3	H2	GFB2/IO143PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO147PDB3	H3	GFC2/IO142PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO137PDB3
B5	IO14RSB0	E5	IO155VPB3	H5	VCC
B6	IO19RSB0	E6	VCCIB0	H6	IO75PDB1
B7	IO23RSB0	E7	VCCIB0	H7	IO75NDB1
B8	IO31RSB0	E8	GCC1/IO67PDB1	H8	GDB2/IO81RSB2
B9	GBB0/IO56RSB0	E9	VCCIB1	H9	GDC0/IO77VPB1
B10	GBB1/IO57RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO69NDB1	H11	IO73PSB1
B12	VMV1	E12	IO70NDB1	H12	VCC
C1	IO154VDB3	F1	GFB0/IO146NPB3	J1	GEB1/IO136PDB3
C2	GFA2/IO144PPB3	F2	VCOMPLF	J2	IO143NDB3
C3	GAC2/IO153UDB3	F3	GFB1/IO146PPB3	J3	VCCIB3
C4	VCC	F4	IO144NPB3	J4	GEC0/IO137NDB3
C5	IO12RSB0	F5	GND	J5	IO125RSB2
C6	IO17RSB0	F6	GND	J6	IO116RSB2
C7	IO25RSB0	F7	GND	J7	VCC
C8	IO32RSB0	F8	GCC0/IO67NDB1	J8	TCK
C9	IO53RSB0	F9	GCB0/IO68NPB1	J9	GDA2/IO80RSB2
C10	GBA2/IO60PDB1	F10	GND	J10	TDO
C11	IO60NDB1	F11	GCA1/IO69PDB1	J11	GDA1/IO79UDB1
C12	GBC2/IO62PPB1	F12	GCA2/IO70PDB1	J12	GDB1/IO78UDB1

144-Pin FBGA	
Pin Number	AGL400 Function
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO133RS B2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2

144-Pin FBGA	
Pin Number	AGL400 Function
M11	VPUMP
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
A1	GNDQ	D1	IO169PDB3	G1	GFA1/IO162PPB3
A2	VMV0	D2	IO169NDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO172NDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO174PPB3	G4	GFA0/IO162NPB3
A5	IO10RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO34RSB0	D7	GBC0/IO54RSB0	G7	GND
A8	VCC	D8	GBC1/IO55RSB0	G8	GDC1/IO86PPB1
A9	IO50RSB0	D9	GBB2/IO61PDB1	G9	IO74NDB1
A10	GBA0/IO58RSB0	D10	IO61NDB1	G10	GCC2/IO74PDB1
A11	GBA1/IO59RSB0	D11	IO62NPB1	G11	IO73NDB1
A12	GNDQ	D12	GCB1/IO70PPB1	G12	GCB2/IO73PDB1
B1	GAB2/IO173PDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO164NDB3	H2	GFB2/IO160PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO164PDB3	H3	GFC2/IO159PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO146PDB3
B5	IO13RSB0	E5	IO174NPB3	H5	VCC
B6	IO19RSB0	E6	VCCIB0	H6	IO80PDB1
B7	IO31RSB0	E7	VCCIB0	H7	IO80NDB1
B8	IO39RSB0	E8	GCC1/IO69PDB1	H8	GDB2/IO90RSB2
B9	GBB0/IO56RSB0	E9	VCCIB1	H9	GDC0/IO86NPB1
B10	GBB1/IO57RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO71NDB1	H11	IO84PSB1
B12	VMV1	E12	IO72NDB1	H12	VCC
C1	IO173NDB3	F1	GFB0/IO163NPB3	J1	GEB1/IO145PDB3
C2	GFA2/IO161PPB3	F2	VCOMPLF	J2	IO160NDB3
C3	GAC2/IO172PDB3	F3	GFB1/IO163PPB3	J3	VCCIB3
C4	VCC	F4	IO161NPB3	J4	GEC0/IO146NDB3
C5	IO16RSB0	F5	GND	J5	IO129RSB2
C6	IO25RSB0	F6	GND	J6	IO131RSB2
C7	IO28RSB0	F7	GND	J7	VCC
C8	IO42RSB0	F8	GCC0/IO69NDB1	J8	TCK
C9	IO45RSB0	F9	GCB0/IO70NPB1	J9	GDA2/IO89RSB2
C10	GBA2/IO60PDB1	F10	GND	J10	TDO
C11	IO60NDB1	F11	GCA1/IO71PDB1	J11	GDA1/IO88PDB1
C12	GBC2/IO62PPB1	F12	GCA2/IO72PDB1	J12	GDB1/IO87PDB1

144-Pin FBGA	
Pin Number	AGL600 Function
K1	GEB0/IO145NDB3
K2	GEA1/IO144PDB3
K3	GEA0/IO144NDB3
K4	GEA2/IO143RSB2
K5	IO119RSB2
K6	IO111RSB2
K7	GND
K8	IO94RSB2
K9	GDC2/IO91RSB2
K10	GND
K11	GDA0/IO88NDB1
K12	GDB0/IO87NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO142RSB 2
L4	IO136RSB2
L5	VCCIB2
L6	IO115RSB2
L7	IO103RSB2
L8	IO97RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO141RSB2
M3	IO138RSB2
M4	IO123RSB2
M5	IO126RSB2
M6	IO134RSB2
M7	IO108RSB2
M8	IO99RSB2
M9	TDI
M10	VCCIB2

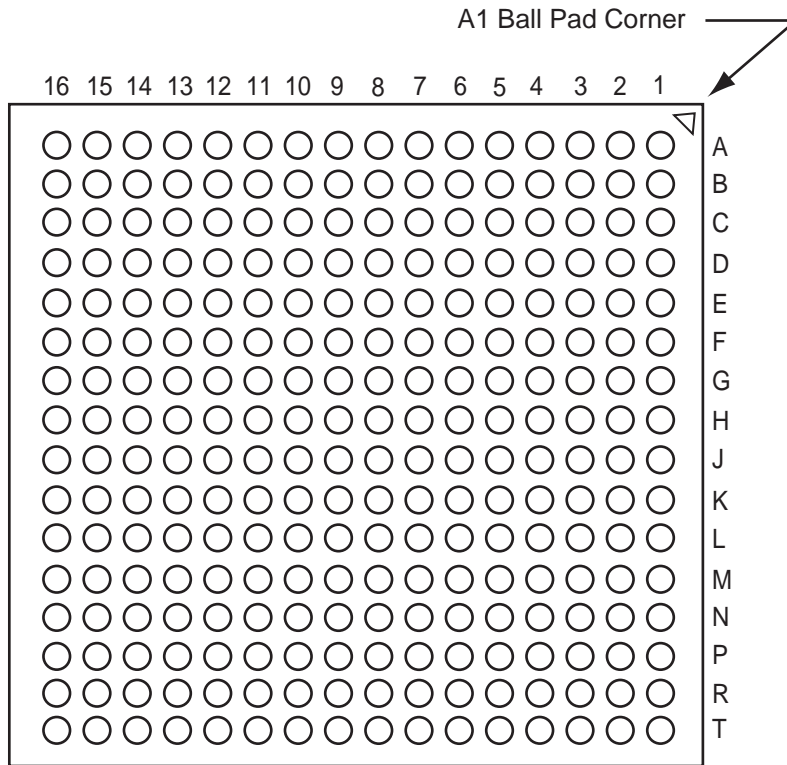
144-Pin FBGA	
Pin Number	AGL600 Function
M11	VPUMP
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
A1	GNDQ	D1	IO213PDB3	G1	GFA1/IO207PPB3
A2	VMV0	D2	IO213NDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO223NDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO225PPB3	G4	GFA0/IO207NPB3
A5	IO10RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO44RSB0	D7	GBC0/IO72RSB0	G7	GND
A8	VCC	D8	GBC1/IO73RSB0	G8	GDC1/IO111PPB1
A9	IO69RSB0	D9	GBB2/IO79PDB1	G9	IO96NDB1
A10	GBA0/IO76RSB0	D10	IO79NDB1	G10	GCC2/IO96PDB1
A11	GBA1/IO77RSB0	D11	IO80NPB1	G11	IO95NDB1
A12	GNDQ	D12	GCB1/IO92PPB1	G12	GCB2/IO95PDB1
B1	GAB2/IO224PDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO209NDB3	H2	GFB2/IO205PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO209PDB3	H3	GFC2/IO204PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO190PDB3
B5	IO13RSB0	E5	IO225NPB3	H5	VCC
B6	IO26RSB0	E6	VCCIB0	H6	IO105PDB1
B7	IO35RSB0	E7	VCCIB0	H7	IO105NDB1
B8	IO60RSB0	E8	GCC1/IO91PDB1	H8	GDB2/IO115RSB2
B9	GBB0/IO74RSB0	E9	VCCIB1	H9	GDC0/IO111NPB1
B10	GBB1/IO75RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO93NDB1	H11	IO101PSB1
B12	VMV1	E12	IO94NDB1	H12	VCC
C1	IO224NDB3	F1	GFB0/IO208NPB3	J1	GEB1/IO189PDB3
C2	GFA2/IO206PPB3	F2	VCOMPLF	J2	IO205NDB3
C3	GAC2/IO223PDB3	F3	GFB1/IO208PPB3	J3	VCCIB3
C4	VCC	F4	IO206NPB3	J4	GEC0/IO190NDB3
C5	IO16RSB0	F5	GND	J5	IO160RSB2
C6	IO29RSB0	F6	GND	J6	IO157RSB2
C7	IO32RSB0	F7	GND	J7	VCC
C8	IO63RSB0	F8	GCC0/IO91NDB1	J8	TCK
C9	IO66RSB0	F9	GCB0/IO92NPB1	J9	GDA2/IO114RSB2
C10	GBA2/IO78PDB1	F10	GND	J10	TDO
C11	IO78NDB1	F11	GCA1/IO93PDB1	J11	GDA1/IO113PDB1
C12	GBC2/IO80PPB1	F12	GCA2/IO94PDB1	J12	GDB1/IO112PDB1

144-Pin FBGA	
Pin Number	AGL1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB 2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2

144-Pin FBGA	
Pin Number	AGL1000 Function
M11	VPUMP
M12	GNDQ

## 256-Pin FBGA



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.



256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GND	C5	GAC0/IO04RSB0	E9	IO31RSB0
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	VCCIB0
A3	GAA1/IO01RSB0	C7	IO20RSB0	E11	VCCIB0
A4	GAB0/IO02RSB0	C8	IO24RSB0	E12	VMV1
A5	IO16RSB0	C9	IO33RSB0	E13	GBC2/IO62PDB1
A6	IO17RSB0	C10	IO39RSB0	E14	IO65RSB1
A7	IO22RSB0	C11	IO45RSB0	E15	IO52RSB0
A8	IO28RSB0	C12	GBC0/IO54RSB0	E16	IO66PDB1
A9	IO34RSB0	C13	IO48RSB0	F1	IO150NDB3
A10	IO37RSB0	C14	VMV0	F2	IO149NPB3
A11	IO41RSB0	C15	IO61NPB1	F3	IO09RSB0
A12	IO43RSB0	C16	IO63PDB1	F4	IO152UDB3
A13	GBB1/IO57RSB0	D1	IO151VDB3	F5	VCCIB3
A14	GBA0/IO58RSB0	D2	IO151UDB3	F6	GND
A15	GBA1/IO59RSB0	D3	GAC2/IO153UDB3	F7	VCC
A16	GND	D4	IO06RSB0	F8	VCC
B1	GAB2/IO154UDB3	D5	GNDQ	F9	VCC
B2	GAA2/IO155UDB3	D6	IO10RSB0	F10	VCC
B3	IO12RSB0	D7	IO19RSB0	F11	GND
B4	GAB1/IO03RSB0	D8	IO26RSB0	F12	VCCIB1
B5	IO13RSB0	D9	IO30RSB0	F13	IO62NDB1
B6	IO14RSB0	D10	IO40RSB0	F14	IO49RSB0
B7	IO21RSB0	D11	IO46RSB0	F15	IO64PPB1
B8	IO27RSB0	D12	GNDQ	F16	IO66NDB1
B9	IO32RSB0	D13	IO47RSB0	G1	IO148NDB3
B10	IO38RSB0	D14	GBB2/IO61PPB1	G2	IO148PDB3
B11	IO42RSB0	D15	IO53RSB0	G3	IO149PPB3
B12	GBC1/IO55RSB0	D16	IO63NDB1	G4	GFC1/IO147PPB3
B13	GBB0/IO56RSB0	E1	IO150PDB3	G5	VCCIB3
B14	IO44RSB0	E2	IO08RSB0	G6	VCC
B15	GBA2/IO60PDB1	E3	IO153VDB3	G7	GND
B16	IO60NDB1	E4	IO152VDB3	G8	GND
C1	IO154VDB3	E5	VMV0	G9	GND
C2	IO155VDB3	E6	VCCIB0	G10	GND
C3	IO11RSB0	E7	VCCIB0	G11	VCC
C4	IO07RSB0	E8	IO25RSB0	G12	VCCIB1

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
G13	GCC1/IO67PPB1	K1	GFC2/IO142PDB3	M5	VMV3
G14	IO64NPB1	K2	IO144NPB3	M6	VCCIB2
G15	IO73PDB1	K3	IO141PPB3	M7	VCCIB2
G16	IO73NDB1	K4	IO120RSB2	M8	IO108RSB2
H1	GFB0/IO146NPB3	K5	VCCIB3	M9	IO101RSB2
H2	GFA0/IO145NDB3	K6	VCC	M10	VCCIB2
H3	GFB1/IO146PPB3	K7	GND	M11	VCCIB2
H4	VCOMPLF	K8	GND	M12	VMV2
H5	GFC0/IO147NPB3	K9	GND	M13	IO83RSB2
H6	VCC	K10	GND	M14	GDB1/IO78UPB1
H7	GND	K11	VCC	M15	GDC1/IO77UDB1
H8	GND	K12	VCCIB1	M16	IO75NDB1
H9	GND	K13	IO71NPB1	N1	IO140NDB3
H10	GND	K14	IO74RSB1	N2	IO138PPB3
H11	VCC	K15	IO72NPB1	N3	GEC1/IO137PPB3
H12	GCC0/IO67NPB1	K16	IO70NDB1	N4	IO131RSB2
H13	GCB1/IO68PPB1	L1	IO142NDB3	N5	GNDQ
H14	GCA0/IO69NPB1	L2	IO141NPB3	N6	GEA2/IO134RSB2
H15	NC	L3	IO125RSB2	N7	IO117RSB2
H16	GCB0/IO68NPB1	L4	IO139RSB3	N8	IO111RSB2
J1	GFA2/IO144PPB3	L5	VCCIB3	N9	IO99RSB2
J2	GFA1/IO145PDB3	L6	GND	N10	IO94RSB2
J3	VCCPLF	L7	VCC	N11	IO87RSB2
J4	IO143NDB3	L8	VCC	N12	GNDQ
J5	GFB2/IO143PDB3	L9	VCC	N13	IO93RSB2
J6	VCC	L10	VCC	N14	VJTAG
J7	GND	L11	GND	N15	GDC0/IO77VDB1
J8	GND	L12	VCCIB1	N16	GDA1/IO79UDB1
J9	GND	L13	GDB0/IO78VPB1	P1	GEB1/IO136PDB3
J10	GND	L14	IO76VDB1	P2	GEB0/IO136NDB3
J11	VCC	L15	IO76UDB1	P3	VMV2
J12	GCB2/IO71PPB1	L16	IO75PDB1	P4	IO129RSB2
J13	GCA1/IO69PPB1	M1	IO140PDB3	P5	IO128RSB2
J14	GCC2/IO72PPB1	M2	IO130RSB2	P6	IO122RSB2
J15	NC	M3	IO138NPB3	P7	IO115RSB2
J16	GCA2/IO70PDB1	M4	GEC0/IO137NPB3	P8	IO110RSB2

256-Pin FBGA	
Pin Number	AGL400 Function
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	FF/GEB2/IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2
T12	GDC2/IO82RSB2

256-Pin FBGA	
Pin Number	AGL400 Function
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
A1	GND	C7	IO20RSB0	E13	GBC2/IO62PDB1
A2	GAA0/IO00RSB0	C8	IO24RSB0	E14	IO67PPB1
A3	GAA1/IO01RSB0	C9	IO33RSB0	E15	IO64PPB1
A4	GAB0/IO02RSB0	C10	IO39RSB0	E16	IO66PDB1
A5	IO11RSB0	C11	IO44RSB0	F1	IO166NDB3
A6	IO16RSB0	C12	GBC0/IO54RSB0	F2	IO168NPB3
A7	IO18RSB0	C13	IO51RSB0	F3	IO167PPB3
A8	IO28RSB0	C14	VMV0	F4	IO169PDB3
A9	IO34RSB0	C15	IO61NPB1	F5	VCCIB3
A10	IO37RSB0	C16	IO63PDB1	F6	GND
A11	IO41RSB0	D1	IO171NDB3	F7	VCC
A12	IO43RSB0	D2	IO171PDB3	F8	VCC
A13	GBB1/IO57RSB0	D3	GAC2/IO172PDB3	F9	VCC
A14	GBA0/IO58RSB0	D4	IO06RSB0	F10	VCC
A15	GBA1/IO59RSB0	D5	GNDQ	F11	GND
A16	GND	D6	IO10RSB0	F12	VCCIB1
B1	GAB2/IO173PDB3	D7	IO19RSB0	F13	IO62NDB1
B2	GAA2/IO174PDB3	D8	IO26RSB0	F14	IO64NPB1
B3	GNDQ	D9	IO30RSB0	F15	IO65PPB1
B4	GAB1/IO03RSB0	D10	IO40RSB0	F16	IO66NDB1
B5	IO13RSB0	D11	IO45RSB0	G1	IO165NDB3
B6	IO14RSB0	D12	GNDQ	G2	IO165PDB3
B7	IO21RSB0	D13	IO50RSB0	G3	IO168PPB3
B8	IO27RSB0	D14	GBB2/IO61PPB1	G4	GFC1/IO164PPB3
B9	IO32RSB0	D15	IO53RSB0	G5	VCCIB3
B10	IO38RSB0	D16	IO63NDB1	G6	VCC
B11	IO42RSB0	E1	IO166PDB3	G7	GND
B12	GBC1/IO55RSB0	E2	IO167NPB3	G8	GND
B13	GBB0/IO56RSB0	E3	IO172NDB3	G9	GND
B14	IO52RSB0	E4	IO169NDB3	G10	GND
B15	GBA2/IO60PDB1	E5	VMV0	G11	VCC
B16	IO60NDB1	E6	VCCIB0	G12	VCCIB1
C1	IO173NDB3	E7	VCCIB0	G13	GCC1/IO69PPB1
C2	IO174NDB3	E8	IO25RSB0	G14	IO65NPB1
C3	VMV3	E9	IO31RSB0	G15	IO75PDB1
C4	IO07RSB0	E10	VCCIB0	G16	IO75NDB1
C5	GAC0/IO04RSB0	E11	VCCIB0	H1	GFB0/IO163NPB3
C6	GAC1/IO05RSB0	E12	VMV1	H2	GFA0/IO162NDB3

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
H3	GFB1/IO163PPB3	K9	GND	M15	GDC1/IO86PDB1
H4	VCOMPLF	K10	GND	M16	IO84NDB1
H5	GFC0/IO164NPB3	K11	VCC	N1	IO150NDB3
H6	VCC	K12	VCCIB1	N2	IO147PPB3
H7	GND	K13	IO73NPB1	N3	GEC1/IO146PPB3
H8	GND	K14	IO80NPB1	N4	IO140RSB2
H9	GND	K15	IO74NPB1	N5	GNDQ
H10	GND	K16	IO72NDB1	N6	GEA2/IO143RSB2
H11	VCC	L1	IO159NDB3	N7	IO126RSB2
H12	GCC0/IO69NPB1	L2	IO156NPB3	N8	IO120RSB2
H13	GCB1/IO70PPB1	L3	IO151PPB3	N9	IO108RSB2
H14	GCA0/IO71NPB1	L4	IO158PSB3	N10	IO103RSB2
H15	IO67NPB1	L5	VCCIB3	N11	IO99RSB2
H16	GCB0/IO70NPB1	L6	GND	N12	GNDQ
J1	GFA2/IO161PPB3	L7	VCC	N13	IO92RSB2
J2	GFA1/IO162PDB3	L8	VCC	N14	VJTAG
J3	VCCPLF	L9	VCC	N15	GDC0/IO86NDB1
J4	IO160NDB3	L10	VCC	N16	GDA1/IO88PDB1
J5	GFB2/IO160PDB3	L11	GND	P1	GEB1/IO145PDB3
J6	VCC	L12	VCCIB1	P2	GEB0/IO145NDB3
J7	GND	L13	GDB0/IO87NPB1	P3	VMV2
J8	GND	L14	IO85NDB1	P4	IO138RSB2
J9	GND	L15	IO85PDB1	P5	IO136RSB2
J10	GND	L16	IO84PDB1	P6	IO131RSB2
J11	VCC	M1	IO150PDB3	P7	IO124RSB2
J12	GCB2/IO73PPB1	M2	IO151NPB3	P8	IO119RSB2
J13	GCA1/IO71PPB1	M3	IO147NPB3	P9	IO107RSB2
J14	GCC2/IO74PPB1	M4	GEC0/IO146NPB3	P10	IO104RSB2
J15	IO80PPB1	M5	VMV3	P11	IO97RSB2
J16	GCA2/IO72PDB1	M6	VCCIB2	P12	VMV1
K1	GFC2/IO159PDB3	M7	VCCIB2	P13	TCK
K2	IO161NPB3	M8	IO117RSB2	P14	VPUMP
K3	IO156PPB3	M9	IO110RSB2	P15	TRST
K4	IO129RSB2	M10	VCCIB2	P16	GDA0/IO88NDB1
K5	VCCIB3	M11	VCCIB2	R1	GEA1/IO144PDB3
K6	VCC	M12	VMV2	R2	GEA0/IO144NDB3
K7	GND	M13	IO94RSB2	R3	IO139RSB2
K8	GND	M14	GDB1/IO87PPB1	R4	GEC2/IO141RSB2

256-Pin FBGA	
Pin Number	AGL600 Function
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/IO142RSB 2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

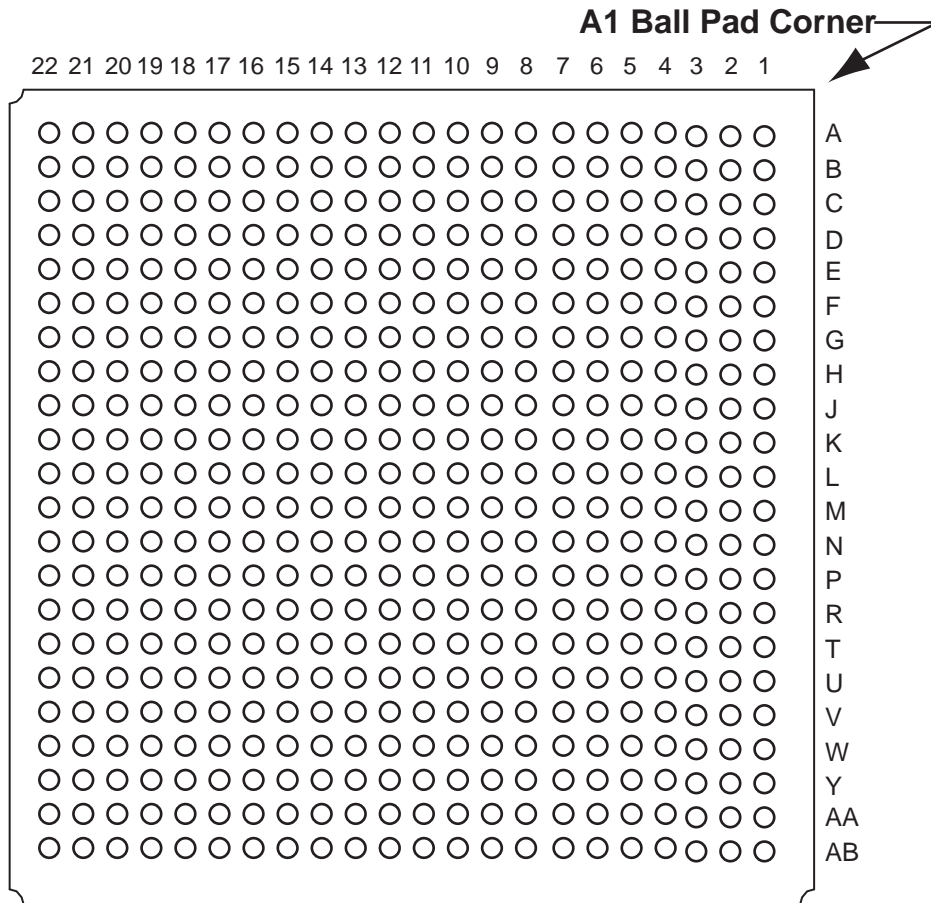
256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
A1	GND	C7	IO25RSB0	E13	GBC2/IO80PDB1
A2	GAA0/IO00RSB0	C8	IO36RSB0	E14	IO83PPB1
A3	GAA1/IO01RSB0	C9	IO42RSB0	E15	IO86PPB1
A4	GAB0/IO02RSB0	C10	IO49RSB0	E16	IO87PDB1
A5	IO16RSB0	C11	IO56RSB0	F1	IO217NDB3
A6	IO22RSB0	C12	GBC0/IO72RSB0	F2	IO218NDB3
A7	IO28RSB0	C13	IO62RSB0	F3	IO216PDB3
A8	IO35RSB0	C14	VMV0	F4	IO216NDB3
A9	IO45RSB0	C15	IO78NDB1	F5	VCCIB3
A10	IO50RSB0	C16	IO81NDB1	F6	GND
A11	IO55RSB0	D1	IO222NDB3	F7	VCC
A12	IO61RSB0	D2	IO222PDB3	F8	VCC
A13	GBB1/IO75RSB0	D3	GAC2/IO223PDB3	F9	VCC
A14	GBA0/IO76RSB0	D4	IO223NDB3	F10	VCC
A15	GBA1/IO77RSB0	D5	GNDQ	F11	GND
A16	GND	D6	IO23RSB0	F12	VCCIB1
B1	GAB2/IO224PDB3	D7	IO29RSB0	F13	IO83NPB1
B2	GAA2/IO225PDB3	D8	IO33RSB0	F14	IO86NPB1
B3	GNDQ	D9	IO46RSB0	F15	IO90PPB1
B4	GAB1/IO03RSB0	D10	IO52RSB0	F16	IO87NDB1
B5	IO17RSB0	D11	IO60RSB0	G1	IO210PSB3
B6	IO21RSB0	D12	GNDQ	G2	IO213NDB3
B7	IO27RSB0	D13	IO80NDB1	G3	IO213PDB3
B8	IO34RSB0	D14	GBB2/IO79PDB1	G4	GFC1/IO209PPB3
B9	IO44RSB0	D15	IO79NDB1	G5	VCCIB3
B10	IO51RSB0	D16	IO82NSB1	G6	VCC
B11	IO57RSB0	E1	IO217PDB3	G7	GND
B12	GBC1/IO73RSB0	E2	IO218PDB3	G8	GND
B13	GBB0/IO74RSB0	E3	IO221NDB3	G9	GND
B14	IO71RSB0	E4	IO221PDB3	G10	GND
B15	GBA2/IO78PDB1	E5	VMV0	G11	VCC
B16	IO81PDB1	E6	VCCIB0	G12	VCCIB1
C1	IO224NDB3	E7	VCCIB0	G13	GCC1/IO91PPB1
C2	IO225NDB3	E8	IO38RSB0	G14	IO90NPB1
C3	VMV3	E9	IO47RSB0	G15	IO88PDB1
C4	IO11RSB0	E10	VCCIB0	G16	IO88NDB1
C5	GAC0/IO04RSB0	E11	VCCIB0	H1	GFB0/IO208NPB3
C6	GAC1/IO05RSB0	E12	VMV1	H2	GFA0/IO207NDB3

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
H3	GFB1/IO208PPB3	K9	GND	M15	GDC1/IO111PDB1
H4	VCOMPLF	K10	GND	M16	IO107NDB1
H5	GFC0/IO209NPB3	K11	VCC	N1	IO194PSB3
H6	VCC	K12	VCCIB1	N2	IO192PPB3
H7	GND	K13	IO95NPB1	N3	GEC1/IO190PPB3
H8	GND	K14	IO100NPB1	N4	IO192NPB3
H9	GND	K15	IO102NDB1	N5	GNDQ
H10	GND	K16	IO102PDB1	N6	GEA2/IO187RSB2
H11	VCC	L1	IO202NDB3	N7	IO161RSB2
H12	GCC0/IO91NPB1	L2	IO202PDB3	N8	IO155RSB2
H13	GCB1/IO92PPB1	L3	IO196PPB3	N9	IO141RSB2
H14	GCA0/IO93NPB1	L4	IO193PPB3	N10	IO129RSB2
H15	IO96NPB1	L5	VCCIB3	N11	IO124RSB2
H16	GCB0/IO92NPB1	L6	GND	N12	GNDQ
J1	GFA2/IO206PSB3	L7	VCC	N13	IO110PDB1
J2	GFA1/IO207PDB3	L8	VCC	N14	VJTAG
J3	VCCPLF	L9	VCC	N15	GDC0/IO111NDB1
J4	IO205NDB3	L10	VCC	N16	GDA1/IO113PDB1
J5	GFB2/IO205PDB3	L11	GND	P1	GEB1/IO189PDB3
J6	VCC	L12	VCCIB1	P2	GEB0/IO189NDB3
J7	GND	L13	GDB0/IO112NPB1	P3	VMV2
J8	GND	L14	IO106NDB1	P4	IO179RSB2
J9	GND	L15	IO106PDB1	P5	IO171RSB2
J10	GND	L16	IO107PDB1	P6	IO165RSB2
J11	VCC	M1	IO197NSB3	P7	IO159RSB2
J12	GCB2/IO95PPB1	M2	IO196NPB3	P8	IO151RSB2
J13	GCA1/IO93PPB1	M3	IO193NPB3	P9	IO137RSB2
J14	GCC2/IO96PPB1	M4	GEC0/IO190NPB3	P10	IO134RSB2
J15	IO100PPB1	M5	VMV3	P11	IO128RSB2
J16	GCA2/IO94PSB1	M6	VCCIB2	P12	VMV1
K1	GFC2/IO204PDB3	M7	VCCIB2	P13	TCK
K2	IO204NDB3	M8	IO147RSB2	P14	VPUMP
K3	IO203NDB3	M9	IO136RSB2	P15	TRST
K4	IO203PDB3	M10	VCCIB2	P16	GDA0/IO113NDB1
K5	VCCIB3	M11	VCCIB2	R1	GEA1/IO188PDB3
K6	VCC	M12	VMV2	R2	GEA0/IO188NDB3
K7	GND	M13	IO110NDB1	R3	IO184RSB2
K8	GND	M14	GDB1/IO112PPB1	R4	GEC2/IO185RSB2



256-Pin FBGA	
Pin Number	AGL1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB 2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

## 484-Pin FBGA



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GND	AA15	NC	B7	NC
A2	GND	AA16	NC	B8	NC
A3	VCCIB0	AA17	NC	B9	NC
A4	NC	AA18	NC	B10	NC
A5	NC	AA19	NC	B11	NC
A6	IO15RSB0	AA20	NC	B12	NC
A7	IO18RSB0	AA21	VCCIB1	B13	NC
A8	NC	AA22	GND	B14	NC
A9	NC	AB1	GND	B15	NC
A10	IO23RSB0	AB2	GND	B16	NC
A11	IO29RSB0	AB3	VCCIB2	B17	NC
A12	IO35RSB0	AB4	NC	B18	NC
A13	IO36RSB0	AB5	NC	B19	NC
A14	NC	AB6	IO121RSB2	B20	NC
A15	NC	AB7	IO119RSB2	B21	VCCIB1
A16	IO50RSB0	AB8	IO114RSB2	B22	GND
A17	IO51RSB0	AB9	IO109RSB2	C1	VCCIB3
A18	NC	AB10	NC	C2	NC
A19	NC	AB11	NC	C3	NC
A20	VCCIB0	AB12	IO104RSB2	C4	NC
A21	GND	AB13	IO103RSB2	C5	GND
A22	GND	AB14	NC	C6	NC
AA1	GND	AB15	NC	C7	NC
AA2	VCCIB3	AB16	IO91RSB2	C8	VCC
AA3	NC	AB17	IO90RSB2	C9	VCC
AA4	NC	AB18	NC	C10	NC
AA5	NC	AB19	NC	C11	NC
AA6	NC	AB20	VCCIB2	C12	NC
AA7	NC	AB21	GND	C13	NC
AA8	NC	AB22	GND	C14	VCC
AA9	NC	B1	GND	C15	VCC
AA10	NC	B2	VCCIB3	C16	NC
AA11	NC	B3	NC	C17	NC
AA12	NC	B4	NC	C18	GND
AA13	NC	B5	NC	C19	NC
AA14	NC	B6	NC	C20	NC

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
C21	NC	E13	IO38RSB0	G5	IO151UDB3
C22	VCCIB1	E14	IO42RSB0	G6	GAC2/IO153UDB3
D1	NC	E15	GBC1/IO55RSB0	G7	IO6RSB0
D2	NC	E16	GBB0/IO56RSB0	G8	GNDQ
D3	NC	E17	IO44RSB0	G9	IO10RSB0
D4	GND	E18	GBA2/IO60PDB1	G10	IO19RSB0
D5	GAA0/IO00RSB0	E19	IO60NDB1	G11	IO26RSB0
D6	GAA1/IO01RSB0	E20	GND	G12	IO30RSB0
D7	GAB0/IO02RSB0	E21	NC	G13	IO40RSB0
D8	IO16RSB0	E22	NC	G14	IO46RSB0
D9	IO17RSB0	F1	NC	G15	GNDQ
D10	IO22RSB0	F2	NC	G16	IO47RSB0
D11	IO28RSB0	F3	NC	G17	GBB2/IO61PPB1
D12	IO34RSB0	F4	IO154VDB3	G18	IO53RSB0
D13	IO37RSB0	F5	IO155VDB3	G19	IO63NDB1
D14	IO41RSB0	F6	IO11RSB0	G20	NC
D15	IO43RSB0	F7	IO07RSB0	G21	NC
D16	GBB1/IO57RSB0	F8	GAC0/IO04RSB0	G22	NC
D17	GBA0/IO58RSB0	F9	GAC1/IO05RSB0	H1	NC
D18	GBA1/IO59RSB0	F10	IO20RSB0	H2	NC
D19	GND	F11	IO24RSB0	H3	VCC
D20	NC	F12	IO33RSB0	H4	IO150PDB3
D21	NC	F13	IO39RSB0	H5	IO08RSB0
D22	NC	F14	IO45RSB0	H6	IO153VDB3
E1	NC	F15	GBC0/IO54RSB0	H7	IO152VDB3
E2	NC	F16	IO48RSB0	H8	VMV0
E3	GND	F17	VMV0	H9	VCCIB0
E4	GAB2/IO154UDB3	F18	IO61NPB1	H10	VCCIB0
E5	GAA2/IO155UDB3	F19	IO63PDB1	H11	IO25RSB0
E6	IO12RSB0	F20	NC	H12	IO31RSB0
E7	GAB1/IO03RSB0	F21	NC	H13	VCCIB0
E8	IO13RSB0	F22	NC	H14	VCCIB0
E9	IO14RSB0	G1	NC	H15	VMV1
E10	IO21RSB0	G2	NC	H16	GBC2/IO62PDB1
E11	IO27RSB0	G3	NC	H17	IO65RSB1
E12	IO32RSB0	G4	IO151VDB3	H18	IO52RSB0

484-Pin FBGA	
Pin Number	AGL400 Function
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO150NDB3
J5	IO149NPB3
J6	IO09RSB0
J7	IO152UDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO49RSB0
J18	IO64PPB1
J19	IO66NDB1
J20	NC
J21	NC
J22	NC
K1	NC
K2	NC
K3	NC
K4	IO148NDB3
K5	IO148PDB3
K6	IO149PPB3
K7	GFC1/IO147PPB3
K8	VCCIB3
K9	VCC
K10	GND

484-Pin FBGA	
Pin Number	AGL400 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO67PPB1
K17	IO64NPB1
K18	IO73PDB1
K19	IO73NDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	VCOMPLF
L8	GFC0/IO147NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC

484-Pin FBGA	
Pin Number	AGL400 Function
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	VCCPLF
M7	IO143NDB3
M8	GFB2/IO143PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PPB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO141PPB3
N7	IO120RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO71NPB1

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
N17	IO74RSB1	R9	VCCIB2	U1	NC
N18	IO72NPB1	R10	VCCIB2	U2	NC
N19	IO70NDB1	R11	IO108RSB2	U3	NC
N20	NC	R12	IO101RSB2	U4	GEB1/IO136PDB3
N21	NC	R13	VCCIB2	U5	GEB0/IO136NDB3
N22	NC	R14	VCCIB2	U6	VMV2
P1	NC	R15	VMV2	U7	IO129RSB2
P2	NC	R16	IO83RSB2	U8	IO128RSB2
P3	NC	R17	GDB1/IO78UPB1	U9	IO122RSB2
P4	IO142NDB3	R18	GDC1/IO77UDB1	U10	IO115RSB2
P5	IO141NPB3	R19	IO75NDB1	U11	IO110RSB2
P6	IO125RSB2	R20	VCC	U12	IO98RSB2
P7	IO139RSB3	R21	NC	U13	IO95RSB2
P8	VCCIB3	R22	NC	U14	IO88RSB2
P9	GND	T1	NC	U15	IO84RSB2
P10	VCC	T2	NC	U16	TCK
P11	VCC	T3	NC	U17	VPUMP
P12	VCC	T4	IO140NDB3	U18	TRST
P13	VCC	T5	IO138PPB3	U19	GDA0/IO79VDB1
P14	GND	T6	GEC1/IO137PPB3	U20	NC
P15	VCCIB1	T7	IO131RSB2	U21	NC
P16	GDB0/IO78VPB1	T8	GNDQ	U22	NC
P17	IO76VDB1	T9	GEA2/IO134RSB2	V1	NC
P18	IO76UDB1	T10	IO117RSB2	V2	NC
P19	IO75PDB1	T11	IO111RSB2	V3	GND
P20	NC	T12	IO99RSB2	V4	GEA1/IO135PDB3
P21	NC	T13	IO94RSB2	V5	GEA0/IO135NDB3
P22	NC	T14	IO87RSB2	V6	IO127RSB2
R1	NC	T15	GNDQ	V7	GEC2/IO132RSB2
R2	NC	T16	IO93RSB2	V8	IO123RSB2
R3	VCC	T17	VJTAG	V9	IO118RSB2
R4	IO140PDB3	T18	GDC0/IO77VDB1	V10	IO112RSB2
R5	IO130RSB2	T19	GDA1/IO79UDB1	V11	IO106RSB2
R6	IO138NPB3	T20	NC	V12	IO100RSB2
R7	GEC0/IO137NPB3	T21	NC	V13	IO96RSB2
R8	VMV3	T22	NC	V14	IO89RSB2

484-Pin FBGA	
Pin Number	AGL400 Function
V15	IO85RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO126RSB2
W6	FF/GEB2/IO133RS B2
W7	IO124RSB2
W8	IO116RSB2
W9	IO113RSB2
W10	IO107RSB2
W11	IO105RSB2
W12	IO102RSB2
W13	IO97RSB2
W14	IO92RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	NC
Y3	NC
Y4	NC
Y5	GND

484-Pin FBGA	
Pin Number	AGL400 Function
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
A1	GND	AA15	NC	B7	IO12RSB0
A2	GND	AA16	IO101RSB2	B8	NC
A3	VCCIB0	AA17	NC	B9	NC
A4	NC	AA18	NC	B10	IO17RSB0
A5	NC	AA19	NC	B11	NC
A6	IO09RSB0	AA20	NC	B12	NC
A7	IO15RSB0	AA21	VCCIB1	B13	IO36RSB0
A8	NC	AA22	GND	B14	NC
A9	NC	AB1	GND	B15	NC
A10	IO22RSB0	AB2	GND	B16	IO47RSB0
A11	IO23RSB0	AB3	VCCIB2	B17	IO49RSB0
A12	IO29RSB0	AB4	NC	B18	NC
A13	IO35RSB0	AB5	NC	B19	NC
A14	NC	AB6	IO130RSB2	B20	NC
A15	NC	AB7	IO128RSB2	B21	VCCIB1
A16	IO46RSB0	AB8	IO122RSB2	B22	GND
A17	IO48RSB0	AB9	IO116RSB2	C1	VCCIB3
A18	NC	AB10	NC	C2	NC
A19	NC	AB11	NC	C3	NC
A20	VCCIB0	AB12	IO113RSB2	C4	NC
A21	GND	AB13	IO112RSB2	C5	GND
A22	GND	AB14	NC	C6	NC
AA1	GND	AB15	NC	C7	NC
AA2	VCCIB3	AB16	IO100RSB2	C8	VCC
AA3	NC	AB17	IO95RSB2	C9	VCC
AA4	NC	AB18	NC	C10	NC
AA5	NC	AB19	NC	C11	NC
AA6	IO135RSB2	AB20	VCCIB2	C12	NC
AA7	IO133RSB2	AB21	GND	C13	NC
AA8	NC	AB22	GND	C14	VCC
AA9	NC	B1	GND	C15	VCC
AA10	NC	B2	VCCIB3	C16	NC
AA11	NC	B3	NC	C17	NC
AA12	NC	B4	NC	C18	GND
AA13	NC	B5	NC	C19	NC
AA14	NC	B6	IO08RSB0	C20	NC



484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
C21	NC	E13	IO38RSB0	G5	IO171PDB3
C22	VCCIB1	E14	IO42RSB0	G6	GAC2/IO172PDB3
D1	NC	E15	GBC1/IO55RSB0	G7	IO06RSB0
D2	NC	E16	GBB0/IO56RSB0	G8	GNDQ
D3	NC	E17	IO52RSB0	G9	IO10RSB0
D4	GND	E18	GBA2/IO60PDB1	G10	IO19RSB0
D5	GAA0/IO00RSB0	E19	IO60NDB1	G11	IO26RSB0
D6	GAA1/IO01RSB0	E20	GND	G12	IO30RSB0
D7	GAB0/IO02RSB0	E21	NC	G13	IO40RSB0
D8	IO11RSB0	E22	NC	G14	IO45RSB0
D9	IO16RSB0	F1	NC	G15	GNDQ
D10	IO18RSB0	F2	NC	G16	IO50RSB0
D11	IO28RSB0	F3	NC	G17	GBB2/IO61PPB1
D12	IO34RSB0	F4	IO173NDB3	G18	IO53RSB0
D13	IO37RSB0	F5	IO174NDB3	G19	IO63NDB1
D14	IO41RSB0	F6	VMV3	G20	NC
D15	IO43RSB0	F7	IO07RSB0	G21	NC
D16	GBB1/IO57RSB0	F8	GAC0/IO04RSB0	G22	NC
D17	GBA0/IO58RSB0	F9	GAC1/IO05RSB0	H1	NC
D18	GBA1/IO59RSB0	F10	IO20RSB0	H2	NC
D19	GND	F11	IO24RSB0	H3	VCC
D20	NC	F12	IO33RSB0	H4	IO166PDB3
D21	NC	F13	IO39RSB0	H5	IO167NPB3
D22	NC	F14	IO44RSB0	H6	IO172NDB3
E1	NC	F15	GBC0/IO54RSB0	H7	IO169NDB3
E2	NC	F16	IO51RSB0	H8	VMV0
E3	GND	F17	VMV0	H9	VCCIB0
E4	GAB2/IO173PDB3	F18	IO61NPB1	H10	VCCIB0
E5	GAA2/IO174PDB3	F19	IO63PDB1	H11	IO25RSB0
E6	GNDQ	F20	NC	H12	IO31RSB0
E7	GAB1/IO03RSB0	F21	NC	H13	VCCIB0
E8	IO13RSB0	F22	NC	H14	VCCIB0
E9	IO14RSB0	G1	IO170NDB3	H15	VMV1
E10	IO21RSB0	G2	IO170PDB3	H16	GBC2/IO62PDB1
E11	IO27RSB0	G3	NC	H17	IO67PPB1
E12	IO32RSB0	G4	IO171NDB3	H18	IO64PPB1

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
H19	IO66PDB1	K11	GND	M3	IO158NPB3
H20	VCC	K12	GND	M4	GFA2/IO161PPB3
H21	NC	K13	GND	M5	GFA1/IO162PDB3
H22	NC	K14	VCC	M6	VCCPLF
J1	NC	K15	VCCIB1	M7	IO160NDB3
J2	NC	K16	GCC1/IO69PPB1	M8	GFB2/IO160PDB3
J3	NC	K17	IO65NPB1	M9	VCC
J4	IO166NDB3	K18	IO75PDB1	M10	GND
J5	IO168NPB3	K19	IO75NDB1	M11	GND
J6	IO167PPB3	K20	NC	M12	GND
J7	IO169PDB3	K21	IO76NDB1	M13	GND
J8	VCCIB3	K22	IO76PDB1	M14	VCC
J9	GND	L1	NC	M15	GCB2/IO73PPB1
J10	VCC	L2	IO155PDB3	M16	GCA1/IO71PPB1
J11	VCC	L3	NC	M17	GCC2/IO74PPB1
J12	VCC	L4	GFB0/IO163NPB3	M18	IO80PPB1
J13	VCC	L5	GFA0/IO162NDB3	M19	GCA2/IO72PDB1
J14	GND	L6	GFB1/IO163PPB3	M20	IO79PPB1
J15	VCCIB1	L7	VCOMPLF	M21	IO78PPB1
J16	IO62NDB1	L8	GFC0/IO164NPB3	M22	NC
J17	IO64NPB1	L9	VCC	N1	IO154NDB3
J18	IO65PPB1	L10	GND	N2	IO154PDB3
J19	IO66NDB1	L11	GND	N3	NC
J20	NC	L12	GND	N4	GFC2/IO159PDB3
J21	IO68PDB1	L13	GND	N5	IO161NPB3
J22	IO68NDB1	L14	VCC	N6	IO156PPB3
K1	IO157PDB3	L15	GCC0/IO69NPB1	N7	IO129RSB2
K2	IO157NDB3	L16	GCB1/IO70PPB1	N8	VCCIB3
K3	NC	L17	GCA0/IO71NPB1	N9	VCC
K4	IO165NDB3	L18	IO67NPB1	N10	GND
K5	IO165PDB3	L19	GCB0/IO70NPB1	N11	GND
K6	IO168PPB3	L20	IO77PDB1	N12	GND
K7	GFC1/IO164PPB3	L21	IO77NDB1	N13	GND
K8	VCCIB3	L22	IO78NPB1	N14	VCC
K9	VCC	M1	NC	N15	VCCIB1
K10	GND	M2	IO155NDB3	N16	IO73NPB1

484-Pin FBGA	
Pin Number	AGL600 Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

484-Pin FBGA	
Pin Number	AGL600 Function
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

484-Pin FBGA	
Pin Number	AGL600 Function
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2

484-Pin FBGA	
Pin Number	AGL600 Function
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB 2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND

484-Pin FBGA	
Pin Number	AGL600 Function
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
A1	GND	AA15	NC	B7	IO15RSB0
A2	GND	AA16	IO122RSB2	B8	IO19RSB0
A3	VCCIB0	AA17	IO119RSB2	B9	IO24RSB0
A4	IO07RSB0	AA18	IO117RSB2	B10	IO31RSB0
A5	IO09RSB0	AA19	NC	B11	IO39RSB0
A6	IO13RSB0	AA20	NC	B12	IO48RSB0
A7	IO18RSB0	AA21	VCCIB1	B13	IO54RSB0
A8	IO20RSB0	AA22	GND	B14	IO58RSB0
A9	IO26RSB0	AB1	GND	B15	IO63RSB0
A10	IO32RSB0	AB2	GND	B16	IO66RSB0
A11	IO40RSB0	AB3	VCCIB2	B17	IO68RSB0
A12	IO41RSB0	AB4	IO180RSB2	B18	IO70RSB0
A13	IO53RSB0	AB5	IO176RSB2	B19	NC
A14	IO59RSB0	AB6	IO173RSB2	B20	NC
A15	IO64RSB0	AB7	IO167RSB2	B21	VCCIB1
A16	IO65RSB0	AB8	IO162RSB2	B22	GND
A17	IO67RSB0	AB9	IO156RSB2	C1	VCCIB3
A18	IO69RSB0	AB10	IO150RSB2	C2	IO220PDB3
A19	NC	AB11	IO145RSB2	C3	NC
A20	VCCIB0	AB12	IO144RSB2	C4	NC
A21	GND	AB13	IO132RSB2	C5	GND
A22	GND	AB14	IO127RSB2	C6	IO10RSB0
AA1	GND	AB15	IO126RSB2	C7	IO14RSB0
AA2	VCCIB3	AB16	IO123RSB2	C8	VCC
AA3	NC	AB17	IO121RSB2	C9	VCC
AA4	IO181RSB2	AB18	IO118RSB2	C10	IO30RSB0
AA5	IO178RSB2	AB19	NC	C11	IO37RSB0
AA6	IO175RSB2	AB20	VCCIB2	C12	IO43RSB0
AA7	IO169RSB2	AB21	GND	C13	NC
AA8	IO166RSB2	AB22	GND	C14	VCC
AA9	IO160RSB2	B1	GND	C15	VCC
AA10	IO152RSB2	B2	VCCIB3	C16	NC
AA11	IO146RSB2	B3	NC	C17	NC
AA12	IO139RSB2	B4	IO06RSB0	C18	GND
AA13	IO133RSB2	B5	IO08RSB0	C19	NC
AA14	NC	B6	IO12RSB0	C20	NC

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
C21	NC	E13	IO51RSB0	G5	IO222PDB3
C22	VCCIB1	E14	IO57RSB0	G6	GAC2/IO223PDB3
D1	IO219PDB3	E15	GBC1/IO73RSB0	G7	IO223NDB3
D2	IO220NDB3	E16	GGB0/IO74RSB0	G8	GNDQ
D3	NC	E17	IO71RSB0	G9	IO23RSB0
D4	GND	E18	GBA2/IO78PDB1	G10	IO29RSB0
D5	GAA0/IO00RSB0	E19	IO81PDB1	G11	IO33RSB0
D6	GAA1/IO01RSB0	E20	GND	G12	IO46RSB0
D7	GAB0/IO02RSB0	E21	NC	G13	IO52RSB0
D8	IO16RSB0	E22	IO84PDB1	G14	IO60RSB0
D9	IO22RSB0	F1	NC	G15	GNDQ
D10	IO28RSB0	F2	IO215PDB3	G16	IO80NDB1
D11	IO35RSB0	F3	IO215NDB3	G17	GGB2/IO79PDB1
D12	IO45RSB0	F4	IO224NDB3	G18	IO79NDB1
D13	IO50RSB0	F5	IO225NDB3	G19	IO82NPB1
D14	IO55RSB0	F6	VMV3	G20	IO85PDB1
D15	IO61RSB0	F7	IO11RSB0	G21	IO85NDB1
D16	GGB1/IO75RSB0	F8	GAC0/IO04RSB0	G22	NC
D17	GBA0/IO76RSB0	F9	GAC1/IO05RSB0	H1	NC
D18	GBA1/IO77RSB0	F10	IO25RSB0	H2	NC
D19	GND	F11	IO36RSB0	H3	VCC
D20	NC	F12	IO42RSB0	H4	IO217PDB3
D21	NC	F13	IO49RSB0	H5	IO218PDB3
D22	NC	F14	IO56RSB0	H6	IO221NDB3
E1	IO219NDB3	F15	GBC0/IO72RSB0	H7	IO221PDB3
E2	NC	F16	IO62RSB0	H8	VMV0
E3	GND	F17	VMV0	H9	VCCIB0
E4	GAB2/IO224PDB3	F18	IO78NDB1	H10	VCCIB0
E5	GAA2/IO225PDB3	F19	IO81NDB1	H11	IO38RSB0
E6	GNDQ	F20	IO82PPB1	H12	IO47RSB0
E7	GAB1/IO03RSB0	F21	NC	H13	VCCIB0
E8	IO17RSB0	F22	IO84NDB1	H14	VCCIB0
E9	IO21RSB0	G1	IO214NDB3	H15	VMV1
E10	IO27RSB0	G2	IO214PDB3	H16	GBC2/IO80PDB1
E11	IO34RSB0	G3	NC	H17	IO83PPB1
E12	IO44RSB0	G4	IO222NDB3	H18	IO86PPB1

484-Pin FBGA	
Pin Number	AGL1000 Function
H19	IO87PDB1
H20	VCC
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	VCCIB3
K9	VCC
K10	GND

484-Pin FBGA	
Pin Number	AGL1000 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3

484-Pin FBGA	
Pin Number	AGL1000 Function
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
N17	IO100NPB1	R9	VCCIB2	U1	IO195PDB3
N18	IO102NDB1	R10	VCCIB2	U2	IO195NDB3
N19	IO102PDB1	R11	IO147RSB2	U3	IO194NPB3
N20	NC	R12	IO136RSB2	U4	GEB1/IO189PDB3
N21	IO101NPB1	R13	VCCIB2	U5	GEB0/IO189NDB3
N22	IO103PDB1	R14	VCCIB2	U6	VMV2
P1	NC	R15	VMV2	U7	IO179RSB2
P2	IO199PDB3	R16	IO110NDB1	U8	IO171RSB2
P3	IO199NDB3	R17	GDB1/IO112PPB1	U9	IO165RSB2
P4	IO202NDB3	R18	GDC1/IO111PDB1	U10	IO159RSB2
P5	IO202PDB3	R19	IO107NDB1	U11	IO151RSB2
P6	IO196PPB3	R20	VCC	U12	IO137RSB2
P7	IO193PPB3	R21	IO104NDB1	U13	IO134RSB2
P8	VCCIB3	R22	IO105PDB1	U14	IO128RSB2
P9	GND	T1	IO198PDB3	U15	VMV1
P10	VCC	T2	IO198NDB3	U16	TCK
P11	VCC	T3	NC	U17	VPUMP
P12	VCC	T4	IO194PPB3	U18	TRST
P13	VCC	T5	IO192PPB3	U19	GDA0/IO113NDB1
P14	GND	T6	GEC1/IO190PPB3	U20	NC
P15	VCCIB1	T7	IO192NPB3	U21	IO108NDB1
P16	GDB0/IO112NPB1	T8	GNDQ	U22	IO109PDB1
P17	IO106NDB1	T9	GEA2/IO187RSB2	V1	NC
P18	IO106PDB1	T10	IO161RSB2	V2	NC
P19	IO107PDB1	T11	IO155RSB2	V3	GND
P20	NC	T12	IO141RSB2	V4	GEA1/IO188PDB3
P21	IO104PDB1	T13	IO129RSB2	V5	GEA0/IO188NDB3
P22	IO103NDB1	T14	IO124RSB2	V6	IO184RSB2
R1	NC	T15	GNDQ	V7	GEC2/IO185RSB2
R2	IO197PPB3	T16	IO110PDB1	V8	IO168RSB2
R3	VCC	T17	VJTAG	V9	IO163RSB2
R4	IO197NPB3	T18	GDC0/IO111NDB1	V10	IO157RSB2
R5	IO196NPB3	T19	GDA1/IO113PDB1	V11	IO149RSB2
R6	IO193NPB3	T20	NC	V12	IO143RSB2
R7	GEC0/IO190NPB3	T21	IO108PDB1	V13	IO138RSB2
R8	VMV3	T22	IO105NDB1	V14	IO131RSB2



484-Pin FBGA	
Pin Number	AGL1000 Function
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/IO186RSB 2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND

484-Pin FBGA	
Pin Number	AGL1000 Function
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1



## 4 – Datasheet Information

### List of Changes

The following table lists critical changes that were made in each revision of the IGLOO datasheet.

Revision	Changes	Page
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "IGLOO Device Status" table indicates the status for each device in the device family.	N/A
<b>Revision 18 (Nov 2009)</b>	The version changed to v2.0 for IGLOO datasheet chapters, indicating the datasheet contains information based on final characterization. Please review the datasheet carefully as most tables were updated with new data	N/A
<b>Revision 17 (Sep 2009)</b> Product Brief v1.6	The "Reprogrammable Flash Technology" section was modified to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	"IGLOO Ordering Information" was revised to note that halogen-free packages are available with RoHS-compliant packaging.	III
	Table 1 • I/O Standards Supported is new.	1-7
	The definitions of hot-swap and cold-sparing were added to the "I/Os with Advanced I/O Standards" section.	1-7
<b>Revision 16 (Apr 2009)</b> Product Brief v1.5  DC and Switching Characteristics Advance v0.6	M1AGL400 is no longer offered and was removed from the "IGLOO Devices" product table, "IGLOO Ordering Information", and "Temperature Grade Offerings".	I, III, IV
	The –F speed grade is no longer offered for IGLOO devices. The speed grade column and note regarding –F speed grade were removed from "IGLOO Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	$I_{IL}$ and $I_{IH}$ input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions <sup>4</sup> were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-5 • Package Thermal Resistivities was updated.	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$ , $V_{CC} = 1.425\text{ V}$ ) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$ , $V_{CC} = 1.14\text{ V}$ ) were updated.	2-7

Revision	Changes	Page
<b>Revision 16 (cont'd.)</b>	In <a href="#">Table 2-190 • RAM4K9</a> and <a href="#">Table 2-192 • RAM4K9</a> , the following specifications were removed: $t_{WRO}$ $t_{CCKH}$	2-124 and 2-126
	In <a href="#">Table 2-191 • RAM512X18</a> and <a href="#">Table 2-193 • RAM512X18</a> , the following specifications were removed: $t_{WRO}$ $t_{CCKH}$	2-125 and 2-127
<b>Revision 15 (Feb 2009)</b> Packaging v1.9	The "132-Pin QFN" pin table for the AGL060 device is new.	3-30
<b>Revision 14 (Feb 2009)</b> Product Brief v1.4	The "Advanced I/O" section was revised to include two bullets regarding wide range power supply voltage support.	I
	3.0 V wide range was added to the list of supported voltages in the "I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new.	1-8
<b>Revision 13 (Jan 2009)</b> Packaging v1.8	The "121-Pin CSP" pin table was revised to add a note regarding pins F1 and G1.	3-6
<b>Revision 12 (Dec 2008)</b> Product Brief v1.3  Packaging v1.7	QN48 and QN68 were added to the AGL030 for the following tables: "IGLOO Devices" Product Family Table "IGLOO Ordering Information" "Temperature Grade Offerings"	N/A
	QN132 is fully supported by AGL125 so footnote 3 was removed.	
	The "48-Pin QFP" pin diagram and pin table are new.	3-23
	The "68-Pin QFN" pin table for AGL030 is new.	3-25
	The AGL600 Function for pin K15 in the "484-Pin FBGA" table was changed to VCCIB1.	3-66
<b>Revision 11 (Oct 2008)</b> Product Brief v1.2  DC and Switching Characteristics Advance v0.5  Packaging v1.6	This document was updated to include AGL400 device information. The following sections were updated: "IGLOO Devices" Product Family Table "IGLOO Ordering Information" "Temperature Grade Offerings" <a href="#">Figure 1-2 • IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)</a>	N/A
	The tables in the "Quiescent Supply Current" section were updated with values for AGL400. In addition, the title was updated to include: (VCC = VJTAG = VPP = 0 V).	2-7
	The tables in the "Power Consumption of Various Internal Resources" section were updated with values for AGL400.	2-13
	<a href="#">Table 2-177 • AGL400 Global Resource</a> is new.	2-109
	The "196-Pin CSP" table for the AGL400 device is new.	3-13
	The "144-Pin FBGA" table for the AGL400 device is new.	3-44
	The "256-Pin FBGA" table for the AGL400 device is new.	3-51
	The "484-Pin FBGA" table for the AGL400 device is new.	3-61

Revision	Changes	Page
<b>Revision 10 (Aug 2008)</b>	3.0 V LVCMOS wide range support data was added to <a href="#">Table 2-2 • Recommended Operating Conditions</a> <sup>4</sup> .	2-2
DC and Switching Characteristics Advance v0.4	3.3 V LVCMOS wide range support data was added to <a href="#">Table 2-24 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings</a> to <a href="#">Table 2-26 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings</a> .	2-24 to 2-26
	3.3 V LVCMOS wide range support data was added to <a href="#">Table 2-27 • Summary of Maximum and Minimum DC Input Levels</a> .	2-27
	3.3 V LVCMOS wide range support text was added to <a href="#">Table 2-49 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range</a> .	2-39
	<a href="#">Table 2-49 • Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range</a> is new.	2-39
<b>Revision 9 (Jul 2008)</b> Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
<b>Revision 8 (Jun 2008)</b>  DC and Switching Characteristics Advance v0.2	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather than simulation values. AGL015 global clock delays have been added.	N/A
	<a href="#">Table 2-1 • Absolute Maximum Ratings</a> was updated to combine the VCCI and VMV parameters in one row. The word "output" from the parameter description for VCCI and VMV, and table note 3 was added.	2-1
	<a href="#">Table 2-2 • Recommended Operating Conditions</a> <sup>4</sup> was updated to add references to tables notes 4, 6, 7, and 8. VMV was added to the VCCI parameter row, and table note 9 was added.	2-2
	In <a href="#">Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature</a> <sup>1</sup> , the maximum operating junction temperature was changed from 110° to 100°.	2-2
	VMV was removed from <a href="#">Table 2-4 • Overshoot and Undershoot Limits</a> 1. The table title was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	<a href="#">Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels</a> is new.	2-5

Revision	Changes	Page
<b>Revision 8 (cont'd)</b>	EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-8 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode*, Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*, and Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode.	2-7
	Note 2 of Table 2-11 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode1 was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.	2-9
	Table 2-12 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, and Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings <sup>1</sup> were updated to change PDC2 to PDC6 and PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI.	2-10 through 2-11
	In Table 2-18 • Different Components Contributing to Dynamic Power Consumption in IGLOO Devices, the description for PAC13 was changed from Static to Dynamic.	2-13
	Table 2-19 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-21 • Different Components Contributing to the Static Power Consumption in IGLOO Device were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power. Subtitles were added to indicate type of devices and core supply voltage.	2-14, 2-16
	The "Total Static Power Consumption—P <sub>STAT</sub> " section was updated to revise the calculation of P <sub>STAT</sub> , including PDC6 and PDC7.	2-17
	Footnote 1 was updated to include information about PAC13. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$ .	2-18
<b>Revision 7 (Jun 2008)</b> Packaging v1.5	The "132-Pin QFN" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	3-27
<b>Revision 6 (Jun 2008)</b> Packaging v1.4	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	Pin numbers were added to the "68-Pin QFN" package diagram. Note 2 was added below the diagram.	3-24
<b>Revision 5 (Mar 2008)</b> Packaging v1.3	The "196-Pin CSP" package and pin table was added for AGL250.	3-11

Revision	Changes	Page
<b>Revision 4 (Mar 2008)</b> Product Brief v1.0	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 12 $\mu$ W)" was removed from "Low Power Active FPGA Operation."  1.2_V was added to the list of core and I/O voltages in the "Advanced I/O" and "I/Os with Advanced I/O Standards" section sections.	I  I, 1-7
	The "Embedded Memory" section was updated to remove the footnote reference from the section heading and place it instead after "4,608-Bit" and "True Dual-Port SRAM (except $\times$ 18)."	I
<b>Revision 3 (Feb 2008)</b> Product Brief rev. 2          Packaging v1.2	This document was updated to include AGL015 device information. QN68 is a new package offered in the AGL015. The following sections were updated: "Features and Benefits" "IGLOO Ordering Information" "Temperature Grade Offerings" "IGLOO Devices" Product Family Table Table 1 • IGLOO FPGAs Package Sizes Dimensions "AGL015 and AGL030" note	N/A
	The "Temperature Grade Offerings" table was updated to include M1AGL600.	IV
	In the "IGLOO Ordering Information" table, the QN package measurements were updated to include both 0.4 mm and 0.5 mm.	III
	In the "General Description" section, the number of I/Os was updated from 288 to 300.	1-1
	The "68-Pin QFN" section is new.	3-24
	<b>Revision 2 (Jan 2008)</b> Packaging v1.1	The "196-Pin CSP" package and pin table was added for AGL125.
<b>Revision 1 (Jan 2008)</b> Product Brief rev. 1	The "Low Power" section was updated to change the description of low power active FPGA operation to "from 12 $\mu$ W" from "from 25 $\mu$ W." The same update was made in the "General Description" section and the "Flash*Freeze Technology" section.	I, 1-1
<b>Revision 0 (Jan 2008)</b>	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the numbering.	N/A
Advance v0.7 (December 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the Temperature Grade Offerings table were updated to reflect the following: CS196 is now supported for AGL250; device/package support for QN132 is to be determined for AGL250; the CS281 package was added for AGL600 and AGL1000.	i, ii, iv
	Table 2 • IGLOO FPGAs Package Sizes Dimensions is new, and package sizes were removed from the "I/Os Per Package1" table.	ii
	The "I/Os Per Package1" table was updated to reflect 77 instead of 79 single-ended I/Os for the VG100 package for AGL030.	ii
	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-20
	In Table 2-26 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings, $T_J$ was changed to $T_A$ in notes 1 and 2.	2-26
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A

Revision	Changes	Page
Advance v0.7 (continued)	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-74
	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1.	N/A
	Table 2-4 • IGLOO CCC/PLL Specification and Table 2-5 • IGLOO CCC/PLL Specification were updated.	2-19, 2-20
	The former Table 2-16 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in IGLOO Devices (maximum drive strength and high slew selected) was removed.	N/A
	The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core.	2-57
	Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent) was updated to add UC81 and CS281. Flash*Freeze pins were assigned for CS81, CS121, and CS196.	2-61
	Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal.	2-55
	Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section.	3-6
	Table 3-8 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics, IGLOO Flash*Freeze Mode <sup>†</sup> was updated.	3-6
	Table 3-9 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics, IGLOO Sleep Mode ( $V_{CC} = 0 V$ ) <sup>†</sup> was updated.	3-6
	Table 3-11 • Quiescent Supply Current ( $I_{DD}$ ), No IGLOO Flash*Freeze Mode <sup>1</sup> was updated.	3-7
	Table 3-115 • Minimum and Maximum DC Input and Output Levels was updated.	3-58
	Table 3-156 • JTAG 1532 was updated and Table 3-155 • JTAG 1532 is new.	3-104
	The "121-Pin CSP" and "281-Pin CSP" packages are new.	4-5, 4-7
	The "81-Pin CSP" table for the AGL030 device was updated to change the G6 pin function to IO44RSB1 and the JG pin function to IO45RSB1.	4-4
	The "121-Pin CSP" table for the AGL060 device is new.	4-6
	The "256-Pin FBGA" table for the AGL1000 device is new.	4-34
	The "281-Pin CSP" table for the AGL 600 device is new.	4-8
	The "100-Pin VQFP" table for the AGL060 device is new.	4-18
	The "144-Pin FBGA" table for the AGL250 device is new.	4-24
The "144-Pin FBGA" table for the AGL1000 device is new.	4-28	
The "484-Pin FBGA" table for the AGL600 device is new.	4-38	
The "484-Pin FBGA" table for the AGL1000 device is new.	4-43	



Revision	Changes	Page
Advance v0.6 (November 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the "IGLOO Ordering Information", and the Temperature Grade Offerings table were updated to add the UC81 package.	i, ii, iii, iv
	The "81-Pin $\mu$ CSP" table for the AGL030 device is new.	4-3
	The "81-Pin CSP" table for the AGL030 device is new.	4-1
Advance v0.5 (September 2007)	Table 1 • IGLOO Product Family was updated for AGL030 in the Package Pins section to change CS181 to CS81.	i
Advance v0.4 (September 2007)	Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
	The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table.	ii
	The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating.	2-51
Advance v0.3 (August 2007)	In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	i
	The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	ii
	The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	iv
	The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent).	2-61
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv
	The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$ , ambient temperature, and table notes 4–6 were added.	3-2

## Datasheet Categories

### **Categories**

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO Device Status" table, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### **Advance**

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

#### **Preliminary**

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

#### **Unmarked (production)**

This version contains information that is considered to be final.

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