High-Voltage, Current-Mode PWM Controller

Features

- 10 to 450V input voltage range
- <1.3mA supply current
- >1.0MHz clock
- >20:1 dynamic range @ 500KHz
- 49% Maximum duty cycle version
- Low internal noise

Applications

- Off-line high frequency power supplies
- Universal input power supplies
- High density power supplies
- Very high efficiency power supplies
- Extra wide load range power supplies

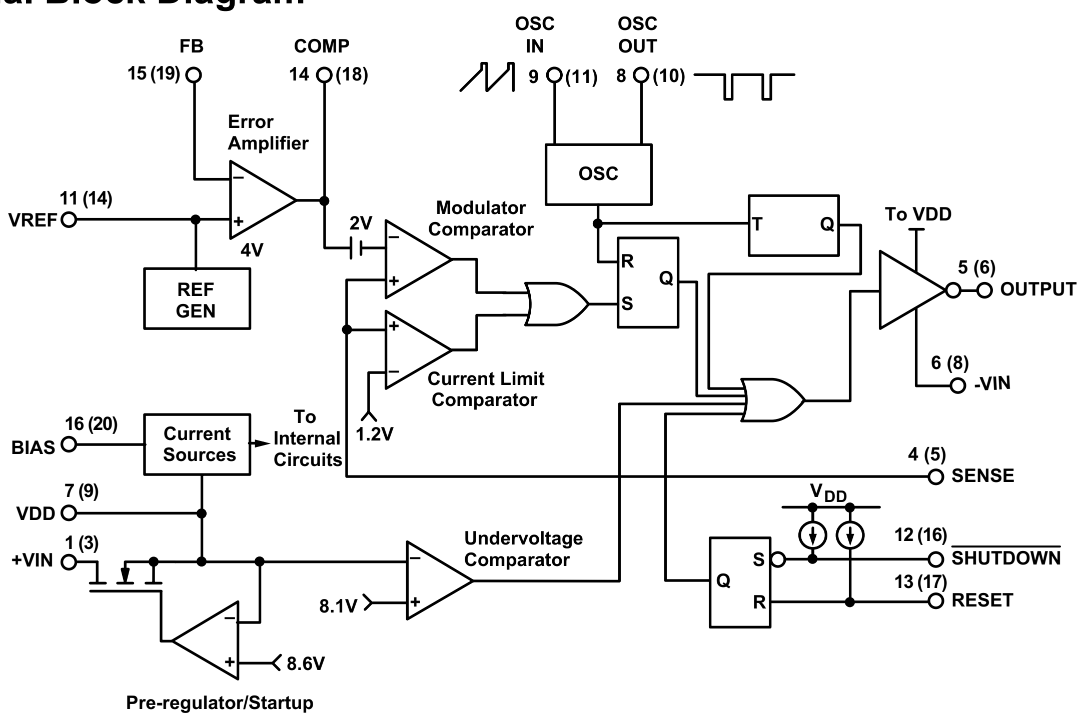
General Description

The Supertex HV9120 is a Switch Mode Power Supply (SMPS) controller subsystem that can start and run directly from almost any DC input, from a 12V battery to a rectified and filtered 240V AC line. It contains all the elements required to build a single-switch converter except for the switch, magnetic assembly, output rectifier(s) and filter(s).

A unique input circuit allows the 9120 to self-start directly from a high voltage input, and subsequently take the power to operate from one of the outputs of the converter it is controlling, allowing very efficient operation while maintaining input-to-output galvanic isolation limited in voltage only by the insulation system of the associated magnetic assembly. A ±2% internal bandgap reference, internal operational amplifier, very high speed comparator, and output buffer allow production of rugged, high performance, high efficiency power supplies of 50W or more, which can still be over 80% efficient at outputs of 1.0W or less. The wide dynamic range of the controller system allows designs with extremely wide line and load variations with much less difficulty and much higher efficiency than usual. The exceptionally wide input voltage range also allows better usage of energy stored in input dropout capacitors than with other PWM ICs. Remote on/off controls allow either latching or nonlatching remote shutdown. During shutdown, the power required is under 6.0mW.

For detailed circuit and application information, please refer to application notes AN-H13 and AN-H21 to AN-H24.

Functional Block Diagram



Note:
Pin numbers in parentheses are for PLCC package.

Ordering Information

Device	Package Options		
	16-Lead SOIC *9.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*	**16-Lead PDIP** *.790x.250in body* *.210in height (max)* *.100in pitch*	**20-Lead PLCC** *.353x.353in body* *.180in height (max)* *.050in pitch*
HV9120	HV9120NG-G	HV9120P-G	HV9120PJ-G

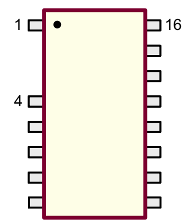
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

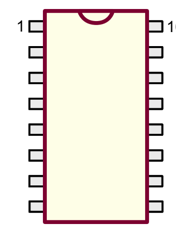
Parameter	Value
Input voltage, $+V_{IN}$	450V
Device supply voltage, V_{DD}	15.5V
Logic input voltage	-0.3V to V_{DD} +0.3V
Linear input voltage	-0.3V to V_{DD} +0.3V
Pre regulator input current (continuous), I_{IN}	2.5mA
Operating junction temperature, T_J	150°C
Storage temperature	-65 to +150°C
Power dissipation:	
16-Lead SOIC	900mW
16-Lead PDIP	1000mW
20-Lead PLCC	1400mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. ***Voltages are referenced to $-V_{IN}$.***

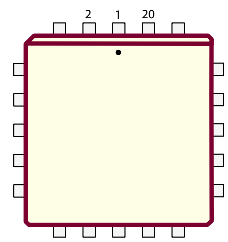
Pin Configurations



16-Lead SOIC (NG)

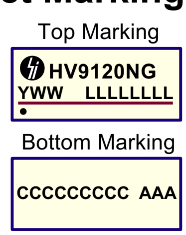


16-Lead PDIP (P)



20-Lead PLCC (PJ)

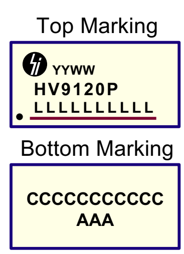
Product Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging

**May be part of top marking*

16-Lead SOIC (NG)



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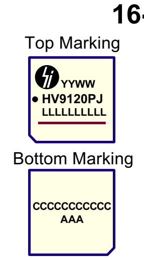
**May be part of top marking*

16-Lead PDIP (P)



YY = Year Sealed
WW = Week Sealed
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____ = "Green" Packaging

**May be part of top marking*

20-Lead PLCC (PJ)

Electrical Characteristics

(Unless otherwise specified, V_{DD} = 10V, +V_{IN} = 48V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

Sym	Parameter	#	Min	Typ	Max	Units	Conditions
Reference							
V_{REF}	Output voltage	-	3.92	4.00	4.08	V	R_L = 10MΩ
			3.84	4.00	4.16		R_L = 10MΩ, T_A = -55 to 125°C
Z_{OUT}	Output impedance	#	15	30	45	KΩ	---
I_{SHORT}	Short circuit current	-	-	125	250	µA	V_{REF} = -V_{IN}
ΔV_{REF}	Change in V_{REF} with temperature	#	-	0.25	-	mV/°C	T_A = -55 to 125°C
Oscillator							
f_{MAX}	Oscillator frequency	-	1.0	3.0	-	MHz	R_{OSC} = 0Ω
f_{OSC}	Initial accuracy[1]	-	80	100	120	KHz	R_{OSC} = 330KΩ
		-	160	200	240		R_{OSC} = 150KΩ
ΔV_{OSC}	Voltage stability	-	-	-	15	%	9.5V < V_{DD} < 13.5V
TC_{OSC}	Temperature coefficient	#	-	170	-	ppm/°C	T_A = -55 to 125°C
PWM							
D_{MAX}	Maximum duty cycle	#	49.0	49.4	49.6	%	---
D_{MIN}	Minimum duty cycle	-	-	-	0	%	---
	Maximum pulse width before pulse drops out	#	-	80	125	ns	---
Current Limit							
V_{LIM}	Maximum input signal	-	1.0	1.2	1.4	V	V_{FB} = 0V
t_D	Delay to output	#	-	80	120	ns	V_{SENSE} = 1.5V, V_{COMP} ≤ 2.0V
Error Amplifier							
V_{FB}	Feedback voltage	-	3.92	4.00	4.08	V	V_{FB} shorted to COMP
I_{IN}	Input bias current	-	-	25	500	nA	V_{FB} = 4.0V
V_{OS}	Input offset voltage	-	nulled during trim			-	---
A_{VOL}	Open loop voltage gain	#	60	80	-	dB	---
GB	Unity gain bandwidth	#	1.0	1.3	-	MHz	---
Z_{OUT}	Out impedance	#	see Fig. 1			Ω	---
I_{SOURCE}	Output source current	-	-1.4	-2.0	-	mA	V_{FB} = 3.4V
I_{SINK}	Output sink current	-	0.12	0.15	-	mA	V_{FB} = 4.5V
PSRR	Power supply rejection	#	see Fig. 2			dB	---

Notes:

 # Guaranteed by design.

1. Stray capacitance on OSC In pin must be ≤5pF.

Electrical Characteristics *(cont.)*

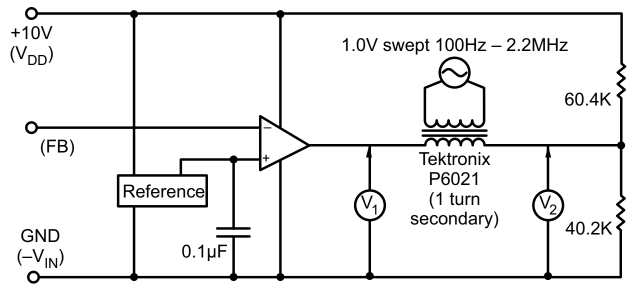
(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ, T_A = 25°C.)

Sym	Parameter	#	Min	Typ	Max	Units	Conditions
Pre-Regulator/Startup							
$+V_{IN}$	Input voltage	-	10	-	450	V	I_{IN} < 10µA; V_{CC} > 9.4V
$+I_{IN}$	Input leakage current	-	-	-	10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} pre-regulator turn-off threshold voltage	-	8.0	8.7	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage lockout	-	7.0	8.1	8.9	V	---
Supply							
I_{DD}	Supply current	-	-	0.75	1.3	mA	C_L < 75pF
I_Q	Quiescent supply current	-	-	0.55	-	mA	$\overline{SHUTDOWN}$ = $-V_{IN}$
I_{BIAS}	Nominal bias current	-	-	20	-	µA	---
V_{DD}	Operating range	-	9.0	-	13.5	V	---
Shutdown Logic							
t_{SD}	$\overline{SHUTDOWN}$ delay	#	-	50	100	ns	C_L = 500pF, V_{SENSE} = $-V_{IN}$
t_{SW}	$\overline{SHUTDOWN}$ pulse width	#	50	-	-	ns	
t_{RW}	RESET pulse width	#	50	-	-	ns	---
t_{LW}	Latching pulse width	#	25	-	-	ns	$\overline{SHUTDOWN}$ and RESET low
V_{IL}	Input low voltage	-	-	-	2.0	V	---
V_{IH}	Input high voltage	-	7.0	-	-	V	---
I_{IH}	Input current, input high voltage	-	-	1.0	5.0	µA	V_{IN} = V_{DD}
I_{IL}	Input current, input low voltage	-	-	-25	-35	µA	V_{IN} = 0V
Output							
V_{OH}	Output high voltage	-	V_{DD} -0.25	-	-	V	I_{OUT} = 10mA
		-	V_{DD} -0.3	-	-	V	I_{OUT} = 10mA, T_A = -55 to 125°C
V_{OL}	Output low voltage	-	-	-	0.2	V	I_{OUT} = -10mA
		-	-	-	0.3	V	I_{OUT} = -10mA, T_A = -55 to 125°C
R_{OUT}	Output resistance, Pull up	-	-	15	25	Ω	I_{OUT} = ±10mA
	Pull down	-	-	8.0	20	Ω	
	Pull up	-	-	20	30	Ω	I_{OUT} = ±10mA, T_A = -55 to 125°C
	Pull down	-	-	10	30	Ω	
t_R	Rise time	#	-	30	75	ns	C_L = 500pF
t_F	Fall time	#	-	20	75	ns	C_L = 500pF

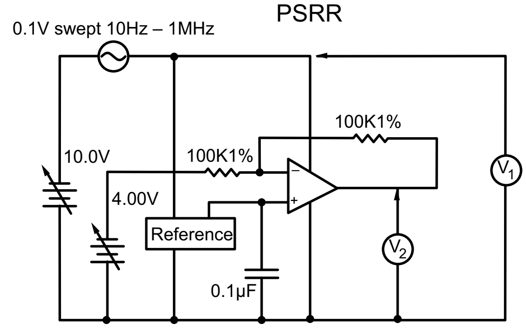
Note:
 # Guaranteed by design.

Test Circuits

Error Amp Z_{OUT}



PSRR



Note:

Set feedback voltage so that $V_{COMP} = V_{DIVIDE} \pm 1.0mV$ before connecting transformer.

Detailed Description

Pre regulator

The pre regulator/startup circuit for the HV9120 consists of a high-voltage n-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the VIN terminal and the VDD terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling), no current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between VDD and VSS is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the VDD supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the effective gate capacitance of the MOSFET being driven, i.e.,

$C_{STORAGE} \geq 100$ x (gate charge of FET at 10V)

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytic capacitors are generally not suitable. A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and VSS is required by the HV9120 to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390 to 510KΩ resistor if a 10V V_{DD} is used, or a 510 to 680KΩ resistor if V_{DD} will be 12V. A precision resistor is not required; ±5% is fine.

Clock Oscillator

The clock oscillator of the HV9120 consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and a frequency dividing flip-flop. A single external resistor between the OSC IN and OSC OUT pins is required to set oscillator frequency (see graph).

One difference exists between the Supertex HV9120 and competitive 9120s: The oscillator is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I-430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The Reference of the HV9120 consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier, when connected in a gain of -1 configuration, is as close to 4.0V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4.0V, the feedback voltage required for proper regulation will be.

A ≈ 50KΩ resistor is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6.0V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required. In general, because the reference voltage of the Supertex HV9120 is not noisy, as some previous examples have been, overriding the reference should seldom be necessary.

Because the reference of the HV9120 is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and VSS is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Error Amplifier

The error amplifier in the HV9120 is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV9120 uses a true dual-comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

Remote Shutdown

The shutdown and reset pins of the HV9120 can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used, they should be left open, or connected to VDD.

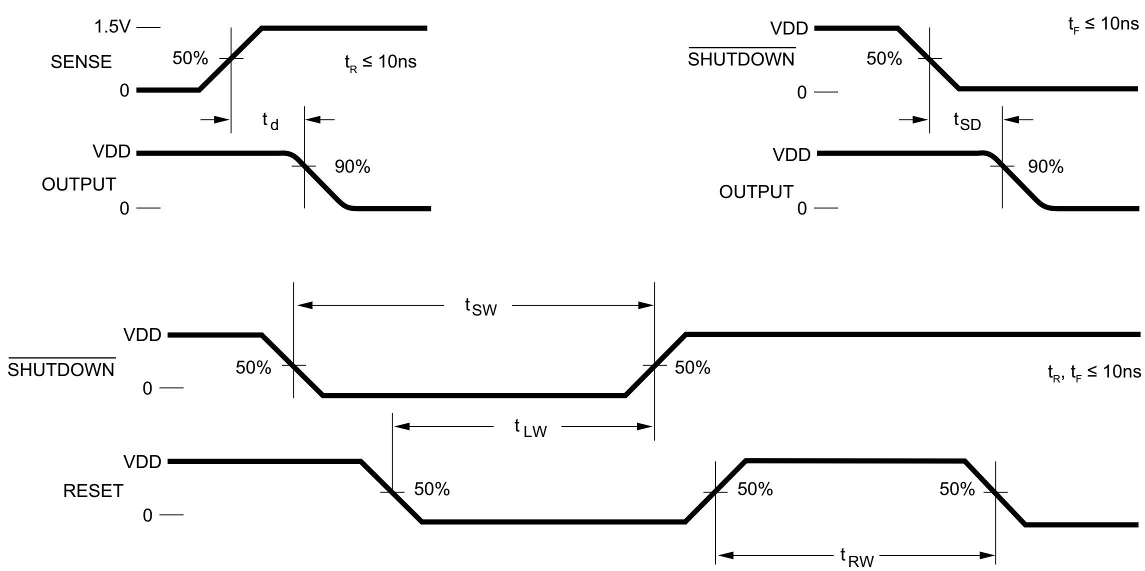
Output Buffer

The output buffer of the HV9120 is of standard CMOS construc-tion (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

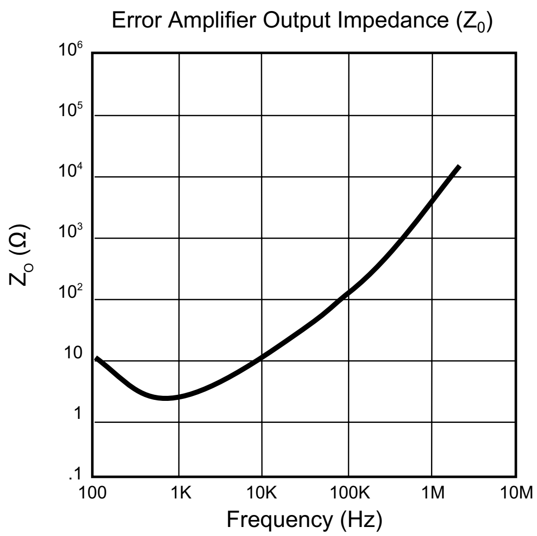
Truth Table

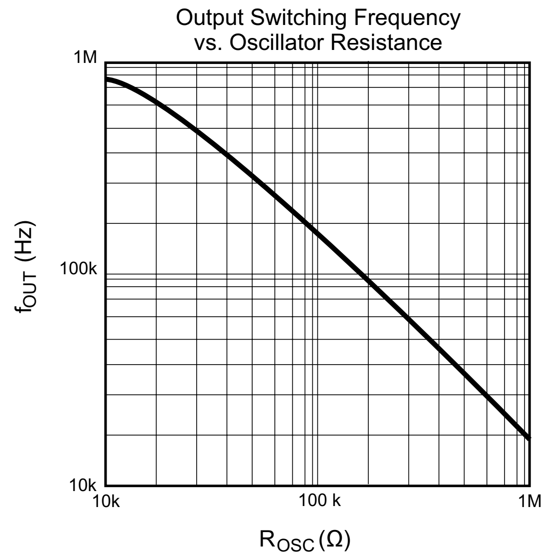
$\overline{\text{SHUTDOWN}}$	RESET	Output
H	H	Normal operation
H	H → L	Normal operation, no change
L	H	Off, not latched
L	L	Off, latched
L → H	L	Off, latched, no change

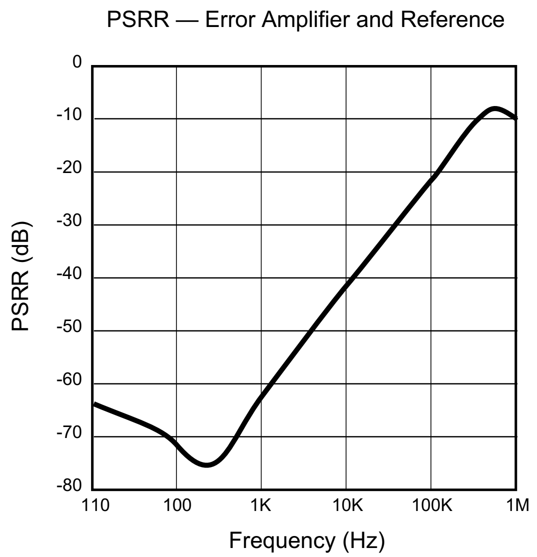
Shutdown Timing Waveforms

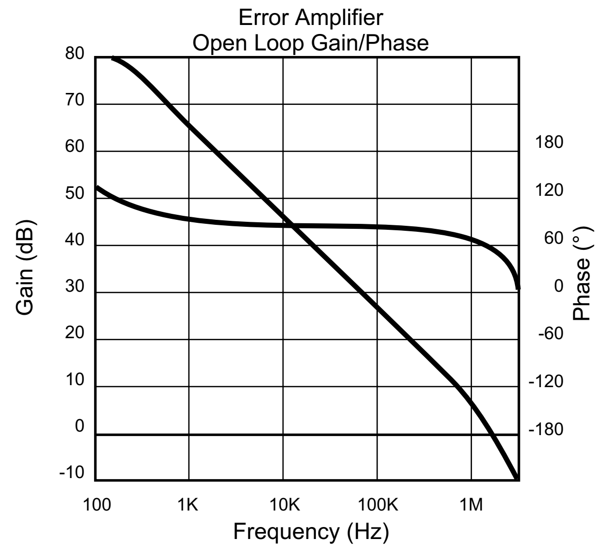


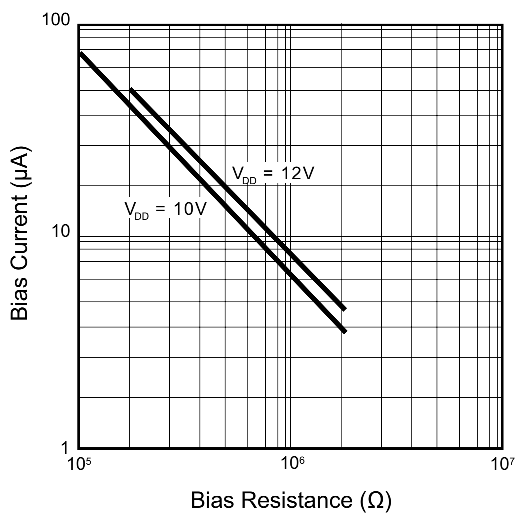
Typical Performance Curves











Pin Descriptions

16-Lead SOIC (NG)

Pin #	Description
1	+VIN
2	-
3	-
4	SENSE
5	OUTPUT
6	-VIN
7	VDD
8	OSC OUT

Pin #	Description
9	OSC IN
10	NC
11	VREF
12	$\overline{\text{SHUTDOWN}}$
13	RESET
14	COMP
15	FB
16	BIAS

16-Lead PDIP (P)

Pin #	Description
1	+VIN
2	NC
3	NC
4	SENSE
5	OUTPUT
6	-VIN
7	VDD
8	OSC OUT

Pin #	Description
9	OSC IN
10	NC
11	VREF
12	$\overline{\text{SHUTDOWN}}$
13	RESET
14	COMP
15	FB
16	BIAS

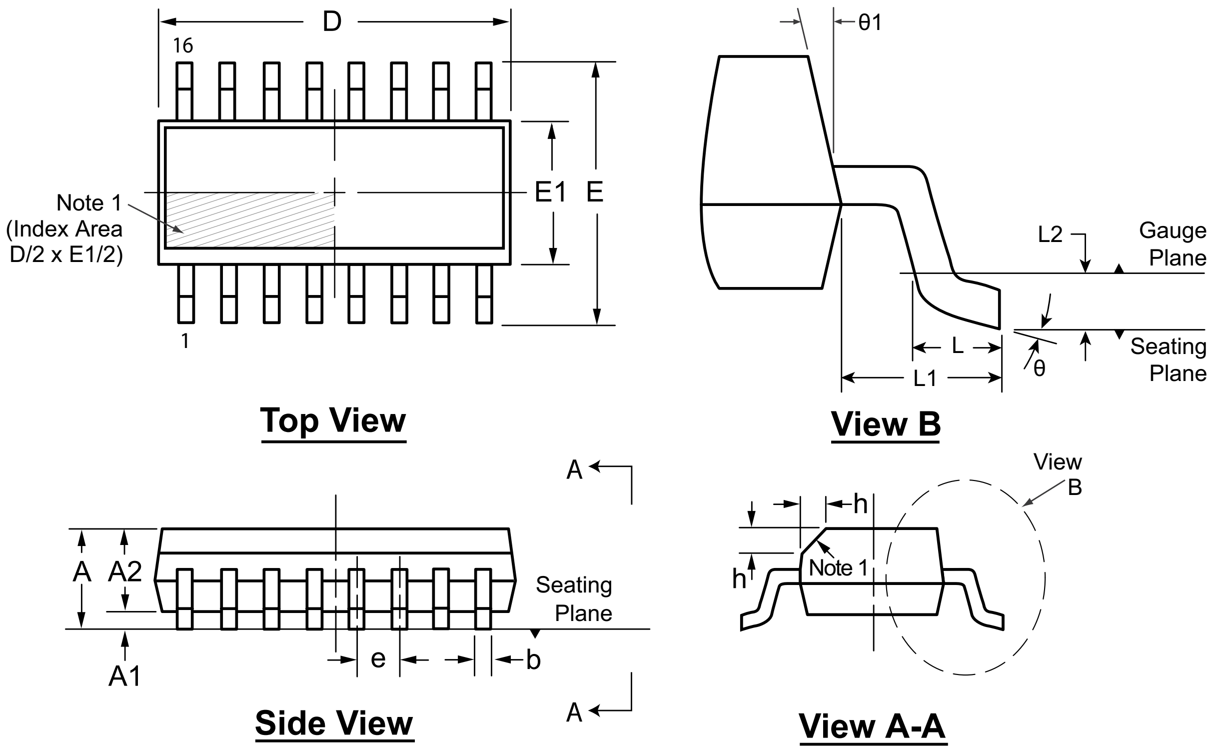
20-Lead PLCC (PJ)

Pin #	Description
1	NC
2	NC
3	+VIN
4	NC
5	SENSE
6	OUTPUT
7	NC
8	-VIN
9	VDD
10	OSC OUT

Pin #	Description
11	OSC IN
12	NC
13	NC
14	VREF
15	NC
16	$\overline{\text{SHUTDOWN}}$
17	RESET
18	COMP
19	FB
20	BIAS

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

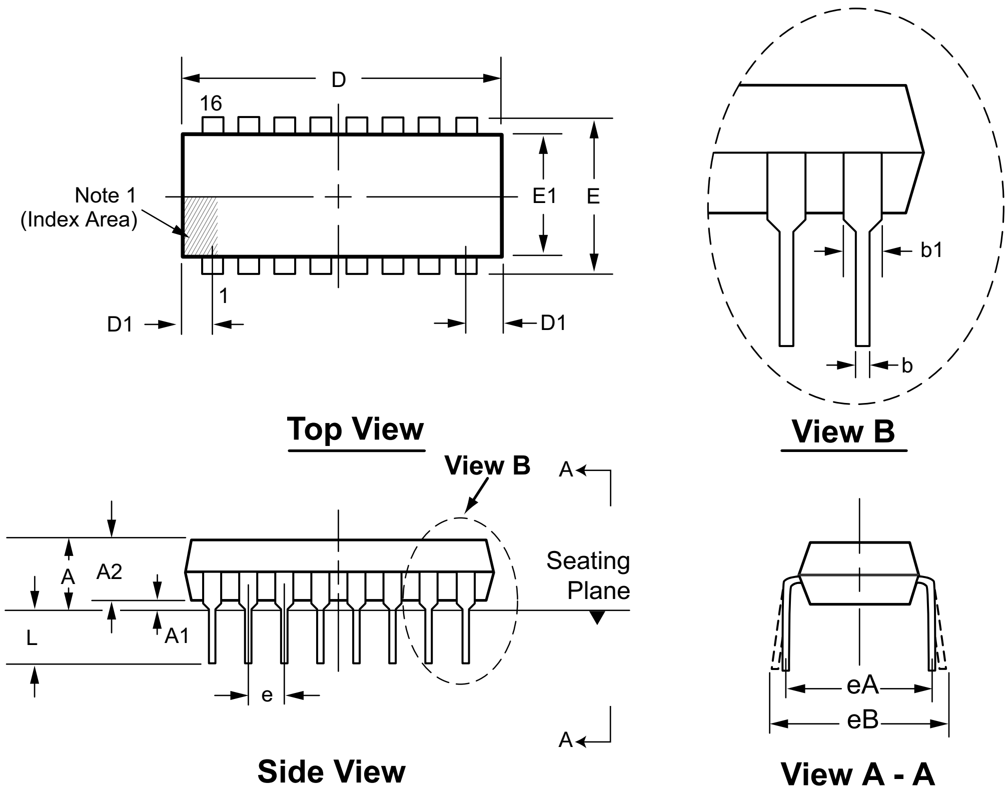
1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-16SONG, Version F101708.*

16-Lead PDIP (.300in Row Spacing) Package Outline (P)

.790x.250in body, .210in height (max), .100in pitch



Note:

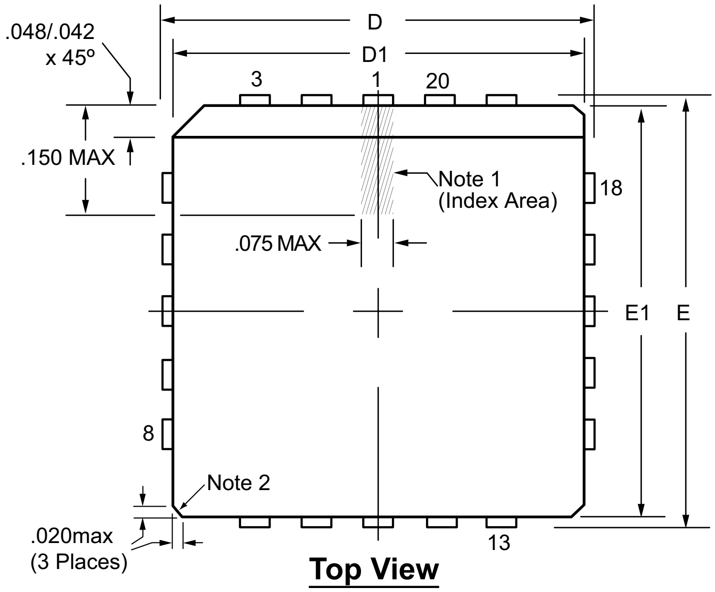
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	eA	eB	L
Dimension (inches)	MIN	.130*	.015	.115	.014	.045	.780	.005	.290†	.240	.100 BSC	.300 BSC	.300*	.115
	NOM	-	-	.130	.018	.060	.790	-	.310	.250			-	.130
	MAX	.210	.035*	.195	.023†	.070	.810†	.050*	.325	.280			.430	.150

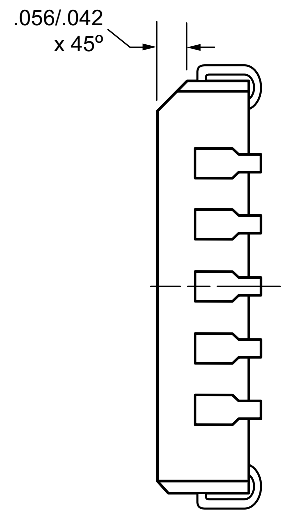
JEDEC Registration MS-001, Variation AB, Issue D, June, 1993.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
† This dimension is a non-JEDEC dimension.
Drawings not to scale.
***Supertex Doc. #:** DSPD-16DIPP, Version A120108.*

20-Lead PLCC Package Outline (PJ)

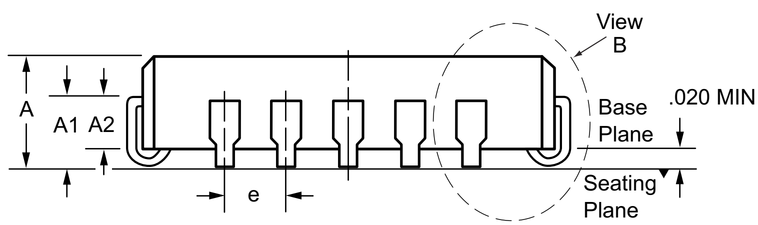
.353x.353in body, .180in height (max), .050in pitch



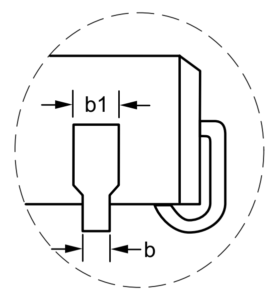
Top View



Vertical Side View



Horizontal Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.385	.350	.385	.350	.050 BSC
	NOM	.172	.105	-	-	-	.390	.353	.390	.353	
	MAX	.180	.120	.083	.021	.032	.395	.356	.395	.356	

JEDEC Registration MS-018, Variation AA, Issue A, June, 1993.
Drawings not to scale.
***Supertex Doc. #:** DSPD-20PLCCPJ, Version B092408*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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