19-5707; Rev 0; 12/10

EVALUATION KIT AVAILABLE

Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

MAX14886

General Description

The MAX14886 high-speed, low-skew, active redriver multiplexer is ideal for switching between outputs of dual-graphics systems and signal conditioning to meet HDMI™ v.1.4 compliance up to 2.25Gbps at an external HDMI connector. It is used for switching between integrated (e.g., Intel or AMD) and discrete graphics (e.g., NVIDIA or ATI GPU). The device is VESA DisplayPort™ Interoperability Guideline v.1.1a-compliant (requires external DDC logic) and integrates seamlessly with an external HDMI connector on the motherboard.

The device accommodates differential inputs as low as 200mV and drives transition minimized differential signaling (TMDS®) outputs to 1000mV (typ). A precision resistor on the output level adjust pin (ADJ) allows differentiated output back-termination resistors of 400Ω (typ) to better meet HDMI mask jitter compliance, while maintaining full TMDS swing requirements. The device supports AC-(DisplayPort) or DC-(HDMI) coupling directly to the graphics IC and must be DC-coupled to the HDMI connector. In addition, the device features current backflow protection at the HDMI connector and a low-power, active-high or active-low shutdown mode.

The device operates with a single +3.3V supply, is specified over the 0°C to +70°C commercial temperature range, and is available in a 5mm x 5mm, 40-pin TQFN package.

Applications

Dual Graphics Notebook Computers

Dual Mode DisplayPort to HDMI External Switches or Adapters

Features

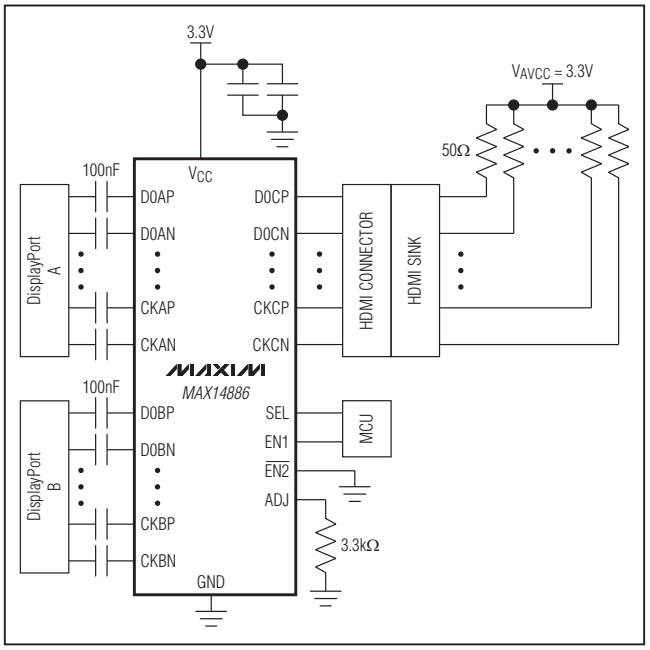
- **Single +3.3V Supply**
- **Meets HDMI v.1.4 Eye Mask Up to 2.25Gbps**
- **Meets VESA DisplayPort Interoperability Guideline v.1.1a (Requires External DDC Logic)**
- **Low-Power Shutdown Mode**
  Active High or Active Low
- **Output Level Adjust (ADJ) for Output Back-Termination Without Amplitude Loss**
- **Seamless Integration into Dual-Graphics Systems with External HDMI Connector**
  DC-Coupled HDMI Outputs Mate Directly to HDMI Connector
  AC- or DC-Coupled TMDS-Formatted Inputs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14886CTL+	0°C to +70°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



HDMI is a trademark of HDMI Licensing, LLC.

DisplayPort is a trademark of Video Electronics Standards Association (VESA).

TMDS is a registered trademark of Silicon Image, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} ..... -0.3V to +4.0V
EN1, $\overline{EN2}$, SEL, ADJ ..... -0.3V to (V_{CC} + 0.3V)
D_CP, D_CN, CKCP, CKCN Short-Circuit
Output Current ..... ±30mA
All Other Pins Short-Circuit Current ..... ±5mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 45°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2°C/W

Note 1: Package thermal resistances were obtained using method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V, T_A = 0°C to +70°C, R_{ADJ} = 3.3kΩ, C_{CL} = 100nF, typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Supply Voltage	V_{CC}		3		3.6	V
Supply Current	I_{CC}	EN1 = high, $\overline{EN2}$ = low			52.5	mA
Total Supply Current	I_{GND}	50Ω termination to AVCC, V_{AVCC} = +3.3V (Note 3)			105	mA
Shutdown Supply Current	I_{SHUT}	EN1 = low or $\overline{EN2}$ = high			100	µA
Single-Ended Input Termination Resistance	R_{IN}	DC	40		60	Ω
Single-Ended Output Voltage High	V_{OH}	DC, V_{AVCC} = +3.3V (Notes 3, 4)	V_{AVCC} - 0.01		V_{AVCC} + 0.01	V
Single-Ended Output Voltage Low	V_{OL}	DC, V_{AVCC} = +3.3V (Notes 3, 4)	V_{AVCC} - 0.6		V_{AVCC} - 0.45	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V, T_A = 0°C to +70°C, R_{ADJ} = 3.3kΩ, C_{CL} = 100nF, typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Differential Input Return Loss	SDD11	150MHz ≤ f ≤ 1.25GHz			-8	dB
Input Frequency Range	f_{IN}	Clock	25		225	MHz
		Data	225		1125	
Differential Input Range	V_{IDIFF}		200		1600	mV
Differential Output Voltage	V_{ODIFF}	50Ω single termination	900		1250	mV
Output Rise/Fall Time	$t_{R/F}$	20% to 80%, 2.25Gbps			80	ps
Deterministic Jitter	t_{DJ}	K28.5 pattern, up to 2.25Gbps (Note 4)			0.04	UI
Random Jitter	t_{RJ}	D10.2 pattern, 2.25Gbps (Note 4)			1.1	ps_{RMS}
Lane-to-Lane Skew	t_{SK}			50		ps
Propagation Delay	t_{PD}			250		ps
CONTROL LOGIC (EN1, $\overline{EN2}$, SEL)						
Input Logic-Low Voltage	V_{IL}				0.6	V
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic Hysteresis	V_{HYST}			50		mV
Input Pulldown/Pullup Resistor	R_{IPULL}			400		kΩ
Shutdown Recovery Time	t_{SHUT}			20		µs
TMDS Mux Switching Time	t_{MUX}			50		ns
ESD PROTECTION						
All Pins		Human Body Model		±8		kV

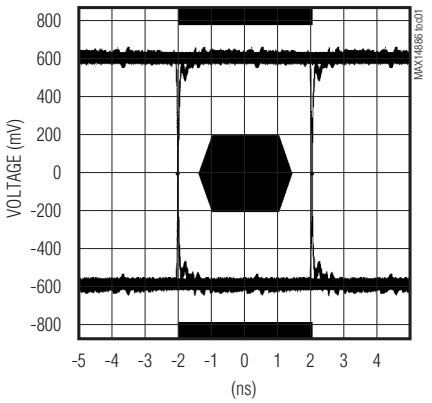
Note 2: All units are production tested at T_A = +70°C. Specifications over temperature are guaranteed by design.
Note 3: AVCC is an external supply.
Note 4: Guaranteed by design; not production tested.

Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

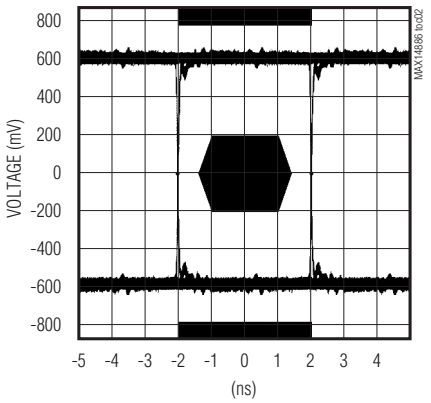
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, R_{ADJ} = 3.3kΩ, unless otherwise noted.)

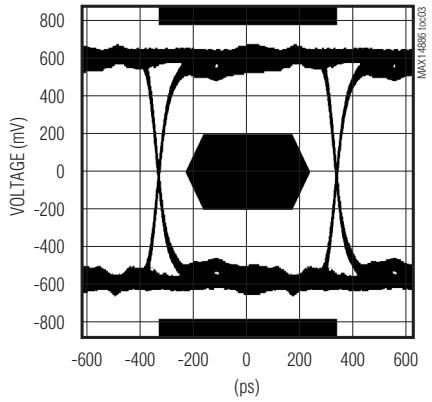
EYE DIAGRAM, V_{IN} = 1600mV$_{P-P}$, 250Mbps, NO BACK TERMINATION, 25MHz CLOCK, 640 x 480, 8-BIT COLOR, 60Hz



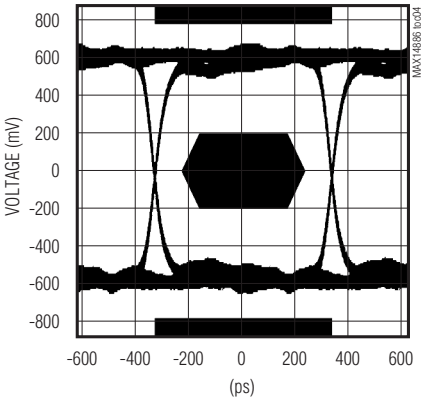
EYE DIAGRAM, V_{IN} = 200mV$_{P-P}$, 250Mbps, NO BACK TERMINATION, 25MHz CLOCK, 640 x 480, 8-BIT COLOR, 60Hz



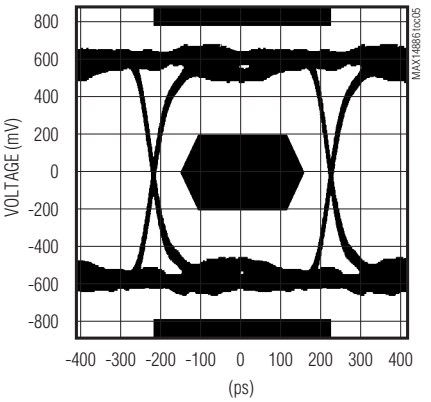
EYE DIAGRAM, V_{IN} = 1600mV$_{P-P}$, 1.5Gbps, NO BACK TERMINATION, 150MHz CLOCK



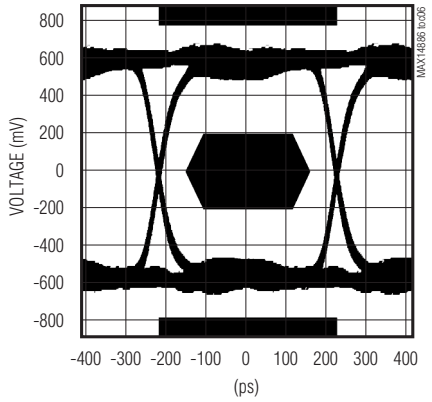
EYE DIAGRAM, V_{IN} = 200mV$_{P-P}$, 1.5Gbps, NO BACK TERMINATION, 1080p, 8-BIT COLOR, 60Hz



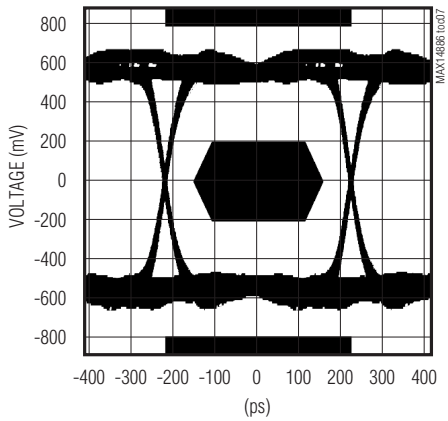
EYE DIAGRAM, V_{IN} = 1600mV$_{P-P}$, 2.25Gbps, NO BACK TERMINATION



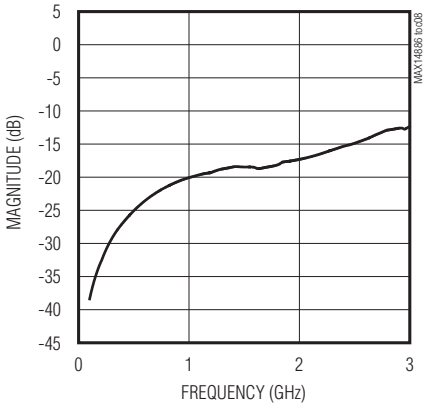
EYE DIAGRAM, V_{IN} = 200mV$_{P-P}$, 2.25Gbps, NO BACK TERMINATION, 225MHz CLOCK, 1080p, 12-BIT COLOR, 60Hz



EYE DIAGRAM, V_{IN} = 200mV$_{P-P}$, 2.25Gbps, 400Ω BACK TERMINATION, RSET = 3kΩ, FIGURE 1

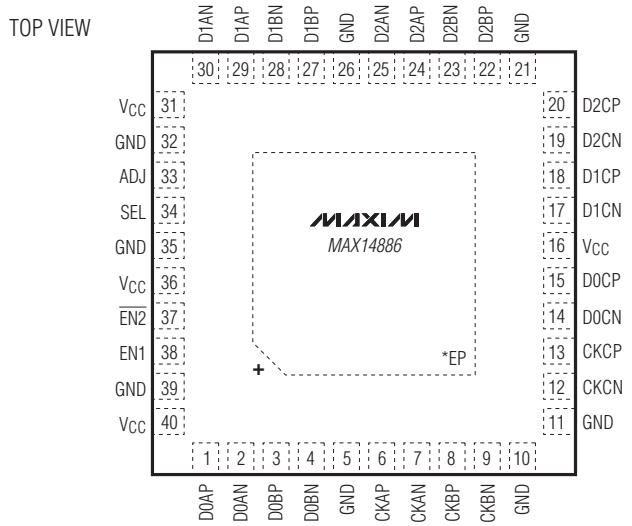


DIFFERENTIAL INPUT RETURN LOSS vs. FREQUENCY



Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

Pin Configuration



TQFN
(5mm × 5mm × 0.75mm)

*CONNECT EP TO GND.

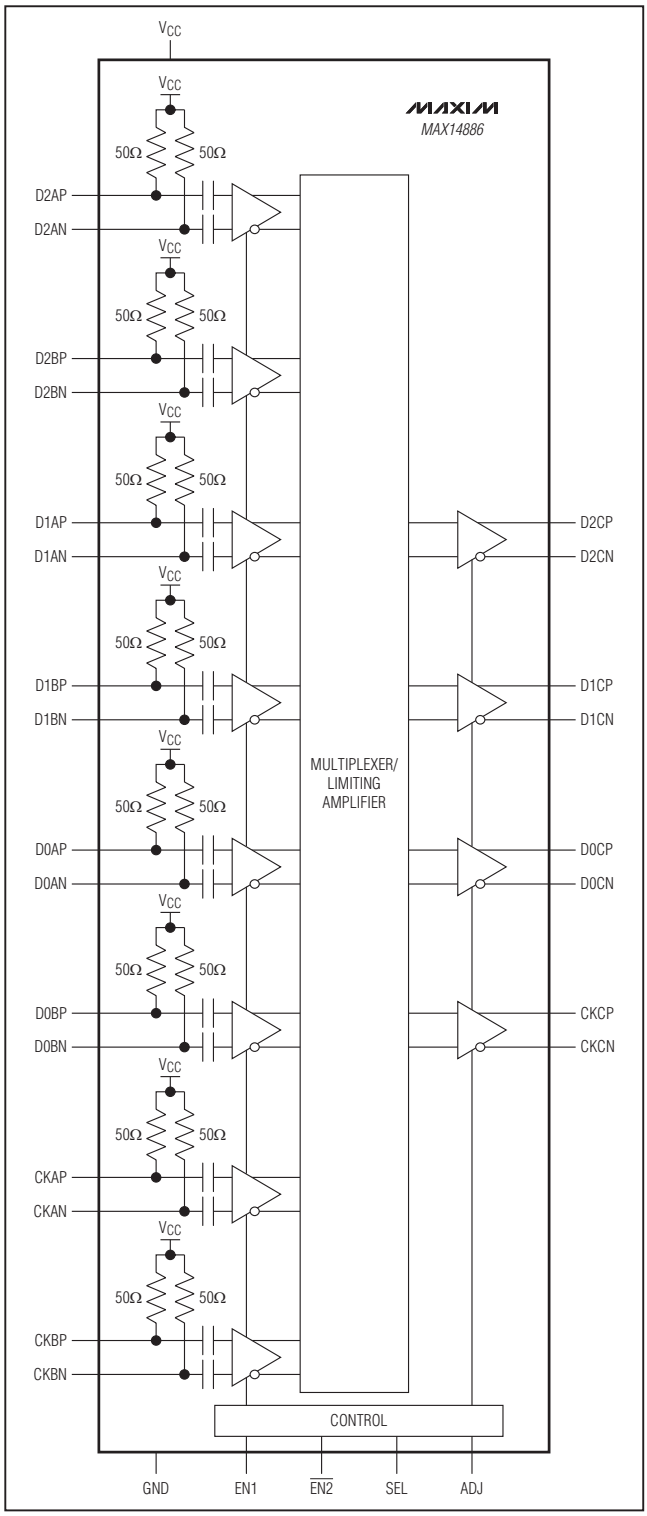
Pin Description

PIN	NAME	FUNCTION
1	D0AP	Noninverting Input D0 for Channel A
2	D0AN	Inverting Input D0 for Channel A
3	D0BP	Noninverting Input D0 for Channel B
4	D0BN	Inverting Input D0 for Channel B
5, 10, 11, 21, 26, 32, 35, 39	GND	Ground
6	CKAP	Noninverting Input Clock for Channel A
7	CKAN	Inverting Input Clock for Channel A
8	CKBP	Noninverting Input Clock for Channel B
9	CKBN	Inverting Input Clock for Channel B
12	CKCN	Inverting Output Clock
13	CKCP	Noninverting Output Clock
14	D0CN	Inverting Output D0
15	D0CP	Noninverting Output D0
16, 31, 36, 40	V_{CC}	Power-Supply Voltage. Bypass V_{CC} to GND with low-ESR 10nF and 4.7µF ceramic capacitors in parallel as close as possible to the device. Recommended on each V_{CC} pin.
17	D1CN	Inverting Output D1

PIN	NAME	FUNCTION
18	D1CP	Noninverting Output D1
19	D2CN	Inverting Output D2
20	D2CP	Noninverting Output D2
22	D2BP	Noninverting Input D2 for Channel B
23	D2BN	Inverting Input D2 for Channel B
24	D2AP	Noninverting Input D2 for Channel A
25	D2AN	Inverting Input D2 for Channel A
27	D1BP	Noninverting Input D1 for Channel B
28	D1BN	Inverting Input D1 for Channel B
29	D1AP	Noninverting Input D1 for Channel A
30	D1AN	Inverting Input D1 for Channel A
33	ADJ	Output Level Adjust
34	SEL	Mux Select Input. SEL is internally pulled down by a 400kΩ (typ) resistor.
37	$\overline{EN2}$	Active-Low Enable Input. $\overline{EN2}$ is internally pulled up by a 400kΩ (typ) resistor.
38	EN1	Active-High Enable Input. EN1 is internally pulled down by a 400kΩ (typ) resistor.
—	EP	Exposed Pad. Connect EP to GND.

Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

Functional Diagram/Truth Tables



EN1	$\overline{EN2}$	FUNCTION
0/Unconnected	X	Shutdown
X	1/Unconnected	Shutdown
1	0	Active

X = Don't care.

SEL	D_A_, CKA_	D_B_, CKB_
0/Unconnected	On	Off
1	Off	On

X = Don't care.

Detailed Description

The MAX14886 is a high-speed, low-skew, active redriver multiplexer designed to switch and amplify TMDS-formatted signals. Input buffers have 50Ω HDMI-compliant terminations to V_{CC} (see the *Functional Diagram/Truth Tables*), allowing either DC-coupling to an HDMI source or AC-coupling to a DisplayPort source. Signals from the input buffers are multiplexed and redriven by the limiting amplifier and an open-collector output buffer. The HDMI monitor sink is DC-coupled to the outputs and provides DC bias.

Both TMDS clock and data are multiplexed and redriven to full HDMI v.1.4 levels with low skew and jitter to guarantee mask compliance at an external HDMI connector. The device is VESA DisplayPort Interoperability Guideline v.1.1a-compliant and integrates seamlessly with an external HDMI connector on the motherboard. The low-frequency signals (DDC, CEC, and HPD) can be handled by external low-cost logic.

The device accommodates differential inputs as low as 200mV and drives differential TMDS outputs to 1000mV (typ). A precision resistor on the output level adjust pin (ADJ) allows differential output back-termination resistors of 400Ω (typ) to better meet HDMI mask jitter compliance, while maintaining full TMDS swing requirements.

This device also features both active-high and active-low enable inputs. One of the enable inputs can be connected to either V_{CC} or GND, while the other can be used to control the device (see the *Functional Diagram/Truth Tables* and *Enable Inputs (EN1, $\overline{EN2}$)* section). This eliminates any issues with logic sense and the need for an inverter.

Level Translation

The device accepts two sets of four differential DisplayPort-level TMDS-formatted inputs, each with magnitudes as low as 200mV. The selected channel is translated to full HDMI TMDS levels that are HDMI v.1.4 port mask-compliant up to 2.25Gbps.

Enable Inputs (EN1, $\overline{EN2}$)

The device features both an active-high enable input (EN1) and an active-low enable input ($\overline{EN2}$) that can be controlled by LVCMOS or LVTTL. EN1 has an internal 400kΩ (typ) pulldown resistor, and $\overline{EN2}$ has an internal 400kΩ (typ) pullup resistor. When EN1 is driven low or left unconnected, or $\overline{EN2}$ is driven high or left unconnected, the device enters low-power shutdown mode. For normal operation drive both EN1 high and $\overline{EN2}$ low. See the *Functional Diagram/Truth Tables*.

Only one input is necessary to control the device. If active-high enable is desired, connect $\overline{EN2}$ to GND and use EN1 to control the device. Similarly, for active-low enable, connect EN1 to V_{CC} and use $\overline{EN2}$ to control the device.

Note: The monitor sink termination must be present and powered before enabling the device (see the *Control Sequence* section and Figure 2).

Digital Control Input (SEL)

The device provides two sets of 4 channels for all the differential signals required by HDMI connections. The SEL input controls which channel is translated to the output channel (see the *Functional Diagram/Truth Tables*). An internal 400kΩ pulldown resistor guarantees that channel A is translated to the output if the SEL pin is not externally driven.

Output Level Adjust (ADJ)

The level-shifter's output current and output signal swing are set with an external ±1% precision 3.3kΩ (typ) resistor. If a double output termination (400Ω typ) is desired for signal integrity reasons, the ADJ resistor value can be decreased to maintain a desired output swing (Figure 1).

Applications Information

HDMI Driver

The device's high-speed, low-skew, active redriver multiplexer is ideal for switching between outputs of dual-graphics systems and signal conditioning to meet HDMI v.1.4 compliance at an external HDMI connector (Figure 1). It is well suited for switching between integrated (e.g., Intel or AMD) and discrete graphics (e.g., NVIDIA or ATI GPU). The device is VESA DisplayPort Interoperability Guideline v.1.1a-compliant (requires external DDC logic) and integrates seamlessly with an external HDMI connector on the motherboard.

Output Termination

Outputs are terminated in normal use by the HDMI monitor. For 50Ω test equipment purposes, terminate each output with a high-frequency bias-T that has an inductor in series with a 50Ω resistor to V_{CC}.

Control Sequence

The monitor sink termination must be present and powered before enabling the device. A simple circuit can be added to protect the device by forcing hot-plug detection (HPD) to be present before the part is enabled (Figure 2).

Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

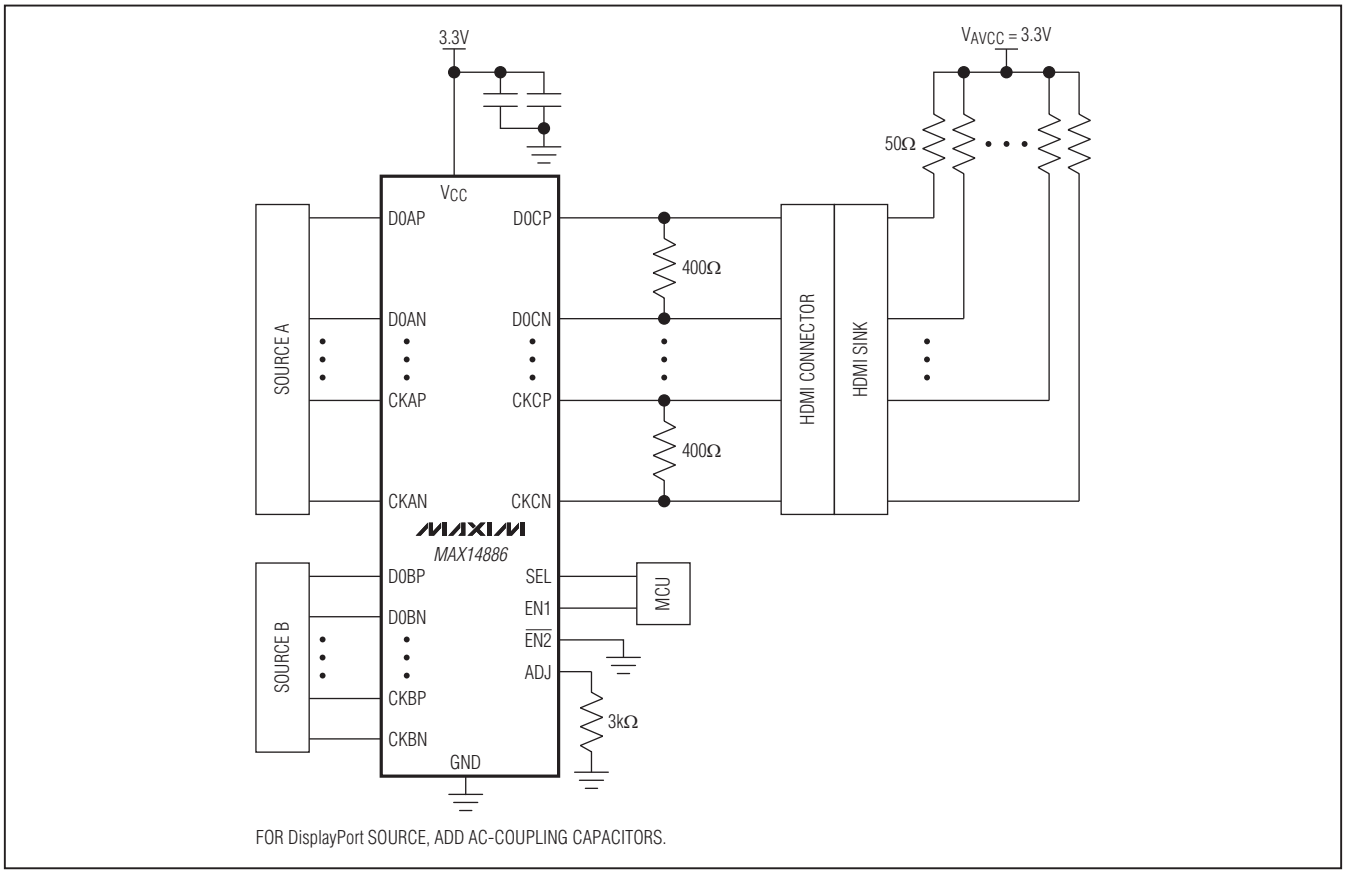


Figure 1. HDMI Driver Application with Output Back Termination

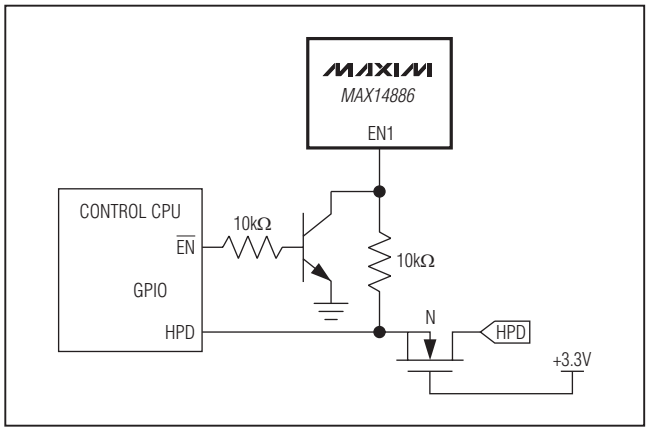


Figure 2. Control Sequence Protection Circuit

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize performance and noise immunity. Bypass each VCC pin to GND with high-frequency, low-ESR, X7R/X5R 10nF and 4.7µF surface-mount ceramic capacitors as close as possible to the device.

Printed Circuit Board (PCB) Traces

Input and output trace characteristics affect the performance of the device. Connect each of the inputs and outputs to a 50Ω characteristic impedance trace in to minimize reflections. Avoid discontinuities in differential impedance and maximize common-mode noise immunity by maintaining the distance between differential traces and avoiding sharp corners. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Exposed-Pad Package

The exposed-pad, 40-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the device must be soldered to the circuit board ground plane for proper electrical and thermal performance. For more information on exposed-pad packages, refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	21-0140	90-0002

Dual DisplayPort Graphics Multiplexer with HDMI Level Shifter

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—