M24LR64-R

64 Kbit EEPROM with password protection & dual interface: 400 kHz I²C serial bus & ISO 15693 RF protocol at 13.56 MHz

Data brief

Features

I²C interface

- Two-wire I²C serial interface supports 400 kHz protocol
- Single supply voltage:
  - 1.8 V to 5.5 V
- Byte and Page Write (up to 4 bytes)
- Random and Sequential Read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection

Contactless interface

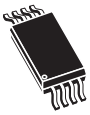
- ISO 15693 and ISO 18000-3 mode 1 compliant
- 13.56 MHz ±7 kHz carrier frequency
- To tag: 10% or 100% ASK modulation using 1/4 (26 Kbit/s) or 1/256 (1.6 Kbit/s) pulse position coding
- From tag: load modulation using Manchester coding with 423 kHz and 484 kHz subcarriers in low (6.6 kbit/s) or high (26 kbit/s) data rate mode. Supports the 53 kbit/s data rate with Fast commands
- Internal tuning capacitance: 27.5 pF
- 64-bit unique identifier (UID)
- Read Block & Write (32-bit Blocks)

Memory

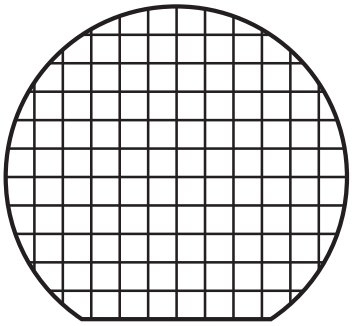
- 64 Kbit EEPROM organized into:
  - 8192 bytes in I²C mode
  - 2048 blocks of 32 bits in RF mode
- Write time
  - I²C: 5 ms (Max.)
  - RF: 5.75 ms including the internal Verify time
- More than 1 Million write cycles

SO8 (MN)
150 mils width

UFDFPN8 (MB)
2 × 3 mm



TSSOP8 (DW)



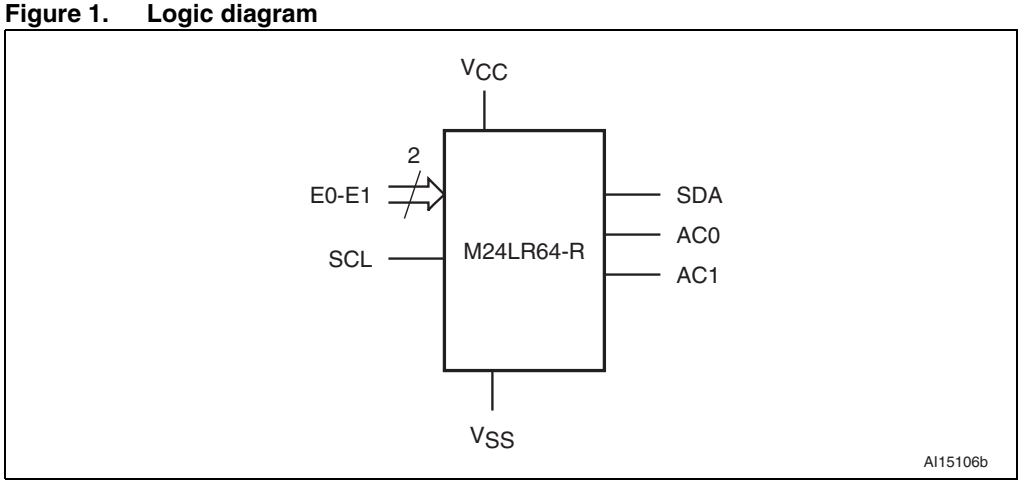
Sawn wafer on UV tape

- Multiple password protection in RF mode
- Single password protection in I²C mode
- More than 40-year data retention
- Package
  - ECOPACK2® (RoHS compliant and Halogen-free)

1 Description

The M24LR64-R device is a dual-interface, electrically erasable programmable memory (EEPROM). It features an I^2C interface and can be operated from a V_{CC} power supply. It is also a contactless memory powered by the received carrier electromagnetic wave. The M24LR64-R is organized as 8192 × 8 bits in the I^2C mode and as 2048 × 32 bits in the ISO 15693 and ISO 18000-3 mode 1 RF mode.

Figure 1. Logic diagram



I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/$\overline{\text{Write}}$ bit ($\text{R}\overline{\text{W}}$), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

In the ISO15693/ISO18000-3 mode 1 RF mode, the M24LR64-R is accessed via the 13.56 MHz carrier electromagnetic wave on which incoming data are demodulated from the received signal amplitude modulation (ASK: amplitude shift keying). The received ASK wave is 10% or 100% modulated with a data rate of 1.6 Kbit/s using the 1/256 pulse coding mode or a data rate of 26 Kbit/s using the 1/4 pulse coding mode.

Outgoing data are generated by the M24LR64-R load variation using Manchester coding with one or two subcarrier frequencies at 423 kHz and 484 kHz. Data are transferred from the M24LR64-R at 6.6 Kbit/s in low data rate mode and 26 Kbit/s high data rate mode. The M24LR64-R supports the 53 Kbit/s in high data rate mode in one subcarrier frequency at 423 kHz.

The M24LR64-R follows the ISO 15693 and ISO 18000-3 mode 1 recommendation for radio-frequency power and signal interface.

Table 1. Signal names

Signal name	Function	Direction
E0, E1	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
AC0, AC1	Antenna coils	I/O
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections

2 User memory organization

The M24LR64-R is divided into 64 sectors of 32 blocks of 32 bits. *Figure 4* shows the memory sector organization. Each sector can be individually read- and/or write-protected using a specific password command. Read and write operations are possible if the addressed data are not in a protected sector.

The M24LR64-R also has a 64-bit block that is used to store the 64-bit unique identifier (UID). The UID is compliant with the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user and its value is written by ST on the production line.

The M24LR64-R includes an AFI register that stores the application family identifier, and a DSFID register that stores the data storage family identifier used in the anticollision algorithm.

The M24LR64-R has four additional 32-bit blocks that store an I^2C password plus three RF password codes.

Figure 3. Block diagram

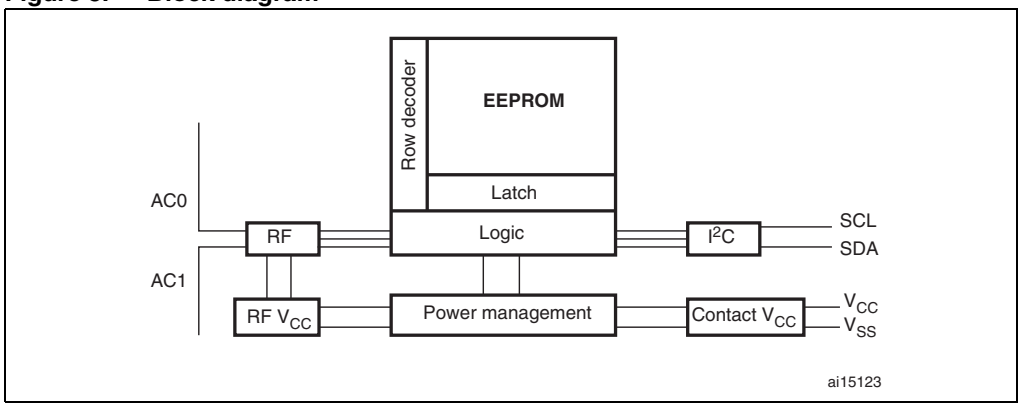
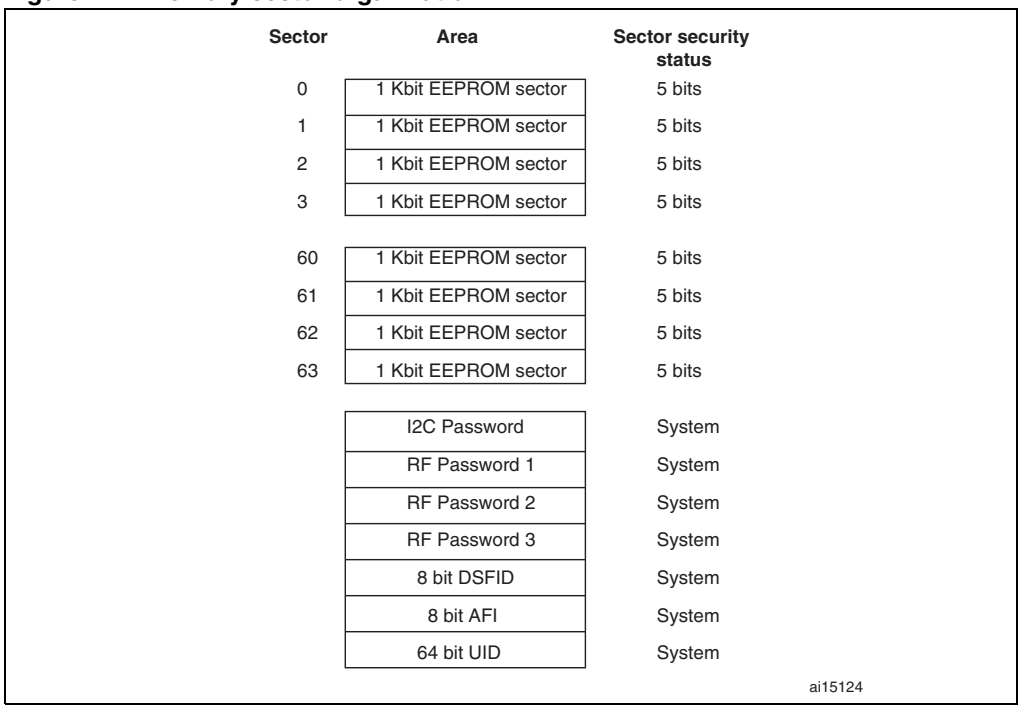


Figure 4. Memory sector organization



3 Commands

The M24LR64-R supports the following commands:

- ***Inventory***, used to perform the anticollision sequence.
- ***Stay Quiet***, used to put the M24LR64-R in quiet mode, where it does not respond to any inventory command.
- ***Select***, used to select the M24LR64-R. After this command, the M24LR64-R processes all Read/Write commands with Select_flag set.
- ***Reset To Ready***, used to put the M24LR64-R in the ready state.
- ***Read Block***, used to output the 32 bits of the selected block and its locking status.
- ***Write Block***, used to write the 32-bit value in the selected block, provided that it is not locked.
- ***Read Multiple Blocks***, used to read the selected blocks and send back their value.
- ***Write AFI***, used to write the 8-bit value in the AFI register.
- ***Lock AFI***, used to lock the AFI register.
- ***Write DSFID***, used to write the 8-bit value in the DSFID register.
- ***Lock DSFID***, used to lock the DSFID register.
- ***Get System Info***, used to provide the system information value
- ***Get Multiple Block Security Status***, used to send the security status of the selected block.
- ***Initiate***, used to trigger the tag response to the Inventory Initiated sequence.
- ***Inventory Initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Write-sector Password***, used to write the 32 bits of the selected password.
- ***Lock-sector Password***, used to write the Sector security status bits of the selected sector.
- ***Present-sector Password***, enables the user to present a password to unprotect the user blocks linked to this password.
- ***Fast Initiate***, used to trigger the tag response to the Inventory Initiated sequence.
- ***Fast Inventory Initiated***, used to perform the anticollision sequence triggered by the Initiate command.
- ***Fast Read Single Block***, used to output the 32 bits of the selected block and its locking status.
- ***Fast Read Multiple Blocks***, used to read the selected blocks and send back their value.

4 Part numbering

Table 2. Ordering information scheme for packaged devices

Example: M24LR64-R MN 6 T /2

Device type

M24LR64 = Dual interface EEPROM

Operating voltage

R = V_{CC} = 1.8 to 5.5 V

Package

MN = SO8N (150 mils width)

MB = UFDFPN8 (MLP8)

DW = TSSOP8

Device grade

6 = industrial: device tested with standard test flow over –40 to 85 °C

Option

T = Tape and reel packing

Capacitance

/2 = 27.5 pF

Table 3. Ordering information scheme for bare die devices

Example: M24LR64-R S 1 8 5 /2

Device type

M24LR64 = Dual interface EEPROM

Operating voltage

R = V_{CC} = 1.8 to 5.5 V

Packing

S = Sawn wafer (inkless) in UV tape

Z = Sawn wafer (inked) in UV tape

Wafer orientation

1 = see *Note 1*

Wafer size in inches

8 = 8-inch wafer (see *Note 1*)

Wafer thickness

5 = 140 µm (see *Note 1*)

Capacitance

/2 = 27.5 pF

Note: 1 Refer to technical note TN0185 for details on the die delivery form.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Revision history

Table 4. Document revision history

Date	Revision	Changes
15-May-2008	0.1	Initial release.
17-Nov-2008	1	Part number changed in *Table 2: Ordering information scheme for packaged devices*
30-Jul-2009	2	Tuning capacitance corrected on page 1
29-Jan-2010	3	Programming time modified in *Features*
09-Aug-2010	4	Added bare die product information.

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