

# DATA SHEET

## **PCA8550**

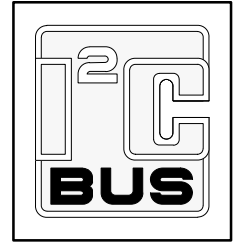
4-bit multiplexed/1-bit latched 5-bit  
I<sup>2</sup>C EEPROM DIP switch

Product data  
Supersedes data of 2001 Jan 12

2003 Jun 27

# 4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM DIP switch

PCA8550



## FEATURES

- 4-bit 2-to-1 multiplexer, 1-bit latch DIP switch
- 5-bit internal non-volatile register
- Override input forces all outputs to logic 0
- Internal non-volatile register write/readable via I<sup>2</sup>C-bus
- Write-protect pin enables/disables I<sup>2</sup>C writes to register
- 2.5 V multiplexed outputs
- 3.3 V non-multiplexed output (latched)
- 5 V tolerant inputs
- Useful for 'jumperless' configuration of PC motherboards
- Designed for use in Pentium Pro/Pentium II™ systems

## DESCRIPTION

The primary function of the 4-bit 2-to-1 I<sup>2</sup>C multiplexer is to select either a 4-bit input or data from a non-volatile register and drive this value onto the output pins. One additional non-multiplexed register output is also provided. The non-multiplexed output is latched to prevent output value changes during I<sup>2</sup>C writes to the non-volatile register. A write protect input is provided to enable/disable the ability to write to the non-volatile register. An "override" input feature forces all outputs to logic 0.

## PIN CONFIGURATION

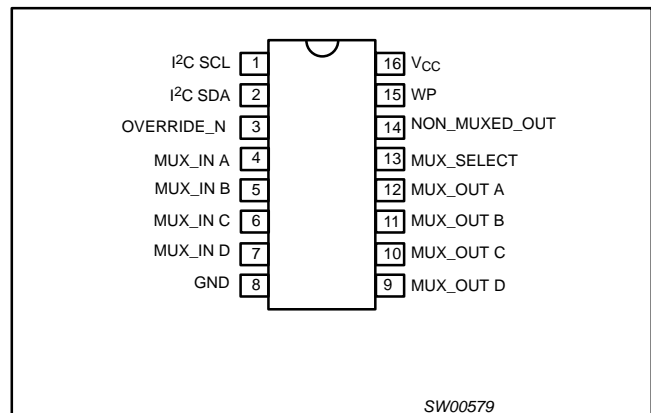


Figure 1. Pin configuration

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-Pin Plastic SO	0 to +70 °C	PCA8550D	PCA8550	SOT109-1
16-Pin Plastic SSOP	0 to +70 °C	PCA8550DB	PA8550	SOT338-1
16-Pin Plastic TSSOP	0 to +70 °C	PCA8550PW	PCA8550	SOT403-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

## FUNCTIONAL DESCRIPTION

When the MUX\_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX\_OUT pins. When the MUX\_SELECT signal is logic 1, the multiplexer will select the MUX\_IN lines to drive on the MUX\_OUT pins. The MUX\_SELECT signal is also used to latch the NON\_MUXED\_OUT signal which outputs data from the non-volatile register. The NON\_MUXED\_OUT signal latch is transparent when MUX\_SELECT is in a logic 0 state, and will latch data when MUX\_SELECT is in a logic 1 state. When the active-LOW OVERRIDE\_N signal is set to logic 0 and the MUX\_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

The write protect (WP) input is used to control the ability to write the contents of the 5-bit non-volatile register. If the WP signal is logic 0, the I<sup>2</sup>C-bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I<sup>2</sup>C bus (described in the next section).

The OVERRIDE\_N, WP, MUX\_IN, and MUX\_SELECT signals have internal pull-up resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I <sup>2</sup> C SCL	I <sup>2</sup> C-bus clock
2	I <sup>2</sup> C SDA	Bi-directional I <sup>2</sup> C-bus data
3	OVERRIDE_N	Forces all outputs to logic 0
4	MUX_IN A	External inputs to multiplexer
5	MUX_IN B	
6	MUX_IN C	
7	MUX_IN D	
8	GND	Common ground voltage rail
9	MUX_OUT D	2.5 V multiplexed output
10	MUX_OUT C	
11	MUX_OUT B	
12	MUX_OUT A	
13	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
14	NON_MUXED_OUT	TTL-level output from non-volatile memory
15	WP	Non-volatile register write-protect
16	V <sub>CC</sub>	Positive voltage rail

## FUNCTION TABLE

Table 1. Function table

OVERRIDE_N	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT <sup>1</sup>
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

### NOTE

- Latched NON\_MUXED\_OUT state will be the value present on the NON\_MUXED\_OUT output at the time of the MUX\_SELECT input transitioned from a logic 0 to a logic 1 state.

## I<sup>2</sup>C INTERFACE

Communicating with this device is initiated by sending a valid address on the I<sup>2</sup>C-bus. The address format (see Figure 2) is a fixed unique 7-bit value followed by a 1-bit read/write value which determines the direction of the data transfer.

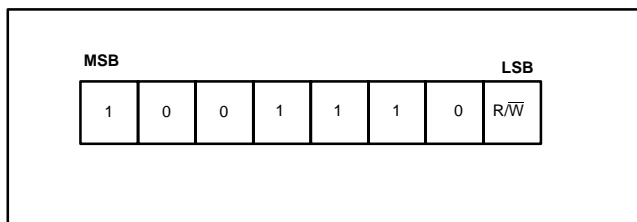


Figure 2. I<sup>2</sup>C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The three high-order bits (see Figure 3) are logic 0. The next bit is data which is non-multiplexed. The low four bits are the data which will be multiplexed. A write with any of the first three bits non-zero will be aborted.

### NOTE:

- To ensure data integrity, the non-volatile register must be internally write protected when V<sub>CC</sub> to the I<sup>2</sup>C-bus is powered down or V<sub>CC</sub> to the component is dropped below normal operating levels.

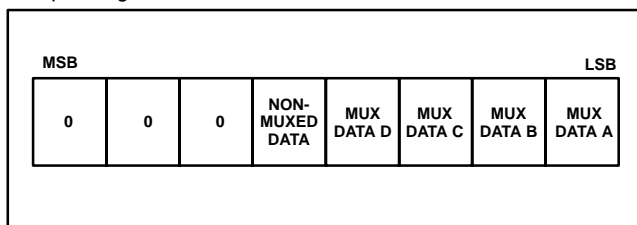


Figure 3. I<sup>2</sup>C Data Byte

## POWER-ON RESET (POR)

When power is applied to V<sub>CC</sub>, an internal power-on reset holds the PCA8550 in a reset state until V<sub>CC</sub> has reached V<sub>POR</sub>. At that point, the reset condition is released and the PCA8550 volatile registers and I<sup>2</sup>C state machine will initialize to their default states.

The MUX\_OUT and NON\_MUXED\_OUT pin values depend on:

- the OVERRIDE\_N and MUX\_SELECT logic levels
- the previously stored values in the EEPROM register/current MUX\_IN pin values as shown in Table 1.

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## BLOCK DIAGRAM

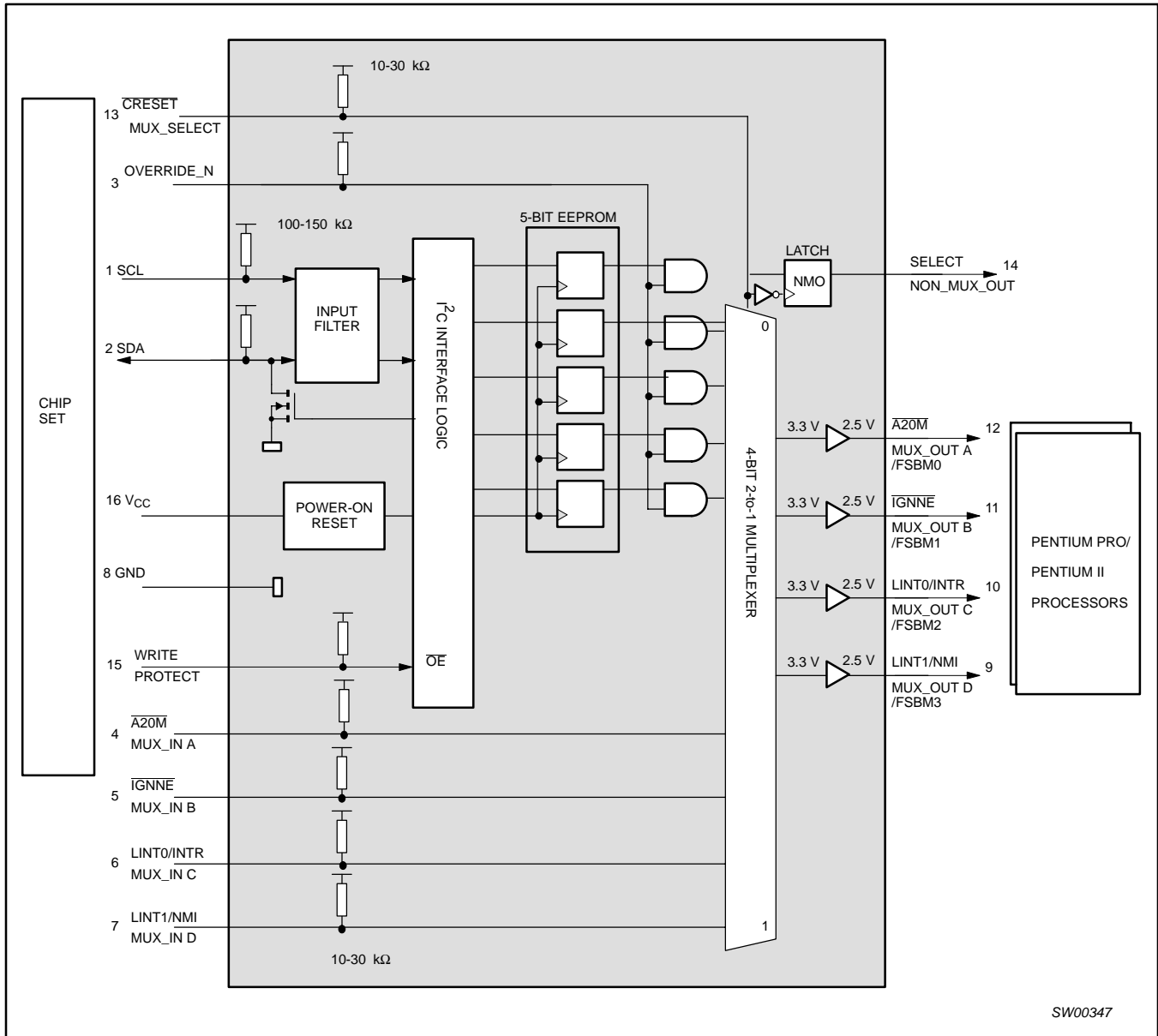


Figure 4. Block diagram

SW00347

# 4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM DIP switch

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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
V <sub>I</sub>	DC input voltage	Note 3	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC output voltage	Note 3	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		CONDITIONS	LIMITS		UNIT
				MIN	MAX	
V <sub>CC</sub>	DC supply voltage			3.0	3.6	V
V <sub>POR</sub>	Power-on reset voltage		No load; V <sub>I</sub> = V <sub>DD</sub> or GND	—	2.6	V
V <sub>IL</sub>	LOW-level input voltage	SCL, SDA	I <sub>OL</sub> = 3 mA	-0.5	0.9	V
V <sub>IH</sub>	HIGH-level input voltage	SCL, SDA	I <sub>OL</sub> = 3 mA	2.7	4.0	V
V <sub>OL</sub>	LOW-level output voltage	SCL, SDA	I <sub>OL</sub> = 3 mA	—	0.4	V
V <sub>IL</sub>	LOW-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT		-0.5	0.8	V
V <sub>IH</sub>	HIGH-level input voltage	OVERRIDE_N, MUX_IN, MUX_SELECT		2.0	4.0	V
I <sub>OL</sub>	LOW-level output current	MUX_OUT NON_MUXED_OUT		—	2.0	mA
I <sub>OH</sub>	HIGH-level output current	MUX_OUT NON_MUXED_OUT		—	-2.0	mA
dt/dv	Input transition rise or fall time			0	10	ns/V
T <sub>amb</sub>	Operating ambient temperature			0	70	°C

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## DC CHARACTERISTICS

Temp = 0 to +70 °C 3.0 V < V<sub>CC</sub> ≤ 3.6 V

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
<b>SCL, SDA</b>					
V <sub>OL</sub>	LOW-level output voltage		0	0.6	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V		3.0	mA
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.6 V		6.0	mA
I <sub>IL</sub> <sup>1</sup>	LOW-level input current	V <sub>IL</sub> = 0.4 V	-7	-32	μA
I <sub>IH</sub>	HIGH-level input current	V <sub>IH</sub> = 2.4 V	-1.5	-12	μA
V <sub>hys</sub>	Hysteresis voltage		0.19		V
<b>VERRIDE_N, WP, MUX_SELECT</b>					
I <sub>IL</sub>	LOW-level input current		-86	-267	μA
I <sub>IH</sub>	HIGH-level input current		-20	-100	μA
<b>MUX_IN A ⇒ D</b>					
I <sub>IL</sub>	LOW-level input current	V <sub>IL</sub> = 0.4 V	-0.72	-2.0	mA
I <sub>IH</sub>	HIGH-level input current	V <sub>IH</sub> = 2.4 V	-0.72	-2.0	mA
<b>MUX_OUT</b>					
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-0.3	0.4	V
		I <sub>OL</sub> = 2.0 mA	-0.3	0.7	
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -100 μA	2.0	2.625	V
		I <sub>OH</sub> = -1.0 mA	1.7	2.625	
<b>NON_MUXED_OUT</b>					
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 100 μA	-0.5	0.4	V
		I <sub>OL</sub> = 2.0 mA	-0.5	0.7	
V <sub>OH</sub>	HIGH-level output voltage	I <sub>OH</sub> = -100 μA	2.4	3.6	V
		I <sub>OH</sub> = -2.0 mA	2.0	3.6	
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 V to V <sub>CC</sub>		10	mA
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub>		500	μA
C <sub>I</sub>	Input capacitance			10	pF
	ESD protection		2.0		KV
	Input diode clamp voltage		-1.5		V

### NOTES:

- V<sub>HYS</sub> is the hysteresis of Schmitt-Trigger inputs
- Human body model

## NON-VOLATILE STORAGE SPECIFICATIONS

Parameter	Specification
Memory cell data retention	10 years min
Number of memory cell write cycles	100,000 cycles min

Application Note AN250 I<sup>2</sup>C DIP Switch provides additional information on memory cell data retention and the minimum number of write cycles.

# 4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM DIP switch

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t <sub>MPD</sub>	Mux input to output propagation delay		20.0	ns
t <sub>SOV</sub>	MUX_SELECT to output valid		22	ns
t <sub>OVN</sub>	OVERRIDE_N to NON_MUX output delay		15.0	ns
t <sub>OVM</sub>	OVERRIDE_N to mux output delay		25.0	ns
t <sub>R</sub>	Output rise time	1.0	3.0	ns/V
t <sub>F</sub>	Output fall time	1.0	3.0	ns/V
C <sub>L</sub>	Test load capacitance on Muxed/Non-Muxed outputs		15	pF
<b>I<sup>2</sup>C-bus</b>				
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	10	400	KHz
t <sub>SCH</sub>	I <sup>2</sup> C clock HIGH time	600		ns
t <sub>SCL</sub>	I <sup>2</sup> C clock LOW time	1.3		ns
t <sub>DSP</sub>	I <sup>2</sup> C data spike time	0	50	ns
t <sub>SDS</sub>	I <sup>2</sup> C data set-up time	100		ns
t <sub>SDH</sub>	I <sup>2</sup> C data hold time	0		ns
t <sub>ICR</sub>	I <sup>2</sup> C input rise time (10-400 pF bus)	20	300	ns
t <sub>ICF</sub>	I <sup>2</sup> C input fall time (10-400 pF bus)	20	300	ns
t <sub>BUF</sub>	I <sup>2</sup> C-bus free time between start and stop	1.3		ns
t <sub>STS</sub>	I <sup>2</sup> C repeated start condition set-up	600		ns
t <sub>STH</sub>	I <sup>2</sup> C repeated start condition hold	600		ns
t <sub>SPS</sub>	I <sup>2</sup> C stop condition set-up	600		ns
C <sub>B</sub>	I <sup>2</sup> C-bus capacitive load		400	pF
T <sub>W</sub>	Write cycle time <sup>1</sup>	TYPICAL = 15		ms

### NOTE:

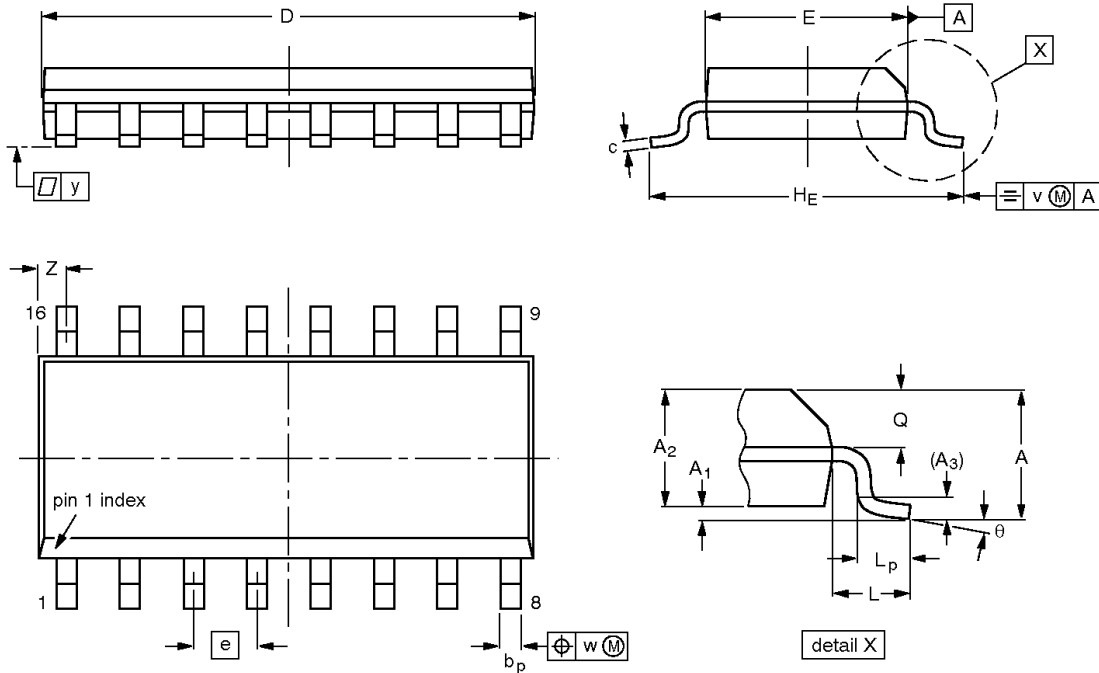
1. WRITE CYCLE time can only be measured indirectly during write cycle. The device will not acknowledge its I<sup>2</sup>C address.

4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM DIP switch

PCA8550

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22 99-12-27

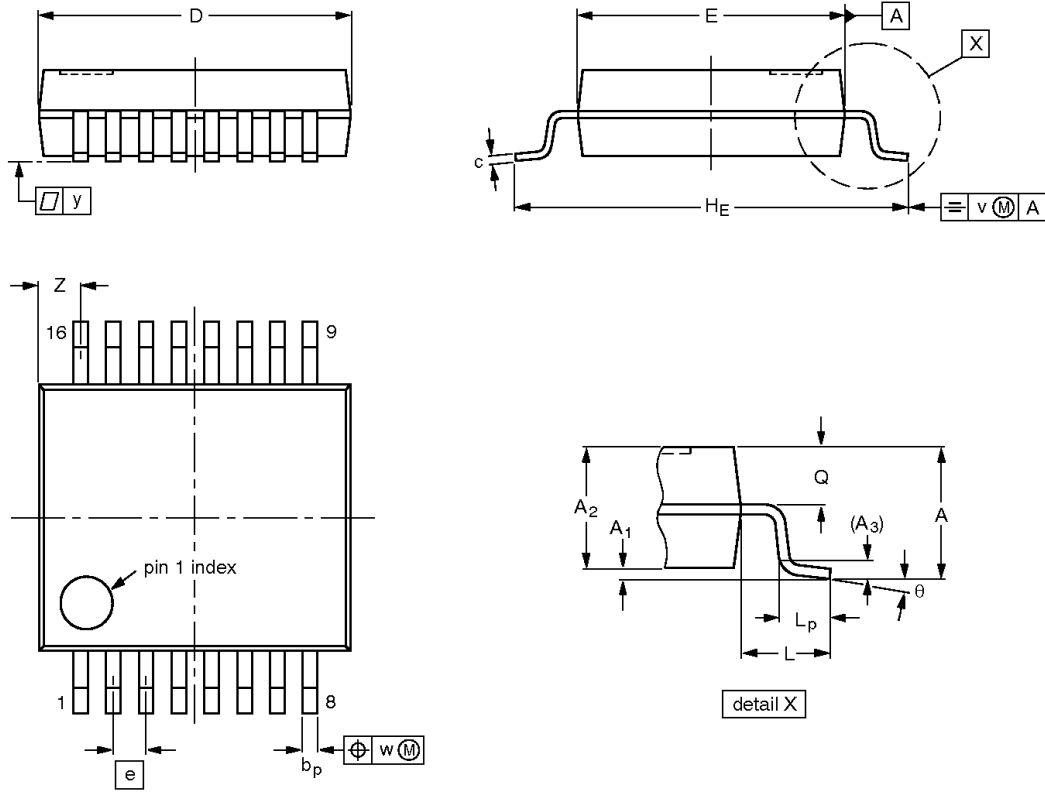


4-bit multiplexed/1-bit latched 5-bit  
I<sup>2</sup>C EEPROM DIP switch

PCA8550

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

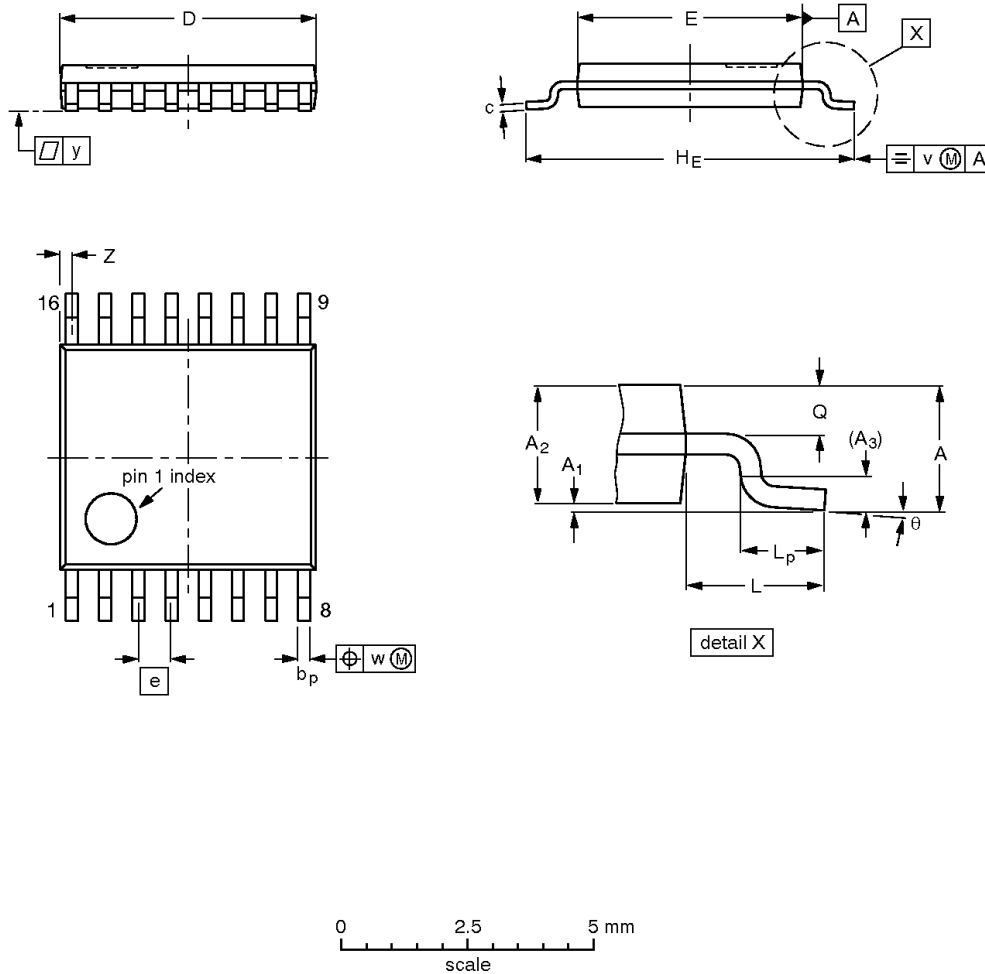
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				95-02-04 99-12-27

4-bit multiplexed/1-bit latched 5-bit  
I<sup>2</sup>C EEPROM DIP switch

PCA8550

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				-95-04-04 99-12-27

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4-bit multiplexed/1-bit latched 5-bit  
I<sup>2</sup>C EEPROM DIP switch

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PCA8550

**REVISION HISTORY**

Rev	Date	Description
_6	20030627	<b>Product data (9397 750 11678); ECN 853-2015 29936 dated 19 May 2003. Supersedes data of 2001 Jan 12 (9397 750 07926).</b> Modifications: <ul style="list-style-type: none"><li>• Update marketing information.</li><li>• Increase number of write cycles from 3K to 100K.</li></ul>
_5	20010112	Product data (9397 750 07926); ECN 853-2015 25405 of 12 Jan 2001.

# 4-bit multiplexed/1-bit latched 5-bit I<sup>2</sup>C EEPROM DIP switch

PCA8550



Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 06-03

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