

# FT8010

## Reset Timer with Configurable Delay Time

### Features

- Long Delay Configurable to 7.5 or 11.25 Seconds
- Primary and Secondary Input Reset Pins
- Push-Pull and Open-Drain Output Pins
- 2.0V to 5.0V Operation
- Packaged in 10-Lead UMLP (1.4mm x 1.8mm) and 8-Lead MLP (2.0mm x 2.0mm) Packages

### Description

The FT8010 is a timer for resetting a mobile device where long reset times are needed. The long time delay helps avoid unintended resets caused by accidental key presses. Two delays can be selected by hard-wiring the DSR pin: 7.5 ±20% seconds or 11.25 ±20% seconds.

The FT8010 has two identical inputs for single or dual switch resetting capability. The device has two outputs: a push-pull output with 0.5mA drive and an open-drain output with 0.5mA pull-down drive.

FT8010 draws minimal  $I_{CC}$  current when inactive and functions over a wide 2.0V to 5.0V power supply range.

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FT8010UMX	-40°C to +85°C	10-Lead Ultrathin MLP, 1.4 x 1.8 x 0.55mm Package, 0.40mm Pitch	5000 Units Tape and Reel
FT8010MPX	-40°C to +85°C	8-Lead, MLP 2.0 x 2.0 x 0.8mm Package, 0.5mm Pitch	3000 Units Tape and Reel

Block Diagram

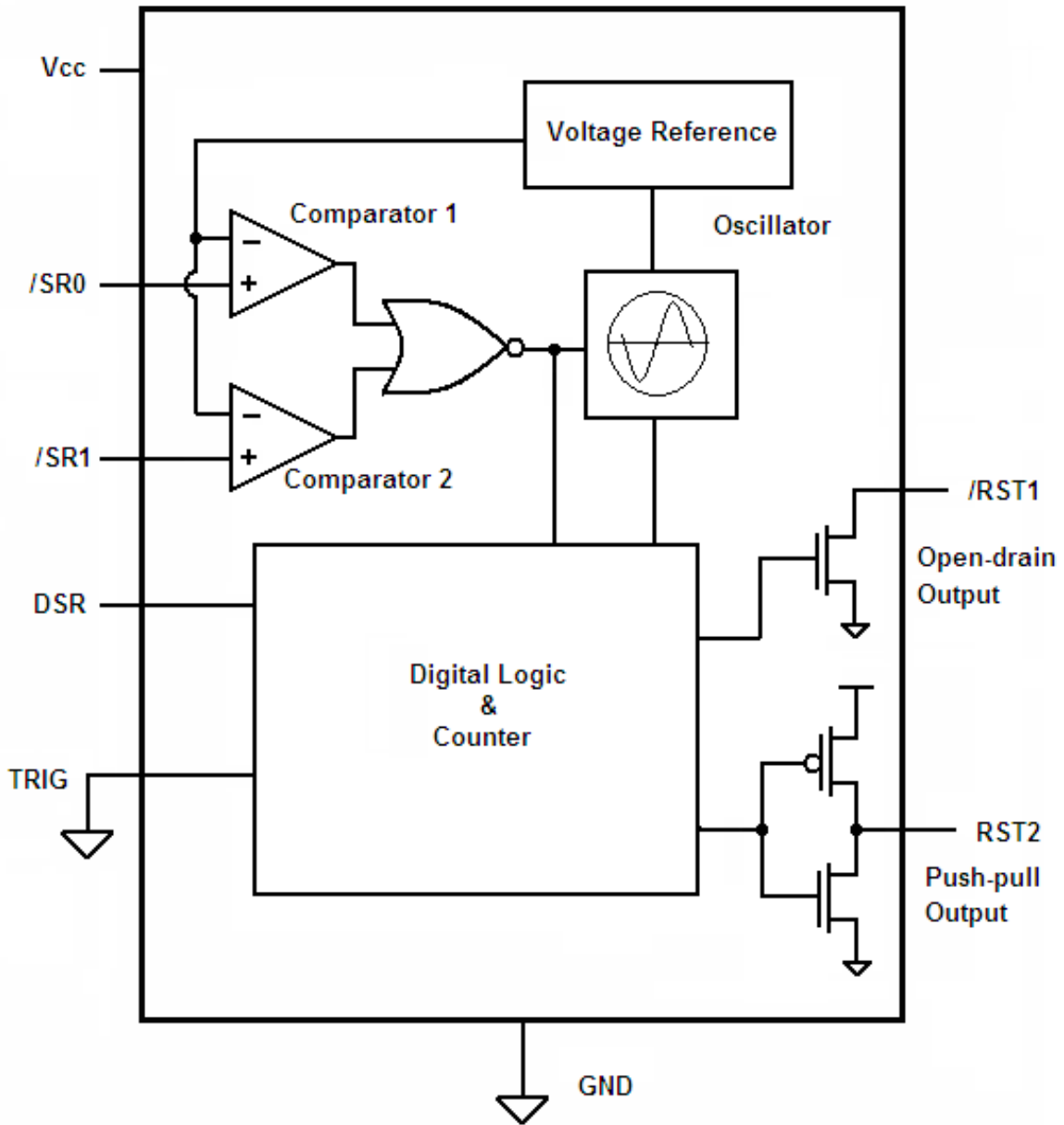


Figure 1. Block Diagram



## Pin Configuration

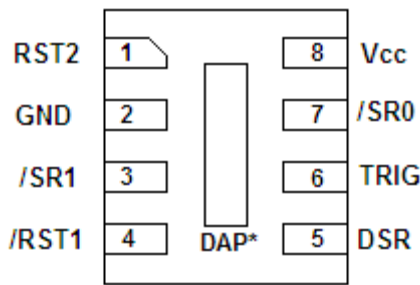


Figure 2. MLP Pin Configuration<sup>(1)</sup>  
(Top Through View)

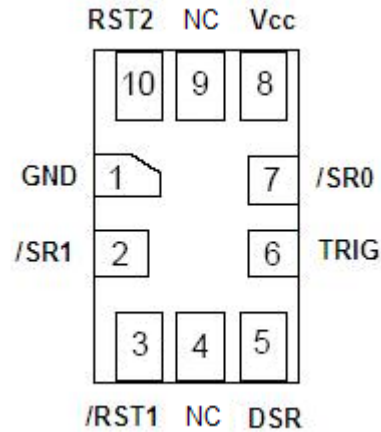


Figure 3. UMLP Pin Configuration<sup>(2)</sup>  
(Top Through View)

**Note:**

1. The DAP may be a no connect or it may be tied to ground.
2. NC = No connect

## Pin Definitions

MLP Pin #	UMLP Pin #	Name	Description
1	10	RST2	Push-Pull Output, Active HIGH
2	1	GND	Ground
3	2	/SR1	Secondary Reset Input, Active LOW
4	3	/RST1	Open-Drain Output, Active LOW
5	5	DSR	Delay Selection Input
6	6	TRIG	Test Pin, Tied to GND in Normal Use
7	7	/SR0	Primary Reset Input, Active LOW
8	8	V <sub>CC</sub>	Power Supply
	4, 9,	NC	No Connect

## Functional Description

The FT8010 reset timer uses an internal oscillator and a two-stage, 21-bit counter to determine when the output pins switch. Time N is set by the hard-wired logic level of the DSR pin. N is either 7.5 ±20% seconds for DSR=LOW or 11.25 ±20% seconds for DSR=HIGH.

**Table 1. FT8010 Truth Table**

DSR	Reset Timer ( ±20% )
0	7.5s
1	11.25s

The two input pins, /SR0 and /SR1, drive voltage comparators that compare the voltage on the input with the voltage set by the reference block. A low input signal on both /SR0 and /SR1 starts the oscillator. The oscillator sends data pulses to the digital core, which includes the counter. There are two scenarios for counting, as described below: short duration and long duration. In the short-duration scenario, outputs /RST1 and RST2 are not affected. In the long duration scenario, the outputs change state after time N. The outputs return to their original states when a HIGH input signal occurs on either /SR0 or /SR1.

The /RST1 output is an open-drain driver. When the count time exceeds time N, the /RST1 output drives LOW. The RST2 output is a push-pull driver. When the count time exceeds time N, the RST2 output drives HIGH.



The TRIG pin should be tied GND or LOW during normal operation. The TRIG pin is a test mode pin used for SCAN testing.

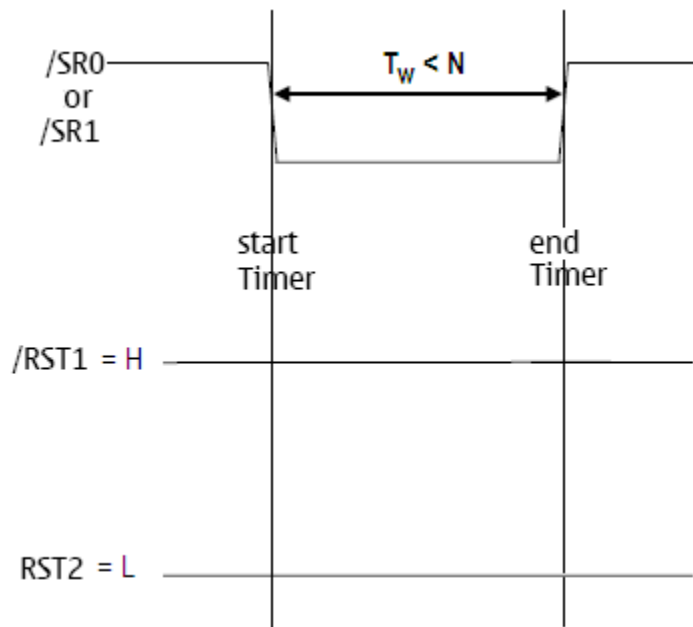
## Application Note

**IMPORTANT:** The DSR pin must be tied to V<sub>CC</sub> or GND to provide a HIGH or LOW voltage level. The voltage level on the DSR pin determines the length of the configurable delay. **It is important that the voltage level on the DSR pin not change during normal operation. The DSR must be tied to valid Vcc or GND before SR0 or SR1 buttons go LOW.**

## Short Duration ( $t_w < N$ )

In this case, both input /SR0 and /SR1 are LOW for a duration  $t_w$  which is shorter than time N. When an input goes LOW, the internal timer starts counting. The input goes HIGH before time N. The timer stops counting and resets and no changes occur on the outputs (see Figure 4).

/SR0	/SR1	/RST1	RST2	Description
	L	H	L	The timer starts counting when both inputs go LOW. The timer stops counting and resets when either input goes HIGH. No changes occur on the outputs, Both /SR0 and /SR1 need to be LOW to activate (start) the timer.
L		H	L	



**Figure 4. Short Duration Waveform**

### Long Duration ( $t_w > N$ )

In this case, inputs /SR0 and /SR1 are LOW for a duration,  $t_w$ , which is longer than time N. When an input goes LOW, the internal timer starts counting. After time N, the outputs switch and the timer stops counting. The input goes HIGH sometime after N

seconds. When the input goes HIGH, the timer resets and the outputs switch back to their original state after a propagation delay (see Figure 5).

/SR0	/SR1	/RST1	RST2	Description
	L			The timer starts counting when both inputs go LOW. After time N, the outputs switch. When either input goes HIGH, the timer resets and the outputs switch back to their original state. Both /SR0 and /SR1 need to be LOW to activate (start) the timer.
L				

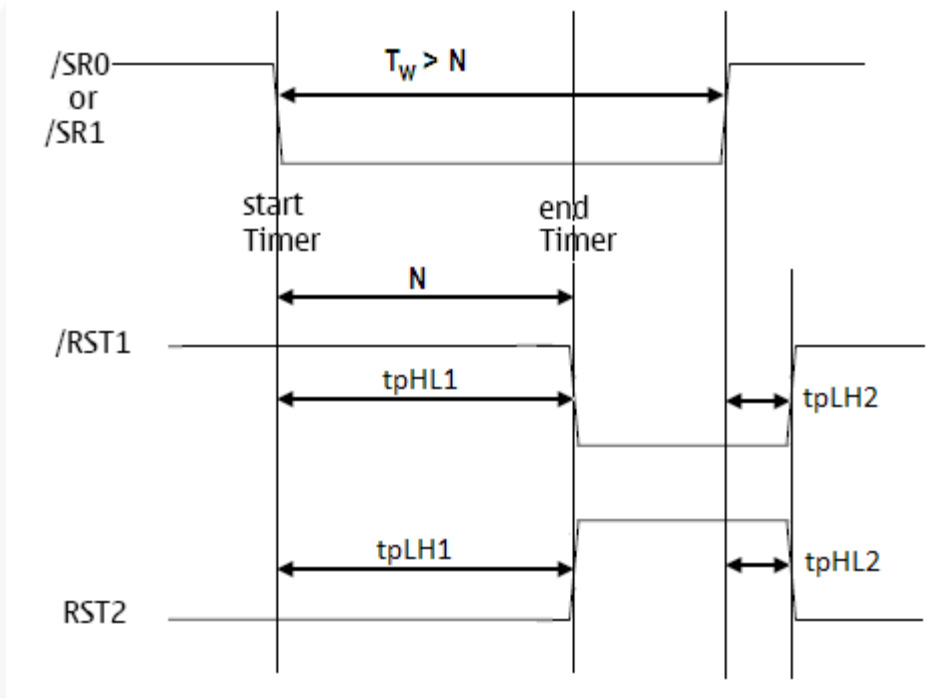


Figure 5. Long Duration Waveform

**Note:**

- Waveforms not drawn to scale ( $tpHL1, tpLH1 \gg tpHL2, tpLH2$ )



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage		-0.5	5.5	V
$V_{IN}$	DC Input Voltage	/SR0, /SR1, TRIG, DSR	-0.5	5.5	V
$V_{OUT}$	Output Voltage <sup>(4)</sup>	/RST1 HIGH or LOW	-0.5	5.5	V
		RST2 HIGH or LOW	-0.5	$V_{CC}+0.5$	
		/RST1, RST2, $V_{CC}=0$	-0.5	5.5	
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < 0V$		-50	mA
		$V_{OUT} > V_{CC}$		+50	
$I_{OH}/I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin			$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	$^{\circ}C$
$T_J$	Junction Temperature under Bias			+150	$^{\circ}C$
$T_L$	Junction Lead Temperature, Soldering 10 Seconds			+260	$^{\circ}C$
$P_D$	Power Dissipation			5	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
		Charged Device Model, JESD22-C101		2	

### Note:

4.  $I_O$  absolute maximum rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage		1.8	5.0	V
$t_{RFC}$	$V_{CC}$ Recovery Time After Power Down	$V_{CC}=0V$ After Power Down, Rising to 0.5V	5		ms
$V_{IN}$	Input Voltage	/SR0, /SR1	0	5	V
$V_{OUT}$	Output Voltage	/RST1 HIGH or LOW	0	5	V
		RST2 HIGH or LOW	0	$V_{CC}$	
		/RST1, RST2, $V_{CC}=0$	0	5	
$I_{OH}$	DC Output Source Current	RST2, $1.8V \leq V_{CC} \leq 3.0V$	-0.1		mA
		RST2, $3.0V \leq V_{CC} \leq 5.0V$	-0.5		
$I_{OL}$	DC Output Sink Current	/RST1, RST2, $V_{CC}=1.8V$ to 5.0V	+0.5		
$T_A$	Free Air Operating Temperature		-40	+85	$^{\circ}C$
$\Theta_{JA}$	Thermal Resistance	MLP-8		245	$^{\circ}C/W$
		UMLP-10		200	

### Note:

5. All unused inputs must be held at  $V_{CC}$  or GND.

## DC Electrical Characteristics

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min.	Max.	Unit
$V_{IH}$	Input High Voltage	/SR0, /SR1	2.0 to 5.0	1.2		V
		DSR	2.0 to 5.0	$0.65 \times V_{CC}$		
$V_{IL}$	Input Low Voltage	/SR0, /SR1	2.0 to 5.0		0.32	V
		DSR	2.0 to 5.0		$0.25 \times V_{CC}$	
$V_{OH}$	High Level Output Voltage	RST2, $I_{OH} = -100\mu\text{A}$	1.8 to 3.0	$0.8 \times V_{CC}$		V
		RST2, $I_{OH} = -500\mu\text{A}$	3.0 to 5.0	$0.8 \times V_{CC}$		
$V_{OL}$	Low Level Output Voltage	RST2, $I_{OL} = 500\mu\text{A}$	2.0 to 5.0		0.3	V
		/RST1, $I_{OL} = 500\mu\text{A}$	1.8 to 5.0		0.3	
$I_{IN}$	Input Leakage Current	$0V \leq V_{IN} \leq 5.0V$	2.0 to 5.0		$\pm 1.0$	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current (Timer Inactive)	/SR0 or /SR1 = $V_{CC}$	2.0 to 5.0		20	$\mu\text{A}$
	Dynamic Supply Current (Timer Active)	/SR0 = /SR1 = $0V$	2.0 to 5.0		100	

## AC Electrical Characteristics

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min.	Typ.	Max.	Unit
$t_{PHL1}$	Timer Delay, /SRn to /RST1, (DSR=0)	$C_L = 5\text{pF}$ , $R_L = 5\text{K}\Omega$ See Figure 6	2.0 to 5.0	6.0	7.5	9.0	s
	Timer Delay, /SRn to /RST1, (DSR=1)	$C_L = 5\text{pF}$ , $R_L = 5\text{K}\Omega$ See Figure 6	2.0 to 5.0	9.00	11.25	13.50	s
$t_{PLH2}$	Propagation Delay, /SRn to /RST1 (DSR=0 or 1)	$C_L = 5\text{pF}$ , $R_L = 5\text{K}\Omega$ See Figure 6	2.0 to 5.0		220	310	ns
$t_{PLH1}$	Timer Delay, /SRn to RST2, (DSR=0)	$C_L = 5\text{pF}$ , $R_L = 10\text{K}\Omega$ See Figure 7	2.0 to 5.0	6.0	7.5	9.0	s
	Timer Delay, /SRn to RST2, (DSR=1)	$C_L = 5\text{pF}$ , $R_L = 10\text{K}\Omega$ See Figure 7	2.0 to 5.0	9.00	11.25	13.50	s
$t_{PHL2}$	Propagation Delay, /SRn to RST2 (DSR=0 or 1)	$C_L = 5\text{pF}$ , $R_L = 10\text{K}\Omega$ See Figure 7	2.0 to 5.0		210	300	ns

## Capacitance Specifications

$T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = \text{GND}$	4.0	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 5.0V$	5.0	pF

AC Test Circuit and Waveforms

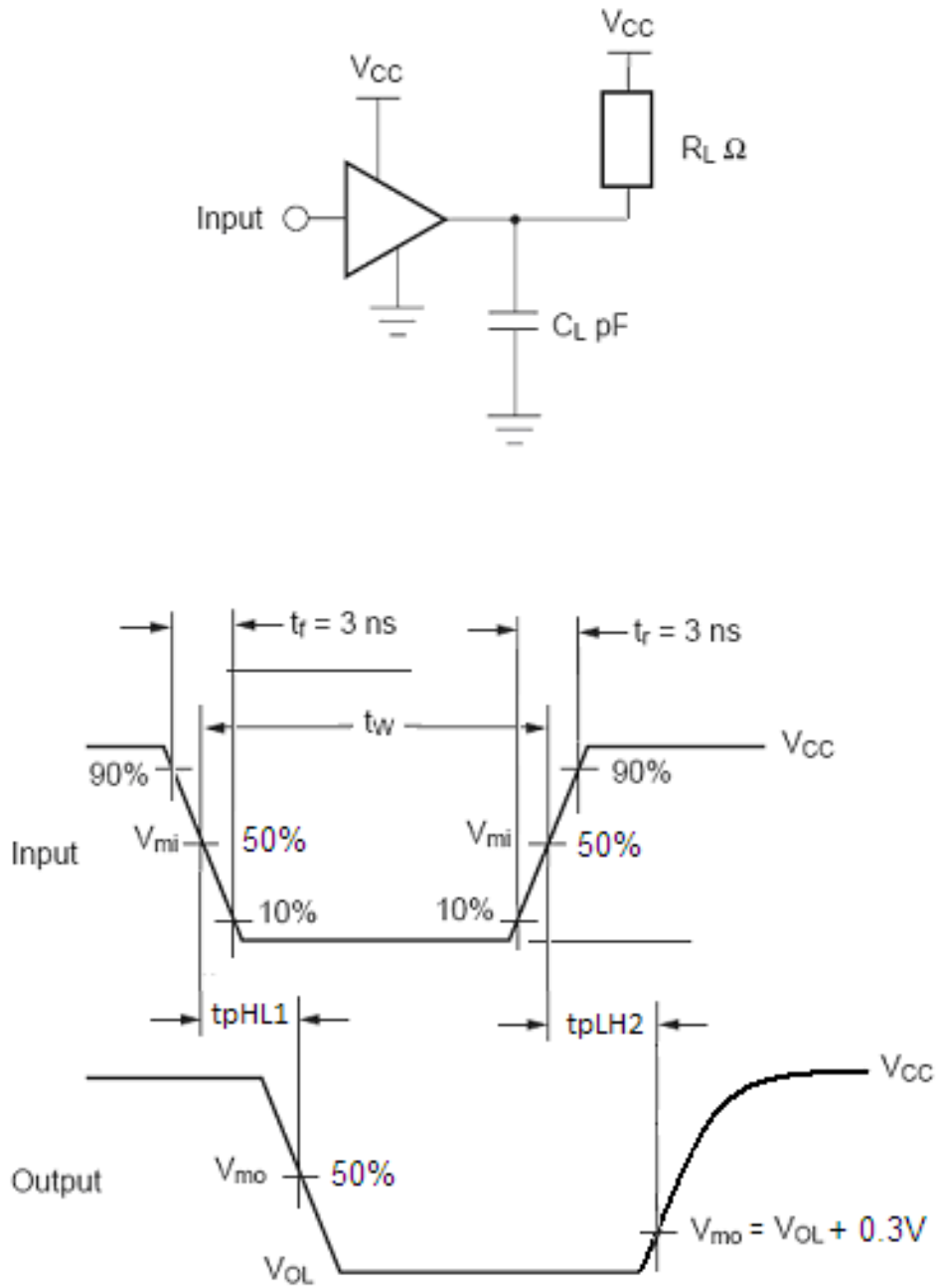


Figure 6. /RST1 Output



AC Test Circuit and Waveforms (Continued)

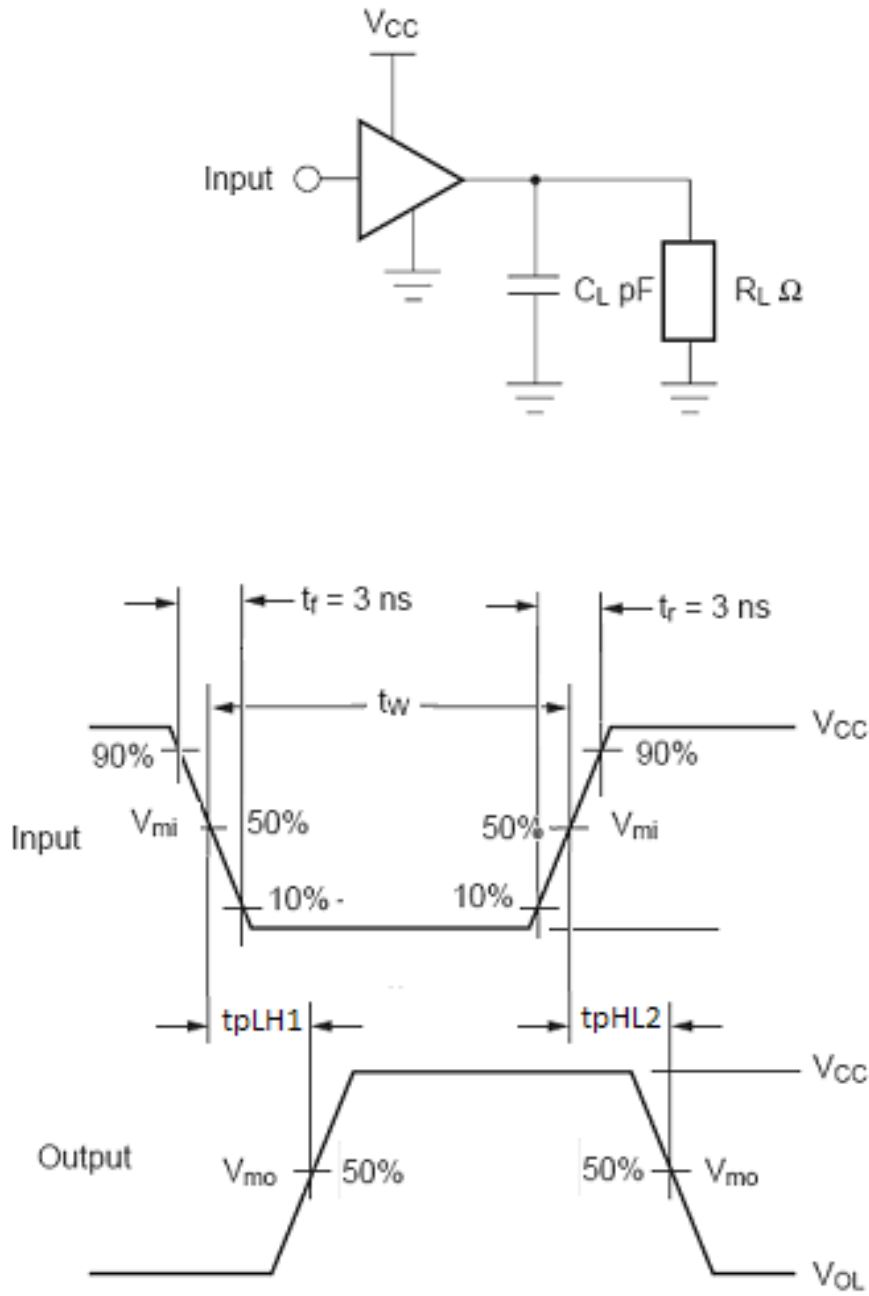
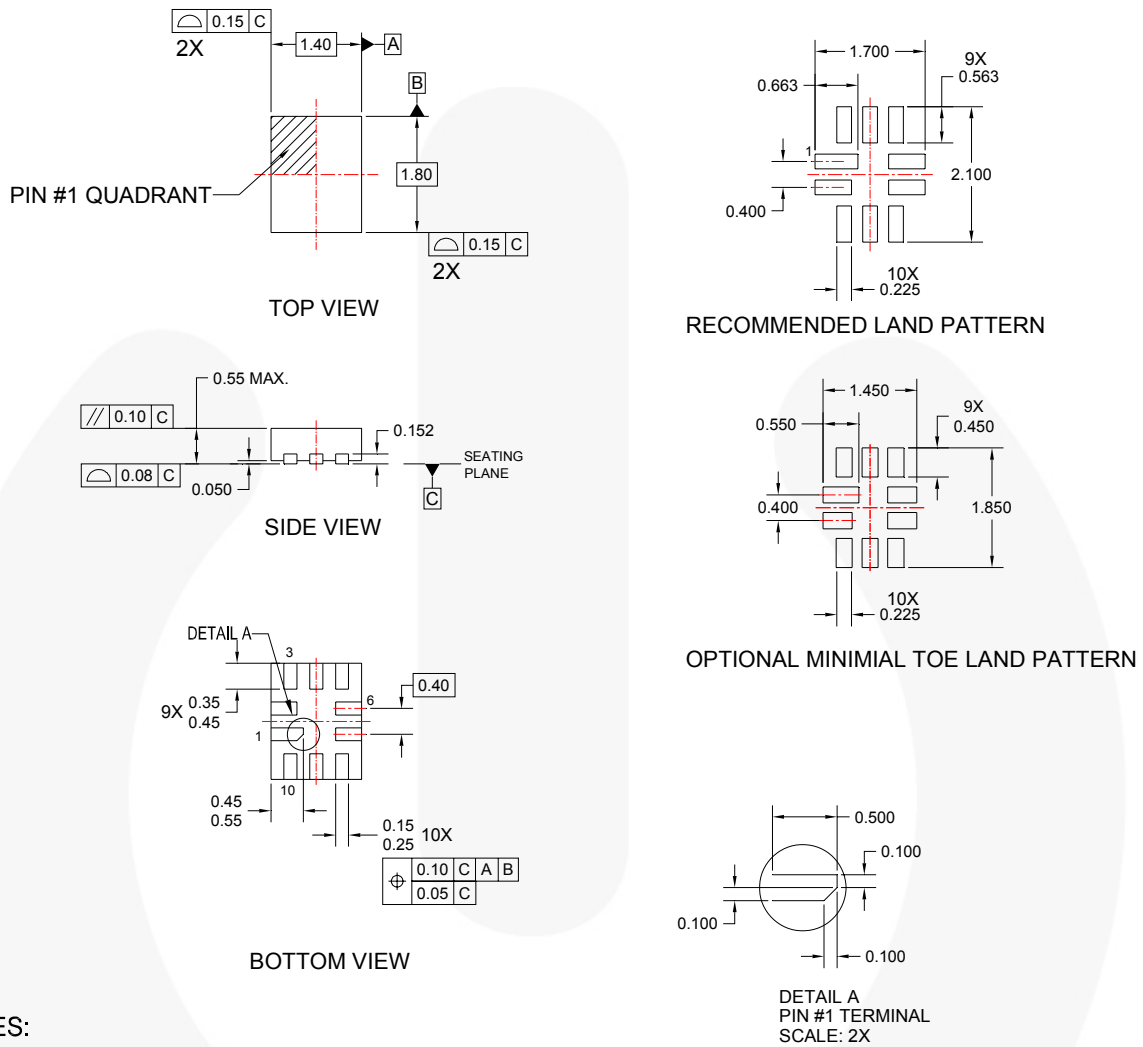


Figure 7. RST2 Output

## Physical Dimensions



### NOTES:

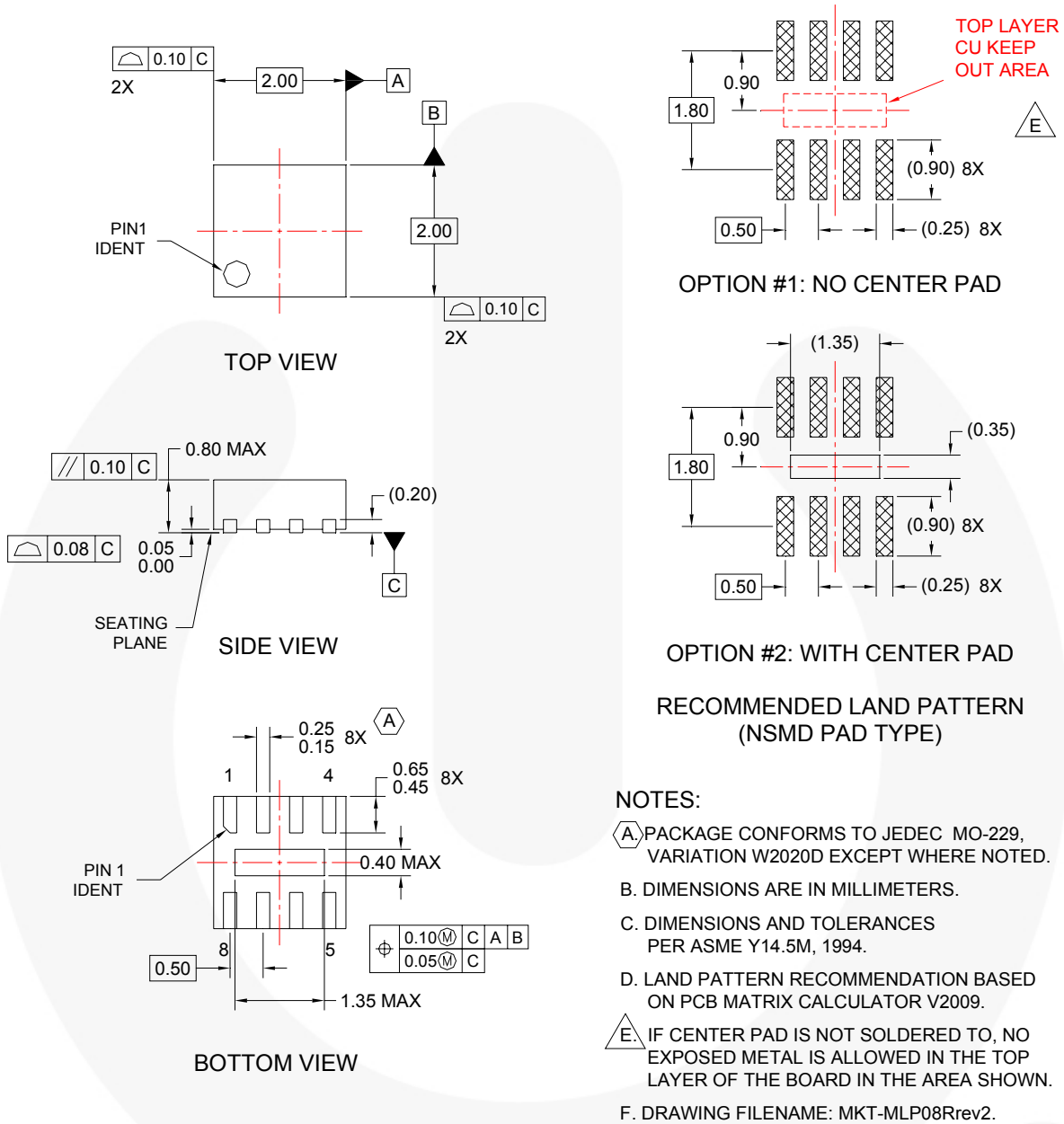
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- B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- C. DRAWING FILENAME: UMLP10Arev2

**Figure 8. 10-Lead Ultrathin MLP, 1.4 x 1.8 x 0.55mm Package**

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**Physical Dimensions (Continued)**



**Figure 9. 8-Lead, Molded Leadless Package (MLP), 2.0 x 2.0 x 0.8mm**





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