



# PCA8802

Smartcard RTC; ultra low power oscillator with integrated counter for initiating one time password generation

Rev. 01 — 19 February 2009

Product data sheet

## 1. General description

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The PCA8802 is a CMOS integrated circuit for battery operation, typically supplied by button cells or flexible polymer batteries. Incorporated is a 32.768 kHz quartz crystal oscillator circuit including the two load capacitors. The circuit is optimized for a quartz with 6 pF load capacitance specification. Higher values can also be used with the addition of external load capacitors.

The main function of the oscillator is to generate a  $\frac{1}{32}$  Hz clock signal which is used to increment a 24 bit binary counter. The counter can be read over the serial interface and may also be set to any desired value. Control over the divider chain also allows for accurate starting of the counter. Incrementing of the counter value during read is prevented by freezing of the counter during access.

An interrupt signal is also available and is triggered coincident with the counter updating. This signal may be used as a wake-up for a microcontroller.

## 2. Features

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- 32.768 kHz quartz oscillator, amplitude regulated with excellent frequency stability and high immunity to leakage currents
- Very low current consumption: typically 130 nA
- Two wire serial interface (I<sup>2</sup>C-bus)
- Integrated 24 bit counter with auto increment every 32 seconds
- Interrupt output for processor wake-up
- Stop function for accurate time setting and current saving during shelf life
- User test modes for accelerated application testing and development
- Two integrated quartz crystal oscillator capacitors

## 3. Applications

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- One time password function generators
- Ultra low power time keeper circuit

## 4. Ordering information

Table 1. Ordering information

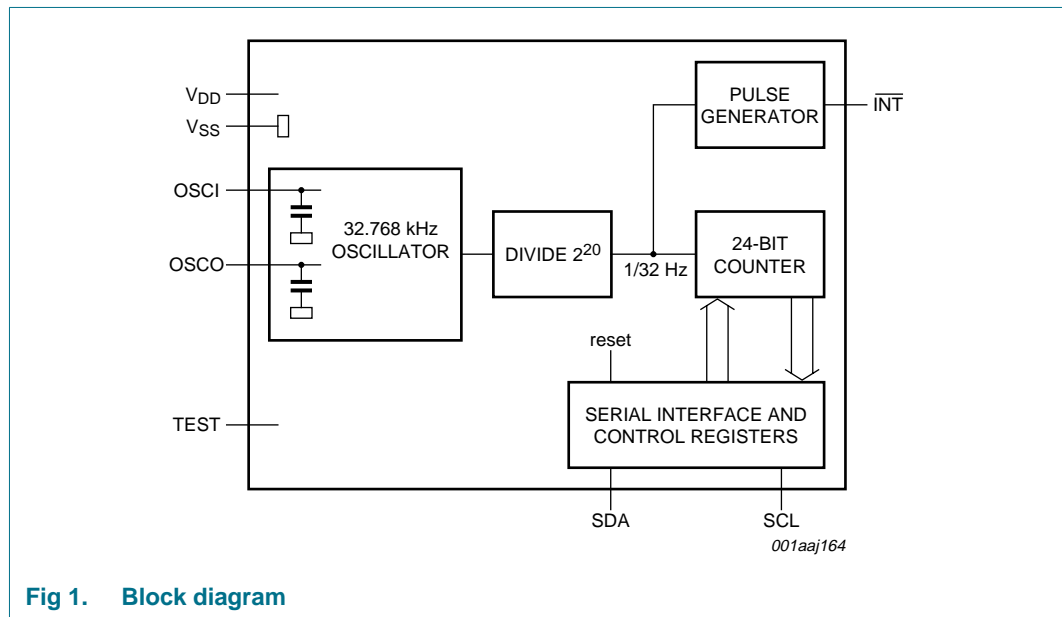
Type number	Package			
	Name	Description	Delivery form	Version
PCA8802CX8/B/1	PCA8802CX	wafer level chip-size package; 8 bumps; 1.19 × 1.14 × 0.29 mm	chip with solder bumps in tape and reel	PCA8802CX
PCA8802U/2AA/1	PCA8802U	wafer level chip-size package; 8 bumps; 1.19 × 1.14 × 0.22 mm	chip with gold bumps in tray	PCA8802U

## 5. Marking

Table 2. Marking codes

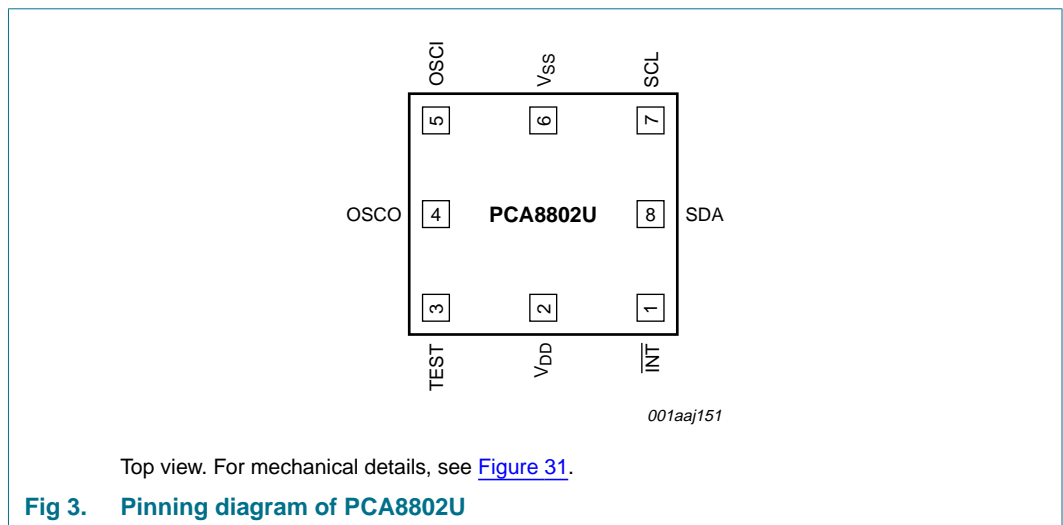
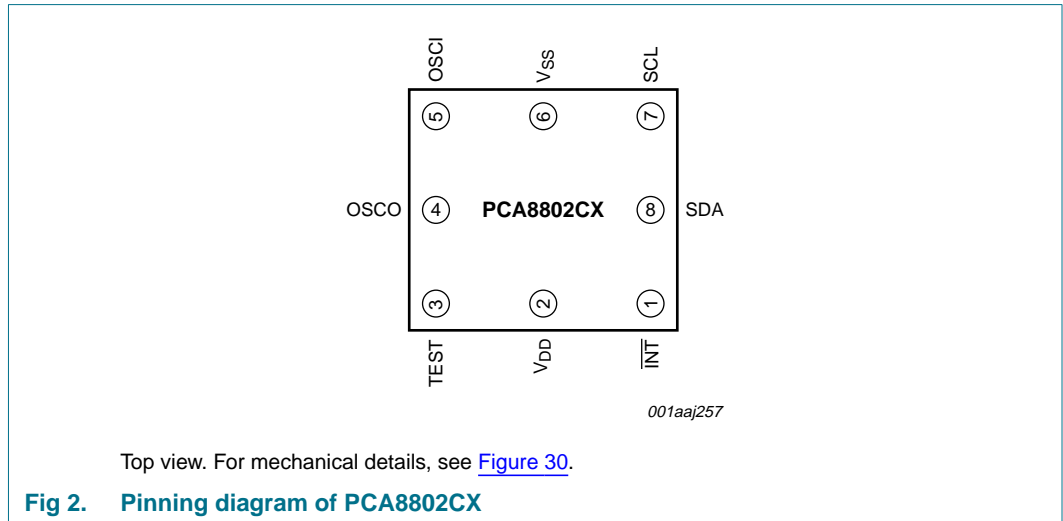
Type number	Marking code
PCA8802CX8/B/1	PC8802-1
PCA8802U/2AA/1	PC8802-1

## 6. Block diagram



## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

Table 3. Pin description for PCA8802

Symbol	Pin	Description
$\overline{\text{INT}}$	1	interrupt and test mode output, push-pull
$V_{\text{DD}}$	2	supply voltage
TEST	3	test pin; must be connected to $V_{\text{SS}}$
OSCO	4	oscillator output
OSCI	5	oscillator input
$V_{\text{SS}}$	6	ground
SCL	7	serial interface, clock
SDA	8	serial interface, bidirectional data line; push-pull

### 8. Device protection diagram

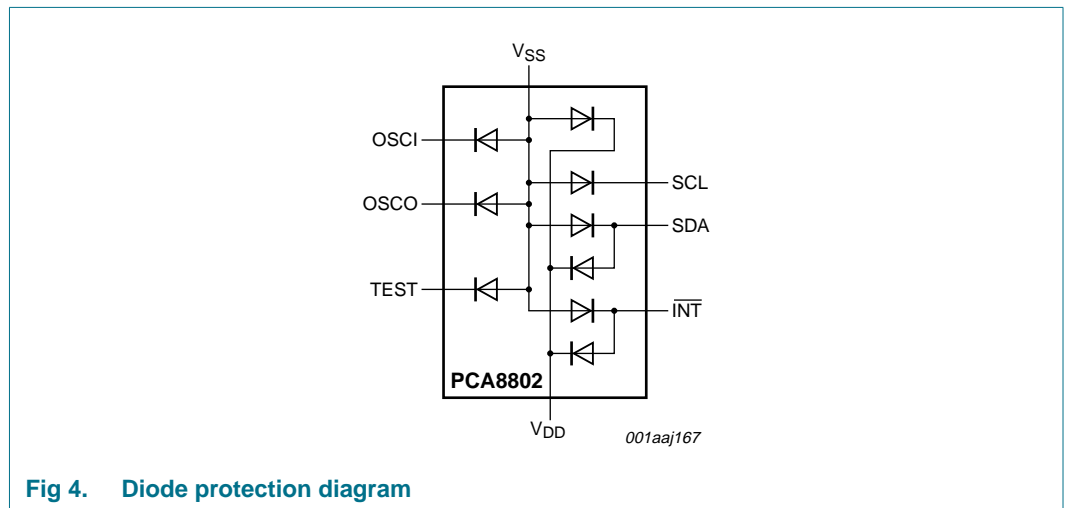


Fig 4. Diode protection diagram

## 9. Functional description

The PCA8802 is an ultra low power device for battery operations. The integrated oscillator circuit generates a  $\frac{1}{32}$  Hz clock signal to increment a 24 bit counter. The communication between the PCA8802 and other devices is made via an I<sup>2</sup>C-bus.

The device is always running but for longer storage time it can be switched off and on again in case of delivery.

The functions of the device can be controlled with the following instruction set:

**Table 4. Instruction set overview**

Instruction	Description	Reference
wrt_cmd	device write access	<a href="#">Section 9.6.2</a>
dvs_cmd	divider start or stop switch	<a href="#">Section 9.6.3</a>
pwd_cmd	low power mode switch	<a href="#">Section 9.6.4</a>
32k_cmd	32.768 kHz clock signal on the pin $\overline{\text{INT}}$ switch	<a href="#">Section 9.6.5</a>
fst_cmd	fast system development mode switch	<a href="#">Section 9.6.6</a>
set_cmd	set counter instruction	<a href="#">Section 9.6.7</a>
rd_cmd	counter read instruction	<a href="#">Section 9.6.8</a>

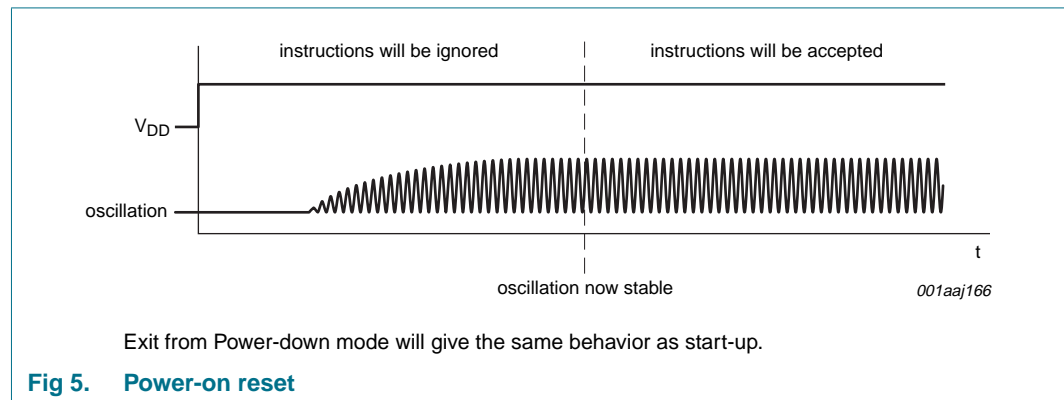
### 9.1 Oscillator

The 32.768 kHz oscillator includes two integrated load capacitors and an automatic gain control to ensure a reliable start-up.

For prototype development and system debugging, it is possible to output a 32.768 kHz square wave on the  $\overline{\text{INT}}$  pin with the 32k\_cmd instruction.

#### 9.1.1 Power-on

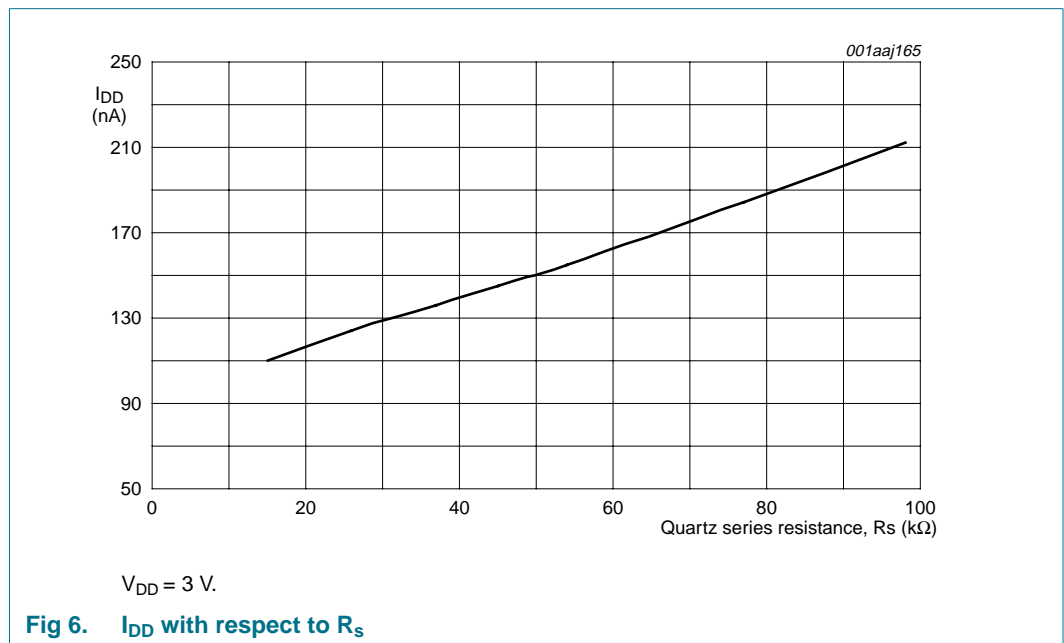
At initial power-on, when the oscillator has not yet started, a reset will be generated. During this state the serial interface will not respond when accessed. To ensure that the oscillator has started and the serial interface is accessible, it is recommended that the master attempts to make write-read accesses to the counter register.



9.1.2 Low power operation

With the power-down instruction (pww\_cmd) the oscillator can be stopped and the device can be put into a low power state where power consumption is reduced to an absolute minimum. The chip would normally reset when the oscillator is stopped, so to prevent a reset of the chip during this state, a special software power-down sequence must be used (see Table 7). In power-down state, the interface is still accessible.

A prime consideration for low power consumption is the series resistance  $R_s$  of the quartz used. The series resistance acts as a loss element. Low  $R_s$  will reduce current consumption further.



9.2 Divider

The divider chain is responsible for reducing the 32.768 kHz oscillator frequency down to  $\frac{1}{32}$  Hz.

The dividers (see Figure 7) divider\_2 and divider\_3 may be reset with the dvs\_cmd instruction. The 24 bit counter may be set when the dividers are held in reset, but this is not a requirement. This allows for accurate setting and restarting of the counter.

The interface is asynchronous to the quartz oscillator and the state of divider\_1 can not be known when the dvs\_cmd is enabled. The 8.192 kHz clock could have just occurred and hence a delay of  $\frac{1}{8192}$  seconds will occur before the next increment of the divider\_2, or the 8.192 kHz clock could be just about to occur and immediately increment the divider\_2.

As a consequence, an uncertainty of between zero and one 8192 Hz clock period (i.e. a time uncertainty of about 0 s to 122  $\mu$ s) will be present when restarting the counter.

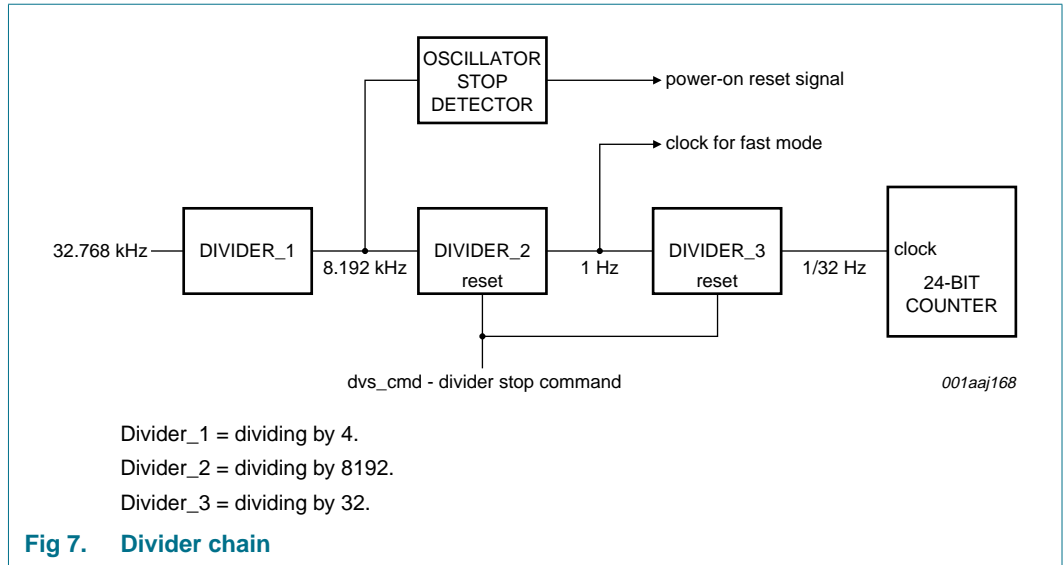


Fig 7. Divider chain

### 9.3 Binary counter

A 24 bit binary roll over counter is implemented. The counter is reset at power-on.

The counter can be set to any value using the `set_cmd` instruction. The `set_cmd` instruction allows partial writing of data. Partial writing of the data parameters will result in partial setting of the counter, e.g. if data transfer is stopped after P1[23:16] (see [Table 5](#)) is transmitted, then only bit 23 to bit 16 will be updated. The counter will not increment whilst being set.

The counter can be halted by means of stopping the dividers using the `dvs_cmd` instruction.

The counter can be read at any time and the counter value will remain stable during reading. If the counter is due to increment during the read or write cycle, then the request to increment will be held off until after the read has concluded. For this reason it is important to read the counter in bursts, ensuring that an interface STOP condition (see [Section 9.5.4](#)) is present between read accesses. Reading for periods of more than 32 seconds at a time will result in loss of counts.

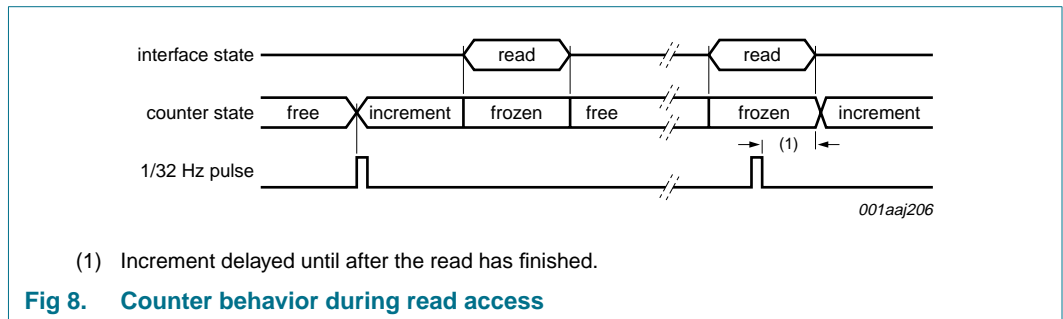


Fig 8. Counter behavior during read access

## 9.4 Pulse generator

An interrupt pulse is available at the  $\overline{\text{INT}}$  pin. This pulse is generated once every 32 seconds and could be used to wake up a microcontroller to perform a periodic function e.g. to calculate and update an LCD display with a new one-time password.

A pulse is generated coincident with the increment of the counter. The new counter value will be available immediately.

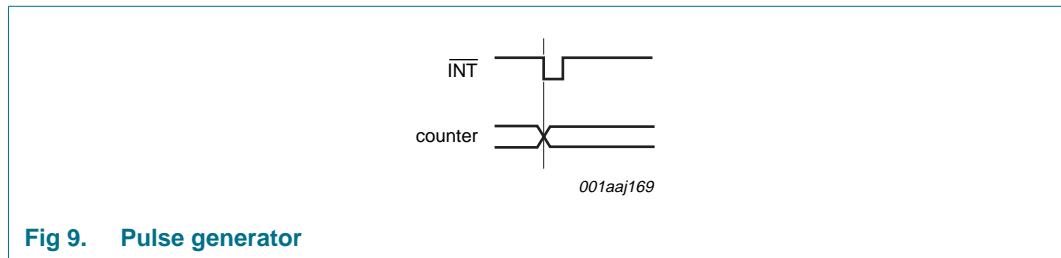


Fig 9. Pulse generator

## 9.5 I<sup>2</sup>C-bus interface

### 9.5.1 Interface protocol

The serial interface is based on the I<sup>2</sup>C-bus protocol. The I<sup>2</sup>C-bus protocol has the advantage of being robust in terms of immunity to electrical noise. Although the PCA8802 does not have the signal filters inside the interface pins, the slave address and acknowledge hand shaking is nevertheless implemented.

For power saving, the SDA output is push-pull instead of the more traditional open-drain output. Push-pull prevents the need for power consuming pull-up resistors, but does limit the operation to point to point only.

The following slave addresses plus a write and read bit are reserved for the PCA8802:

- write: 1010 0000
- read: 1010 0001

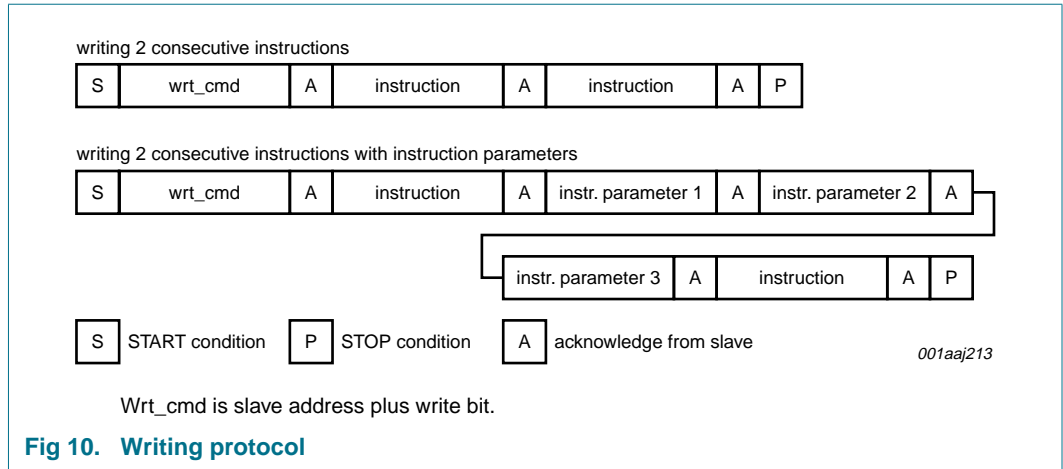
An incorrect slave address will result in the device ignoring all bus data. A STOP or START condition (see [Section 9.5.4](#)) will be required before a new transfer can be made.

#### 9.5.1.1 The writing protocol

The writing protocol is shown in [Figure 10](#).

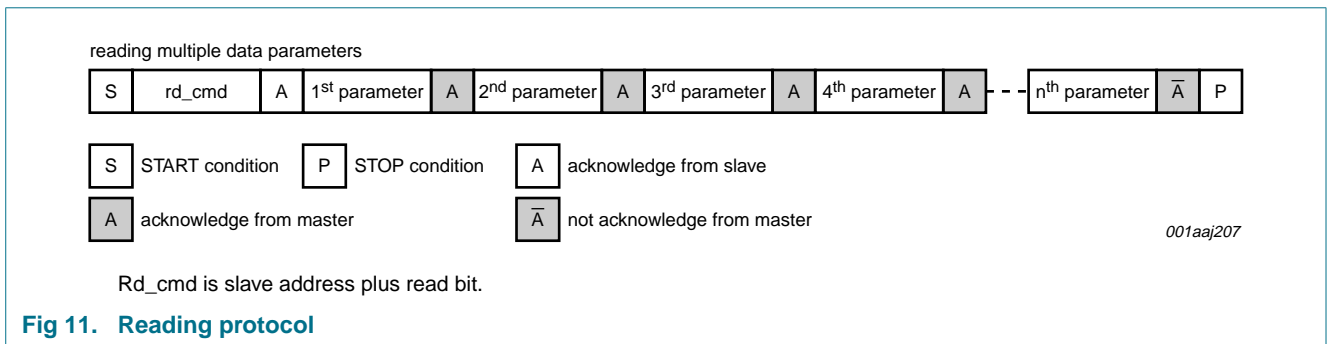
There is no restriction for the order of sending instructions. As many instructions as needed may be sent in one access. The total duration of one access must not exceed 32 seconds (see [Figure 12](#)).





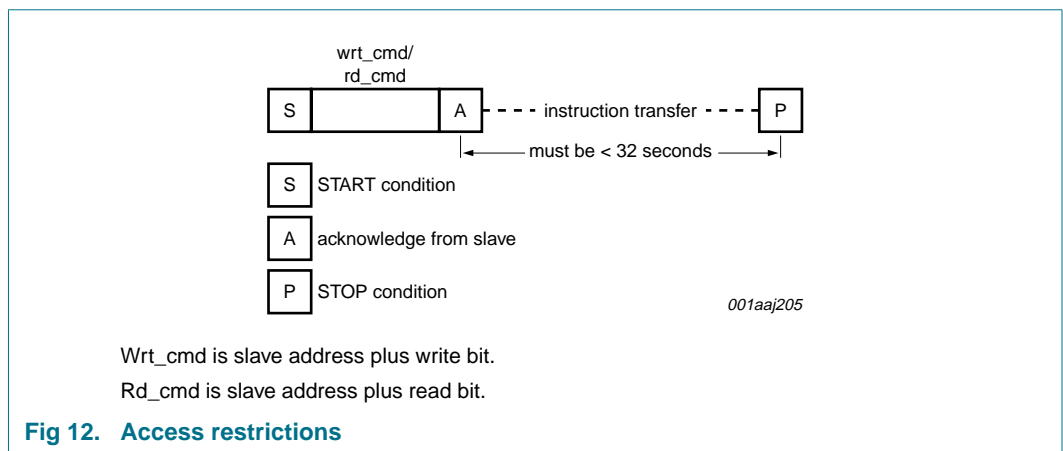
9.5.1.2 The reading protocol

The reading protocol is shown in [Figure 11](#).



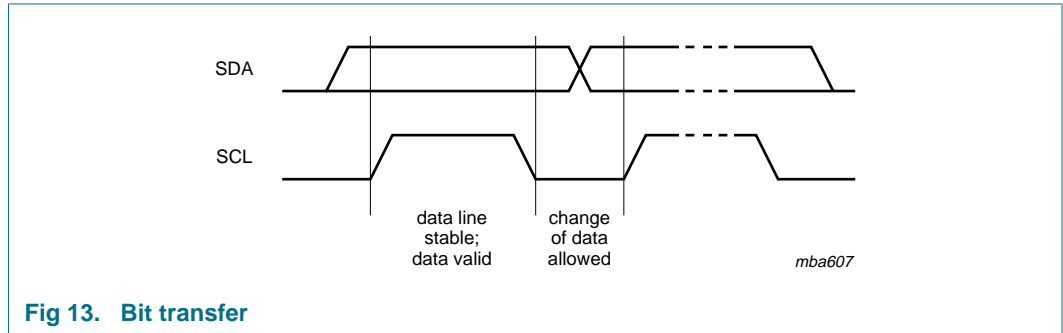
9.5.1.3 Reading and writing limitations

As the counter is frozen during interface accesses, all access must be completed within 32 seconds (see [Figure 12](#)). If this rule is not adhered to, then counts will be dropped.



**9.5.2 Bit transfer**

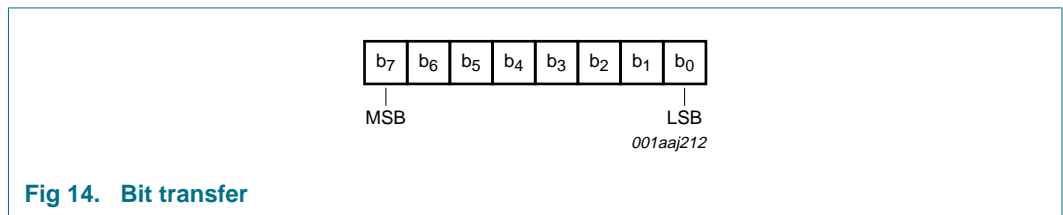
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is shown in [Figure 13](#).



**Fig 13. Bit transfer**

**9.5.3 Bit order**

Data is transferred MSB first.

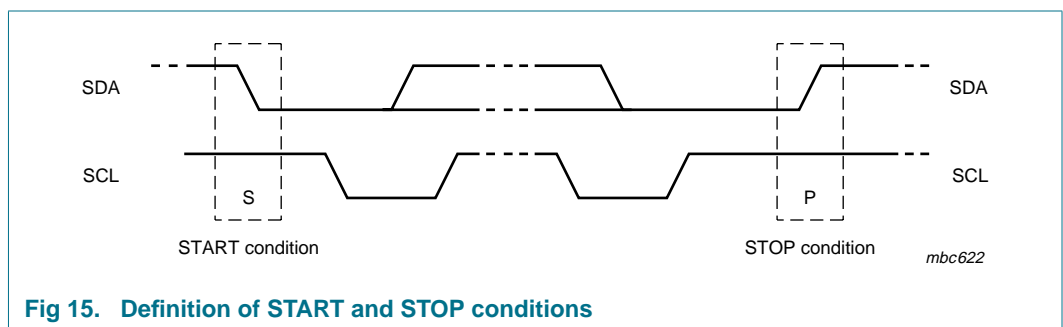


**Fig 14. Bit transfer**

**9.5.4 START and STOP conditions**

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are shown in [Figure 15](#).

The data on SDA is sampled with the rising edge of SCL. Data is output to SDA on the falling edge of SCL.



**Fig 15. Definition of START and STOP conditions**

**9.5.5 System configuration**

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the device which is controlled by the master is the slave.

### 9.5.6 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited, but the duration of the access must not exceed 32 seconds. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement is shown in [Figure 16](#).

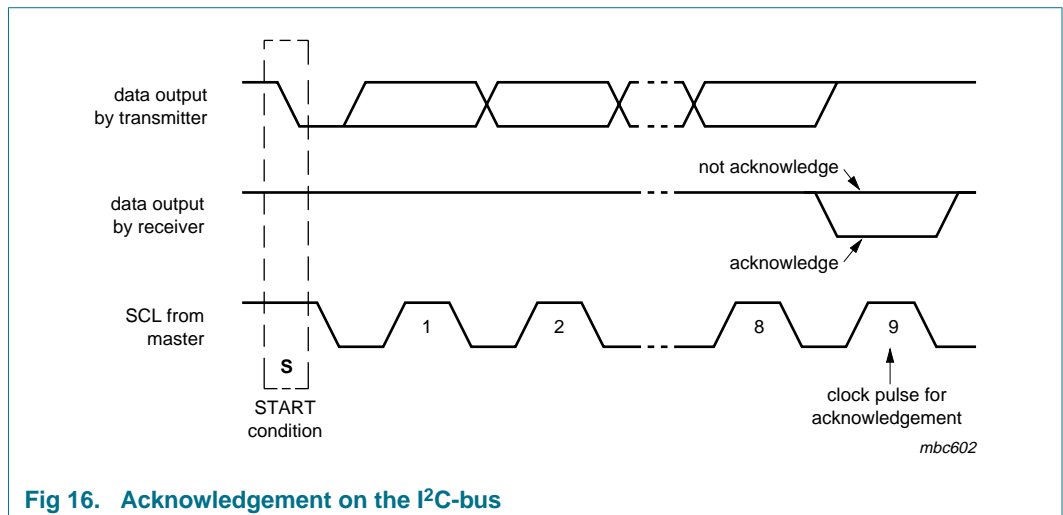


Fig 16. Acknowledgement on the I<sup>2</sup>C-bus

### 9.5.7 Data transfer

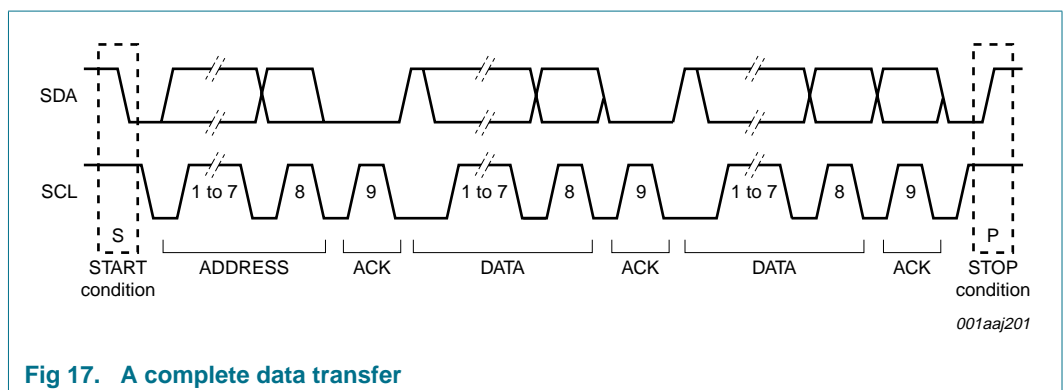
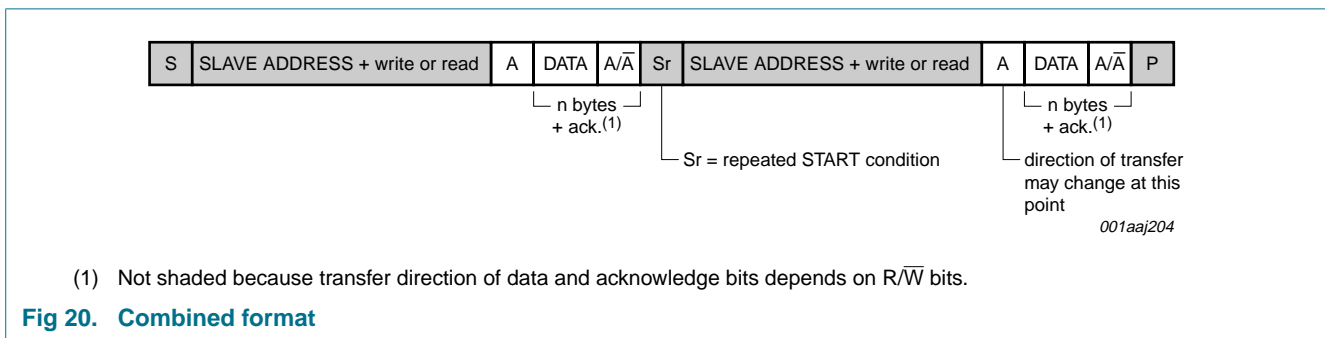
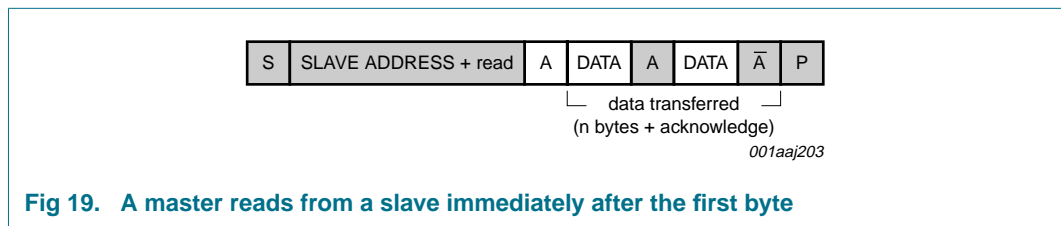
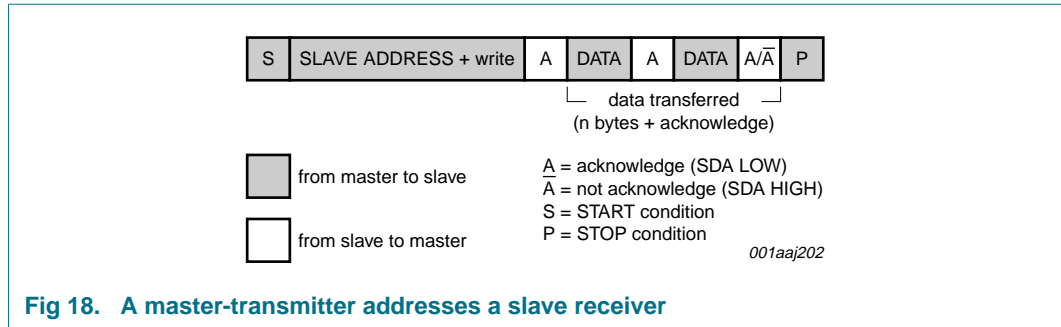
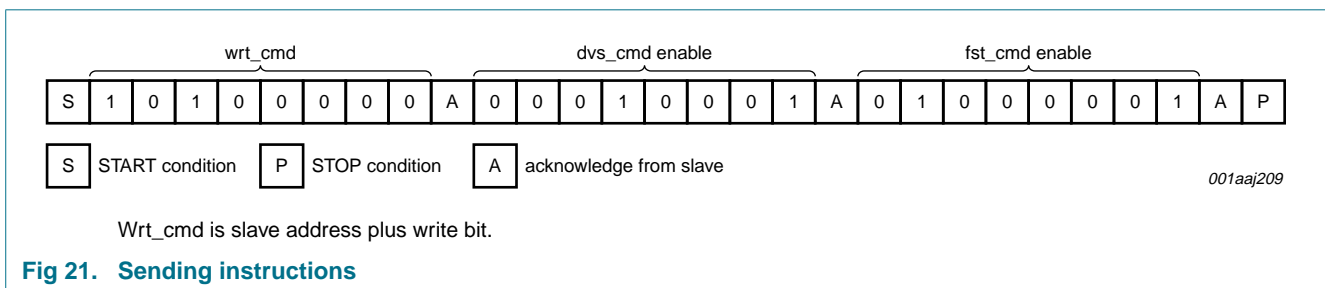


Fig 17. A complete data transfer

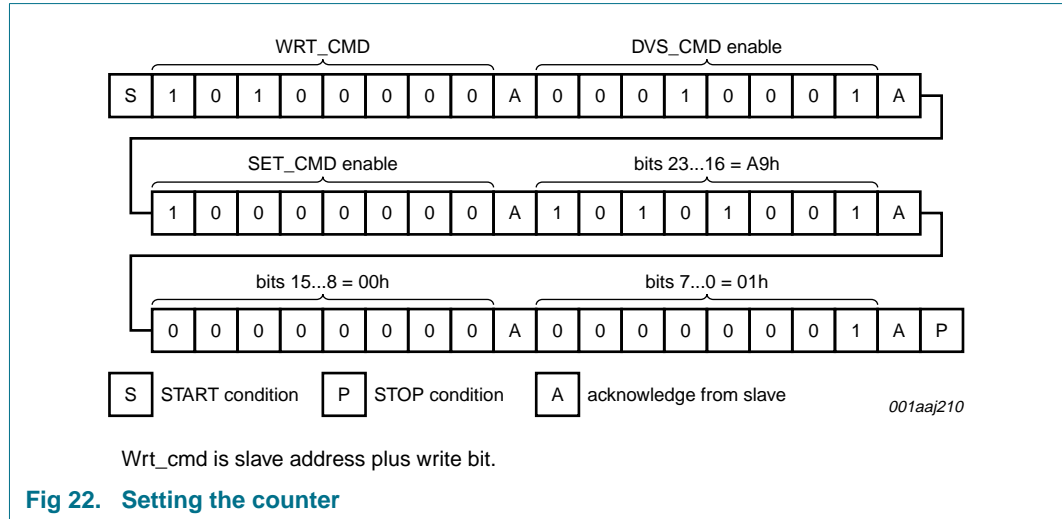


9.5.7.1 Example data transfers

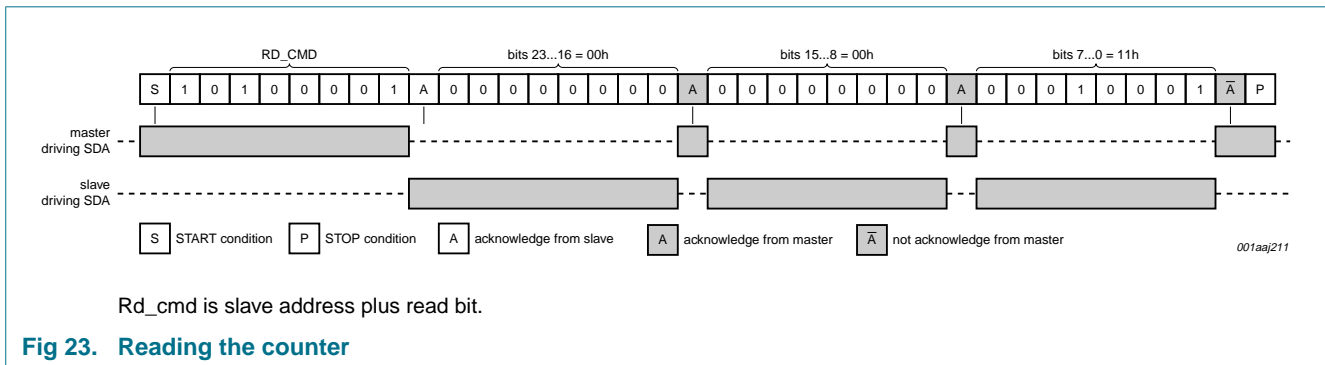
Example 1: Sending the instruction dvs\_cmd followed by fst\_cmd is shown in Figure 21.



**Example 2:** Sending dvs\_cmd followed by setting the counter to A90001h is shown in [Figure 22](#)



**Example 3:** Reading the counter (counter = 000011h) is shown in [Figure 23](#).



## 9.6 Instructions

### 9.6.1 Instruction set

**Table 5. Write instructions**

The writing protocol is illustrated in [Figure 10](#).

First byte		Second byte		Further bytes	Action
Instruction	Instruction code	Instruction	Instruction code	Parameters	
wrt_cmd	1010 0000			-	device slave write address: slave address plus write bit
		dvs_cmd	0001 0001	-	stop and reset dividers
			0001 0000	-	start dividers
		pwd_cmd	0010 0001	-	shut down the device
			0010 0000	-	enable the device
		32k_cmd	0011 0001	-	enable output of 32.768 kHz on pin $\overline{\text{INT}}$
			0011 0000	-	disable output of 32.768 kHz on pin $\overline{\text{INT}}$
		fst_cmd	0100 0001	-	fast mode; increments counter every second
			0100 0000	-	fast mode disable
		set_cmd	1000 0000		set the counter value
				P1[23:16]	parameter with counter values
				P2[15:8]	
				P3[7:0]	

**Table 6. Read instructions**

The reading protocol is illustrated in [Figure 11](#).

First byte		Further bytes	Action
Instruction	Instruction code	Parameters	
rd_cmd <sup>[1]</sup>	1010 0001		device slave read address: slave address plus read bit
		P1[23:16]	parameter with counter values; continues to read until no ACK is received; counter is not updated during this time
		P2[15:8]	
		P3[7:0]	
		P4[23:16]	
		:	

[1] Read of the counter is implicit with an interface read.

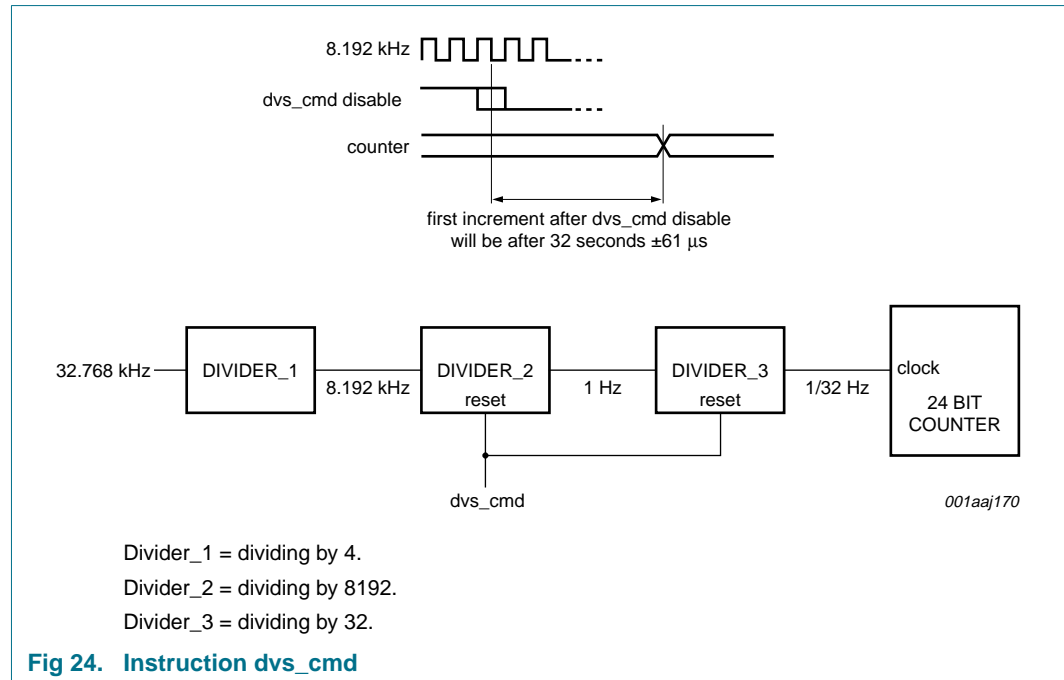
### 9.6.2 Instruction wrt\_cmd

The write instruction (wrt\_cmd) precedes each write sequence. Details of the writing protocol can be found in [Section 9.5.1.1](#).

### 9.6.3 Instruction dvs\_cmd

The divider switch instruction (dvs\_cmd) can be used to freeze the divider chain and to put it in a defined state. The first two bits of the divider chain can not be influenced. With this instruction it is possible to control the time to the next increment of the counter. See [Table 8](#).

When the dividers are restarted, the first increment of the 24 bit counter will be after 32 seconds.



When the dividers are restarted, the 8192 Hz clock could have just occurred and hence a delay of  $\frac{1}{8192}$  seconds will occur before the next increment of the divider\_2, or the 8192 Hz clock could be just about to occur and immediately increment the divider\_2. As a consequence, an uncertainty of one half clock period will be present when restarting (see [Figure 24](#)).

#### 9.6.4 Instruction pwd\_cmd

The power down instruction (pwd\_cmd) is intended to be used to put the system into a low power mode for storage. Static leakage current will be the only power consumed. Storage at temperatures above room temperature may increase leakage currents.

Entering power-down requires a specific sequence of events since under normal circumstances stopping the oscillator would result in a chip reset.

Table 7. Power-down sequence

Step	Action	Code sequence	Note
<b>To enter power-down</b>			
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	enable dvs_cmd	0001 0001	stop the divider
4	set counter with set_cmd	1000 0000	set the counter = AAAAAAh
		1010 1010	P1[23:16]
		1010 1010	P2[15:8]
		1010 1010	P3[7:0]
5	enable pwd_cmd	0010 0001	stop the oscillator
6	end transfer	STOP condition	-
7	device is now in a power-down state	-	-
<b>To exit power-down</b>			
1	initiate transfer	START condition	-
2	send wrt_cmd	1010 0000	-
3	disable pwd_cmd	0010 0000	oscillator starts on the ACK cycle of this instruction
4	disable dvs_cmd	0001 0000	enable the divider again
5	end transfer	STOP condition	-

### 9.6.5 Instruction 32k\_cmd

The 32.768 kHz enable instruction (32k\_cmd) is intended to aid with oscillator characterization during system development. With this instruction it is possible to obtain a 32.768 kHz clock on the  $\overline{\text{INT}}$  pin which may be used for measurement.

This mode does not affect other operation of the chip with the exception of loss of interrupt output.

### 9.6.6 Instruction fst\_cmd

The fast mode instruction (fst\_cmd) is intended to enable faster system development. When enabled, the counter will increment once every second instead of once every 32 seconds. Interrupt pulses will also be generated once every second.

When using fst\_cmd, data access to the device must be completed within 1 second, if not then counter increments will be lost. The 1 second period is measured from the ACK cycle of a valid slave address to the next STOP or repeated START. A repeated START will be sufficient to allow the counter to increment.

### 9.6.7 Instruction set\_cmd

The counter can be set to any value using the set instruction (set\_cmd). Partial writing of the data parameters will result in partial setting of the counter. E.g. if data transfer is stopped after P1[23:16] is transmitted, then only bit 23 to bit 16 will be updated.



This instruction takes only 3 parameters in one command. Data after the 3rd parameter will be interpreted as the next instruction.

Accurate setting and start-up can be implemented using the `dvs_cmd` instruction in cooperation with the `set_cmd` instruction. An example is shown in [Table 8](#).

**Table 8. Example of accurate setting of the counter**

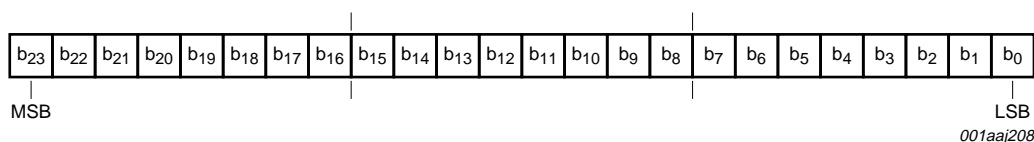
Step	Action	Code sequence	Note
1	initiate transfer	START condition	-
2	send <code>wrt_cmd</code>	1010 0000	-
3	enable <code>dvs_cmd</code>	0001 0001	-
4	set counter with <code>set_cmd</code>	1000 0000	set the counter = 1
		0000 0000	P1[23:16]
		0000 0000	P2[15:8]
		0000 0001	P3[7:0]
5	end transfer	STOP condition	-
6	wait for an external time marker	-	-
7	initiate transfer	START condition	-
8	send <code>wrt_cmd</code>	1010 0000	-
9	disable <code>dvs_cmd</code>	0001 0000	counter starts on the ACK cycle of this instruction
10	end transfer	STOP condition	-

### 9.6.8 Instruction `rd_cmd`

With the read instruction (`rd_cmd`) the counter value can be read at any time. When the counter value is read, the counter is frozen so that there will be no changes during the read back. After a read is terminated, the counter will be allowed to increment again. Any increment that was scheduled during the frozen period will then be effected.

Reading the counter is cyclic i.e. the device will repeatedly return the present counter value until the read is terminated. Reading the counter more than once may be useful in the case that the application is subject to a strong Electromagnetic Interference (EMI) environment so that read back values can be compared.

Read back must be terminated within 32 seconds else a count will be dropped.



**Fig 25. Read bit order**

## 9.7 Reset

As described in [Section 9.1](#), the device will be in reset when the oscillator is stopped with the exception of a controlled power-down using the `pwd_cmd`. The state of the device after reset is shown in [Table 9](#).

**Table 9. Reset state**

Instruction name	State after reset
<code>dvs_cmd</code>	disabled
<code>pwd_cmd</code>	disabled
<code>32k_cmd</code>	disabled
<code>fst_cmd</code>	disabled
24 bit counter	000000h

## 10. Limiting values

**Table 10. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+6.5	V
$I_{DD}$	supply current		-50	+50	mA
$V_I$	input voltage		-0.5	+6.5	V
$I_I$	input current		-10	+10	mA
$V_O$	output voltage		-0.5	+6.5	V
$I_O$	output current		-10	+10	mA
$P_{tot}$	total power dissipation		-	300	mW
$V_{esd}$	electrostatic discharge voltage	HBM	[1] -	±2500	V
		MM	[2] -	±200	V
$I_{lu}$	latch-up current		[3] -	200	mA
$T_{amb}$	ambient temperature		-40	+85	°C
$T_{stg}$	storage temperature		[4] -65	+150	°C

[1] Pass level; Human Body Model (HBM) according to JESD22-A114.

[2] Pass level; Machine Model (MM), according to JESD22-A115.

[3] Pass level; Latch-up testing, according to JESD78.

[4] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

## 11. Static characteristics

**Table 11. Static characteristics**

$V_{DD} = 1.6\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $f_{osc} = 32.768\text{ kHz}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; quartz crystal:  $R_s = 30\text{ k}\Omega$ ,  $C_L = 6.0\text{ pF}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage		1.6	-	5.5	V
		$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; $f_{SCL} = 0\text{ Hz}$	-	1.0	-	V
$\Delta V_{DD}$	supply voltage variation	$\Delta V/\Delta t = 1\text{ V}/\mu\text{s}$	-	0.25	-	V
$I_{DD}$	supply current	power-down active	[1]			
		$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; $V_{DD} = 3\text{ V}$ ; $f_{SCL} = 0\text{ Hz}$	-	3	-	nA
		device running				
		$f_{SCL} = 0\text{ Hz}$	-	-	400	nA
		$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; $V_{DD} = 3\text{ V}$ ; $f_{SCL} = 0\text{ Hz}$	-	130	-	nA
		interface active				
		$f_{SCL} = 100\text{ kHz}$	-	5	20	$\mu\text{A}$
		$f_{SCL} = 1\text{ MHz}$	-	50	100	$\mu\text{A}$
<b>Oscillator</b>						
$V_{start}$	start voltage		-	1.1	-	V
$t_{startup}$	start-up time		-	0.2	-	s
$C_{L(itg)}$	integrated load capacitance		[2]	6.0	-	pF
<b>Inputs</b>						
$V_{IL}$	LOW-level input voltage		-	-	$0.3V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
$V_I$	input voltage	on pins SCL, OSCI, TEST	-0.5	-	5.5	V
		on pin SDA	-0.5	-	$V_{DD} + 0.5$	V
$I_{LI}$	input leakage current	$V_I = V_{DD}$ or $V_{SS}$ ; on pins SCL, SDA and TEST	-200	0	+200	nA
<b>Outputs</b>						
$V_O$	output voltage		-0.5	-	$V_{DD}+0.5$	V
$I_{OH}$	HIGH-level output current	$V_{OH} = 4.0\text{ V}$ ; $V_{DD} = 5\text{ V}$ ; on pins INT and SDA	-	5	2	mA
		$V_{OH} = 1.28\text{ V}$ ; $V_{DD} = 1.6\text{ V}$ ; on pins INT and SDA	-	0.5	0.2	mA

**Table 11. Static characteristics ...continued**

$V_{DD} = 1.6\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $f_{osc} = 32.768\text{ kHz}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; quartz crystal:  $R_s = 30\text{ k}\Omega$ ,  $C_L = 6.0\text{ pF}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OL}$	LOW-level output current	$V_{OL} = 1.0\text{ V}$ ; $V_{DD} = 5\text{ V}$ ; on pins INT and SDA	-2	-7	-	mA
		$V_{OL} = 0.32\text{ V}$ ; $V_{DD} = 1.6\text{ V}$ ; on pins INT and SDA	-0.4	-1	-	mA
$I_{LO}$	output leakage current	$V_O = V_{DD}$ or $V_{SS}$ ; on pins SDA and INT	-200	0	+200	nA

[1] Unless otherwise defined,  $I_{DD}$  is measured with the reset state, see [Section 9.7](#).

[2] Integrated load capacitance,  $C_{L(itg)}$ , is a calculation of  $C_{OSCI}$  and  $C_{OSCO}$  in series:  $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$ .

## 12. Dynamic characteristics

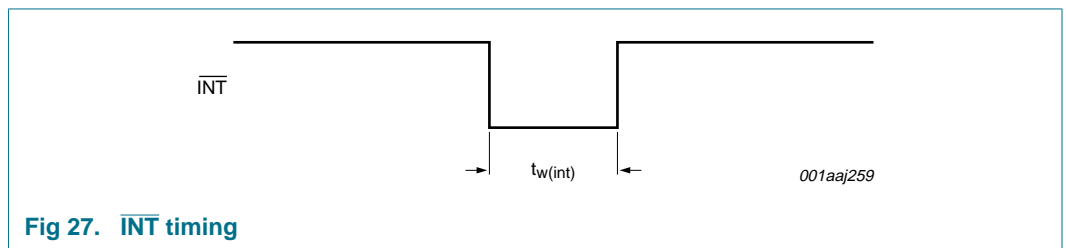
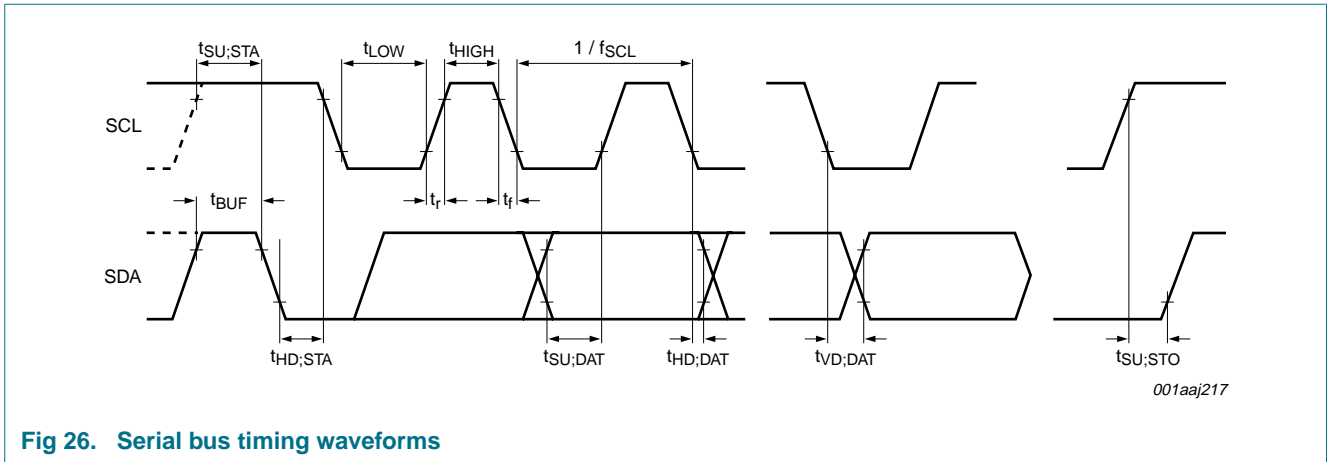
**Table 12. Dynamic characteristics**

$V_{DD} = 1.6\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified. [\[1\]](#)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Timing characteristics: serial bus</b>						
$f_{SCL}$	SCL clock frequency		-	-	1	MHz
$t_{LOW}$	LOW period of the SCL clock		500	-	-	ns
$t_{HIGH}$	HIGH period of the SCL clock		260	-	-	ns
$t_{BUF}$	bus free time between a STOP and START condition		500	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		260	-	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		260	-	-	ns
$t_r$	rise time of both SDA and SCL signals	<a href="#">[2]</a>	-	10	-	ns
$t_f$	fall time of both SDA and SCL signals	<a href="#">[2]</a>	-	10	-	ns
$t_{SU;DAT}$	data set-up time		50	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		260	-	-	ns
$t_{VD;DAT}$	data valid time		75	-	450	ns
$C_b$	capacitive load for each bus line		-	-	50	pF
<b>Timing characteristics: INT</b>						
$t_{w(int)}$	interrupt pulse width		20	40	80	$\mu\text{s}$

[1] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

[2] Rise and fall times are not limited. Fast edges may lead to system EMI problems, whilst slow edges are susceptible to noise.



## 13. Bare die information

### 13.1 Locations

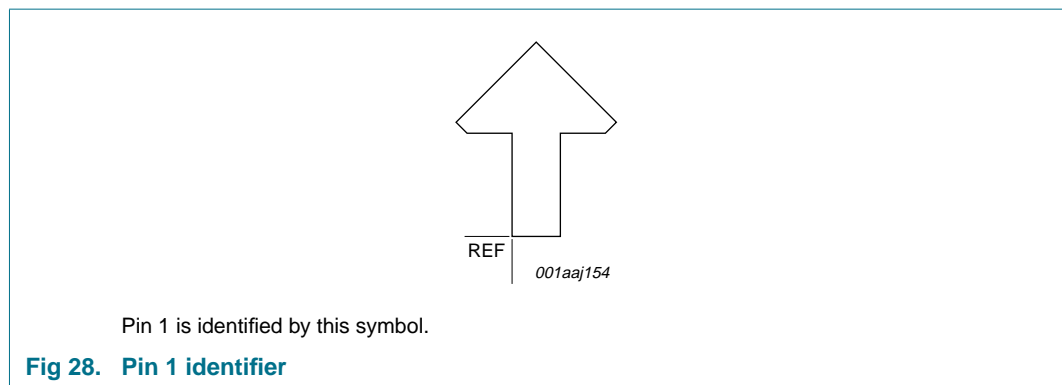
Table 13. Bump and reference point locations

Symbol	Pad	Coordinates <sup>[1]</sup>	
		x	y
$\overline{\text{INT}}$	1	437	-396
V <sub>DD</sub>	2	-12	-430
TEST	3	-460	-396
OSCO	4	-460	1
OSCI	5	-460	396
V <sub>SS</sub> <sup>[2]</sup>	6	-12	430
SCL	7	437	396
SDA	8	437	1
pin 1 identifier	-	474.7	-472.0
bottom left die corner <sup>[3]</sup>	-	-594.8	-568.2
top right die corner <sup>[3]</sup>	-	594.7	568.3

[1] All coordinates are referenced, in  $\mu\text{m}$ , to the center of the die (see [Figure 30](#) and [Figure 31](#)).

[2] The substrate (rear side of the die) is wired to V<sub>SS</sub> but should not be electrically connected.

[3] Die size before dicing. Final dimensions will be 10  $\mu\text{m}$  to 20  $\mu\text{m}$  smaller.

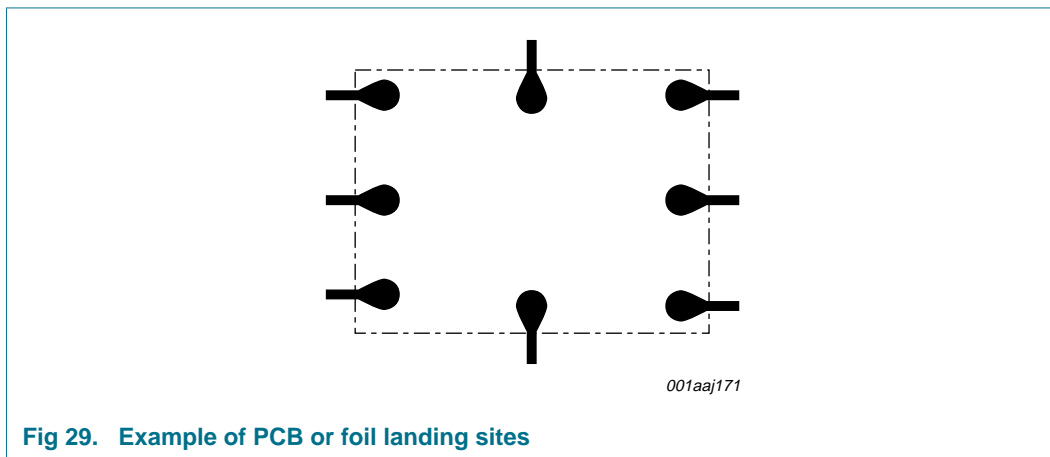


### 13.2 PCB or foil landing site

The layout of the landing sites is important. It is recommended to follow the following guidelines

1. All landing sites should be the same size. When one site has a different size or shape, e.g. to indicate pad one, then the pull on the die produced by the surface tension of the solder will be different in one place. This variation can lead to the die not laying flat on the Printed-Circuit Board (PCB) or foil. This can also result in weak solder joints for some pins.
2. It is recommended to use circular landing sites of the same diameter as the solder ball. This will help with self alignment. Solder bump dimensions may be found in [Figure 30](#).

3. If no solder resist is used on the PCB or foil, then consideration should be given to the amount of run-off of the solder along the track connected to the landing site. Uneven run-off may result in similar problems as described in 1.



**Fig 29. Example of PCB or foil landing sites**



14. Bare die outline

WLCSP8: wafer level chip-size package; 8 bumps; 1.19 x 1.14 x 0.29 mm

PCA8802CX

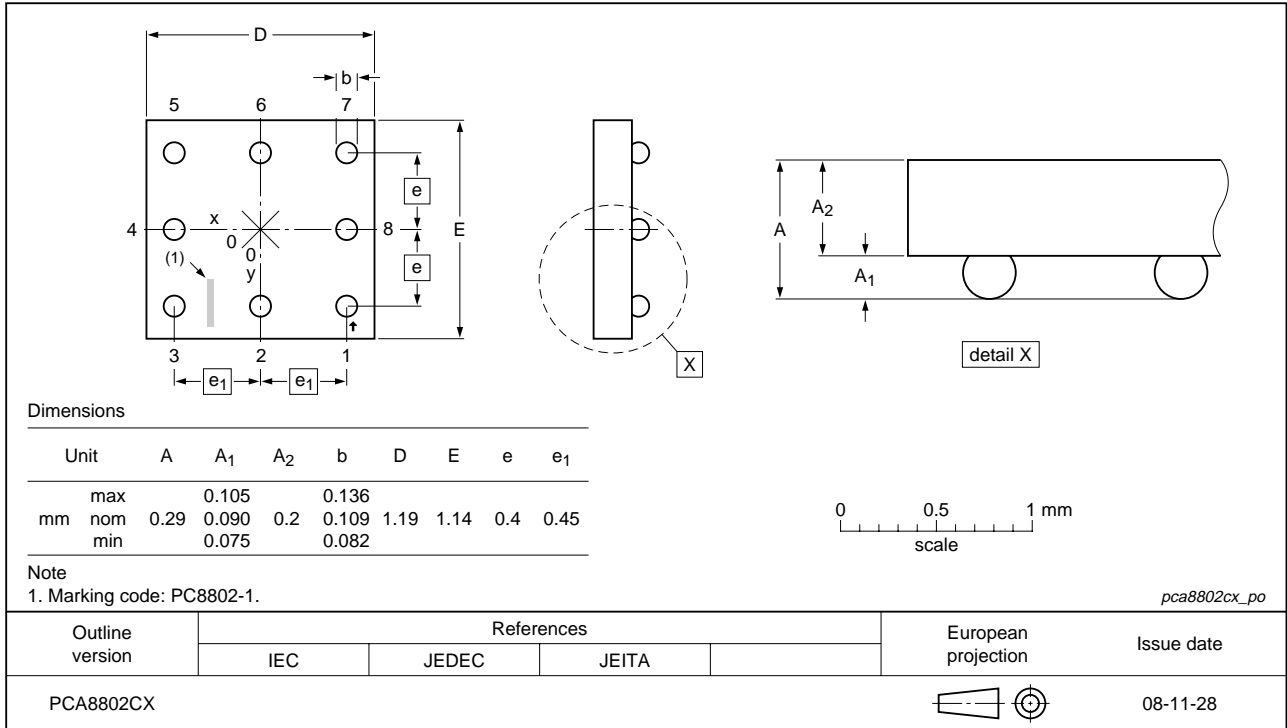


Fig 30. Bare die outline PCA8802CX

WLCSP8: wafer level chip-size package; 8 bumps; 1.19 x 1.14 x 0.22 mm

PCA8802U

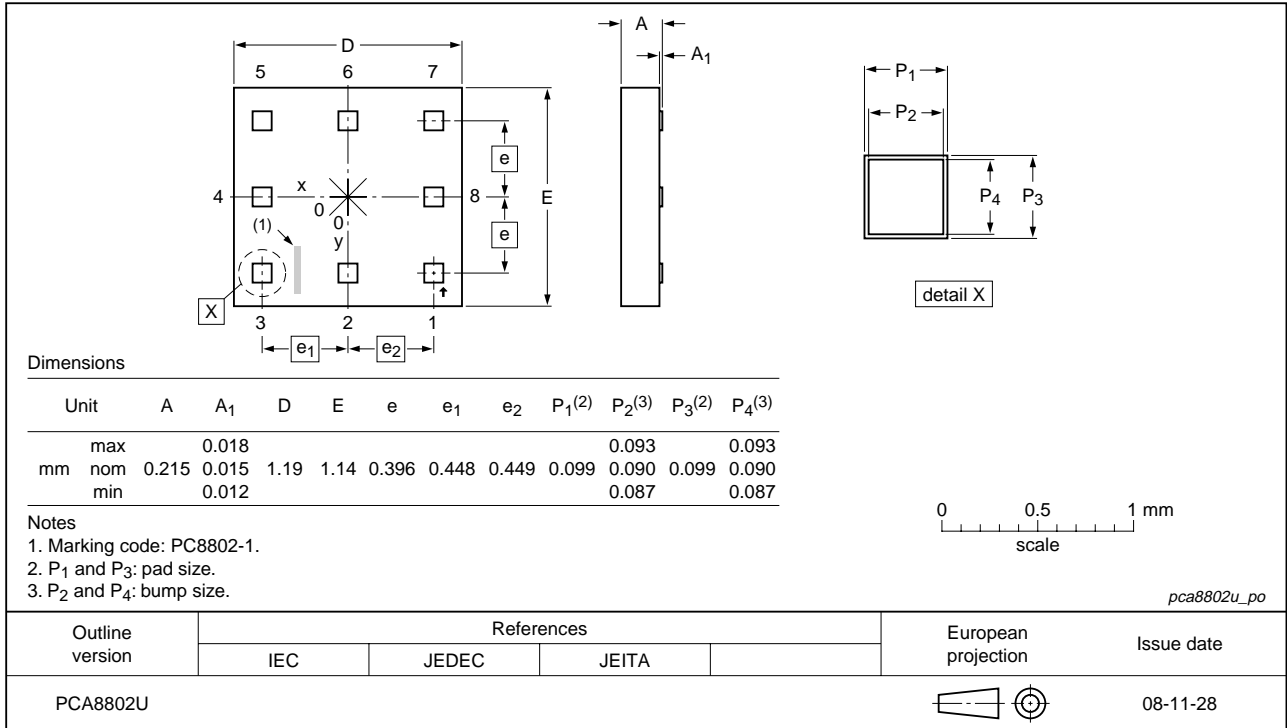


Fig 31. Bare die outline PCA8802U

## 15. Packing information

### 15.1 Tray information

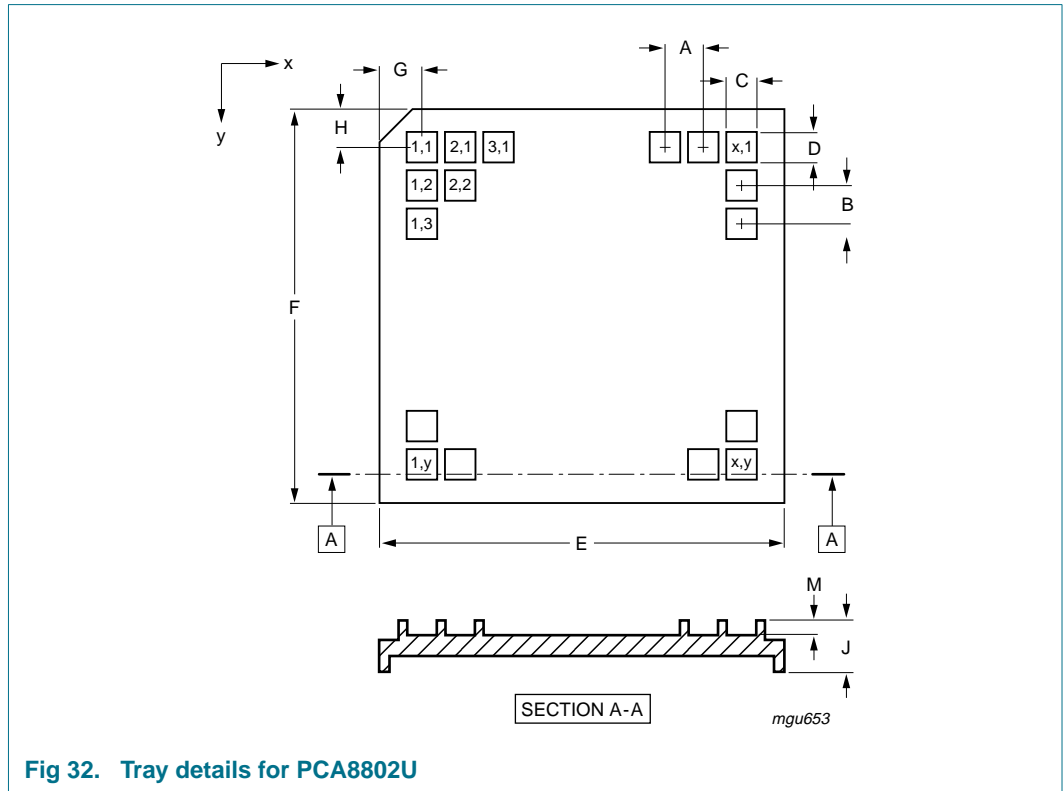


Fig 32. Tray details for PCA8802U

Table 14. Tray dimensions [1]

Dimension	Description	Value
A	pocket pitch; x direction	3.1 mm
B	pocket pitch; y direction	3.1 mm
C	pocket width; x direction	1.29 mm
D	pocket width; y direction	1.24 mm
E	tray width; x direction	50.8 mm
F	tray width; y direction	50.8 mm
G	distance from cut corner to pocket (1,1) center	5.25 mm
H	distance from cut corner to pocket (1,1) center	5.25 mm
J	tray thickness	3.96 mm
M	pocket depth	0.5 mm
x	number of pockets in x direction	14
y	number of pockets in y direction	14

[1] Die is placed in pocket bump side up.

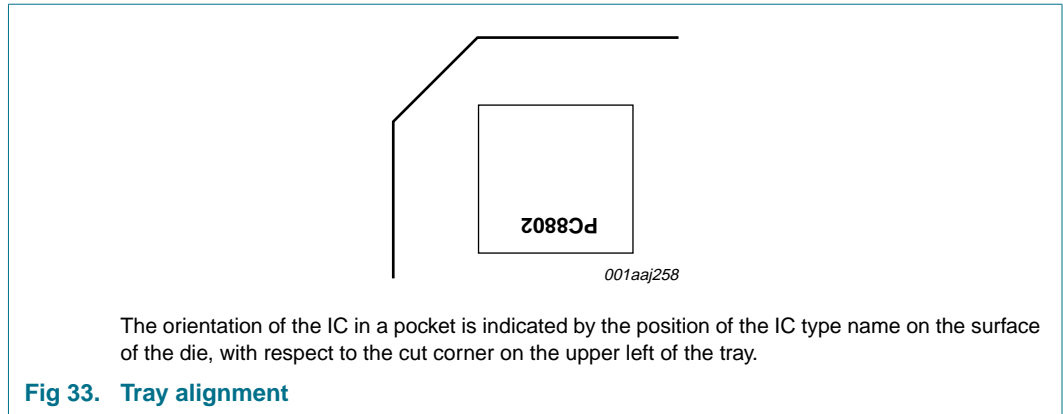


Fig 33. Tray alignment

### 15.2 Tape and reel

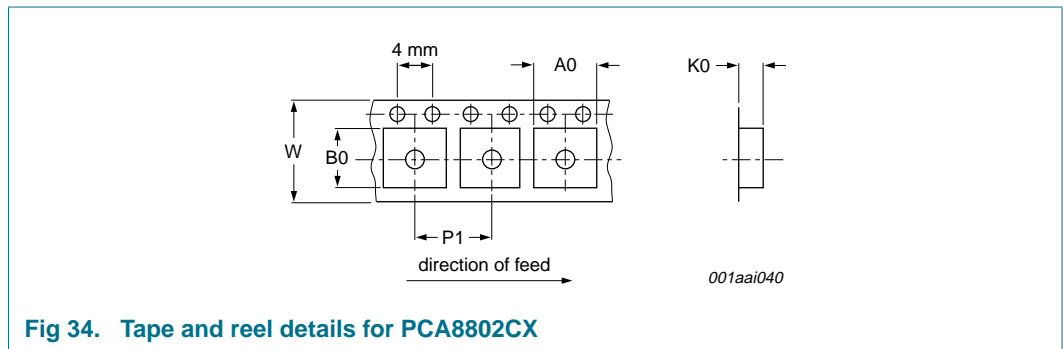


Fig 34. Tape and reel details for PCA8802CX

Table 15. Tape and reel dimensions [1]

Dimension	Description	Value
W	tape width	8.0 mm
A0	pocketed length	1.3 mm
B0	pocket width	1.3 mm
K0	pocket depth	0.5 mm
P1	pocket pitch	4.0 mm

[1] Die is placed in pocket bump side down.

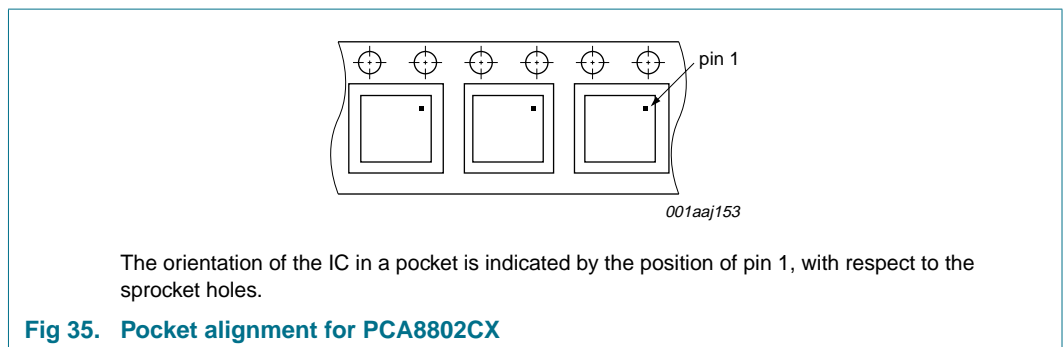


Fig 35. Pocket alignment for PCA8802CX

## 16. Soldering of WLCSP packages

### 16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note AN10439 "Wafer Level Chip Scale Package" and in application note AN10365 "Surface mount reflow soldering description".

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

### 16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

### 16.3 Reflow soldering

Key characteristics in reflow soldering are:

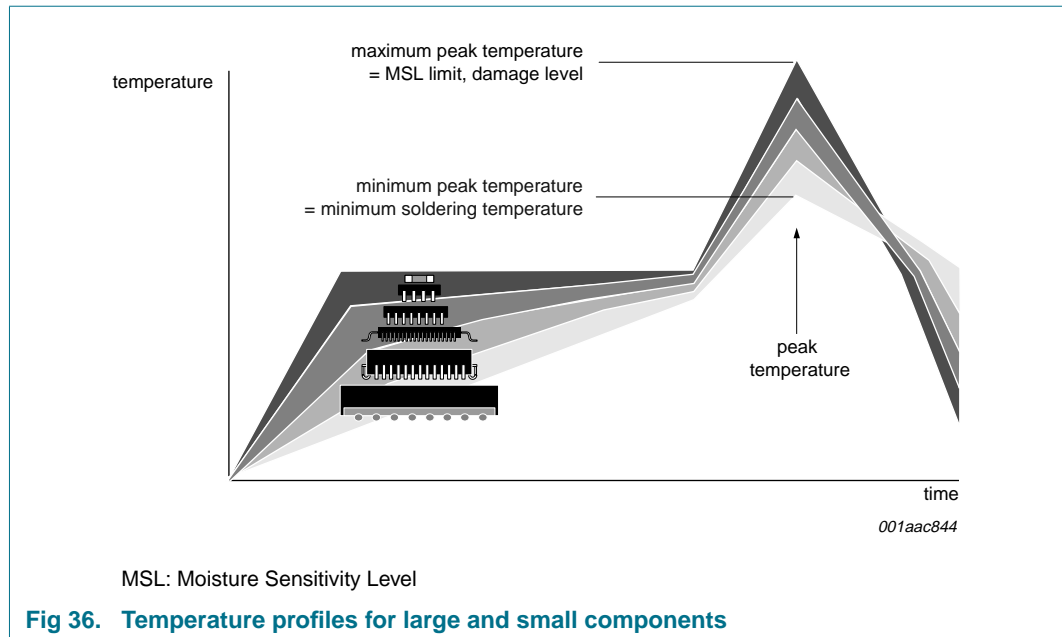
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 36](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 16](#).

**Table 16. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 36](#).



For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

### 16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

### 16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

### 16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note AN10365 "Surface mount reflow soldering description".

#### 16.3.4 Cleaning

Cleaning can be done after reflow soldering.

## 17. Abbreviations

**Table 17. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
EMI	ElectroMagnetic Interference
HBM	Human Body Model
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
PCB	Printed-Circuit Board
RTC	Real Time Clock
WLCSP	Wafer Level Chip-Size Package

## 18. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8802_1	20090219	Product data sheet	-	-



## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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