

## 3.3V Low Skew 1-to-4 LVTTL/LVCMOS to LVDS Fanout Buffer

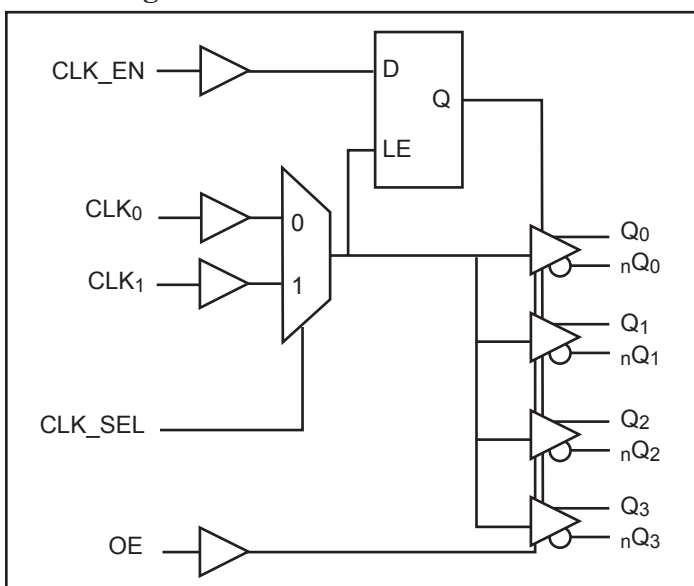
### Features

- Maximum operation frequency: 650 MHz
- 4 pair of differential LVDS outputs
- Selectable CLK<sub>0</sub> and CLK<sub>1</sub> inputs
- CLK<sub>0</sub>, CLK<sub>1</sub> accept LVCMOS, LVTTL input level
- Output Skew: 40ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 2.2ns (maximum)
- 3.3V power supply
- Pin-to-pin compatible to ICS8545
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green):  
- 20-pin TSSOP (L)

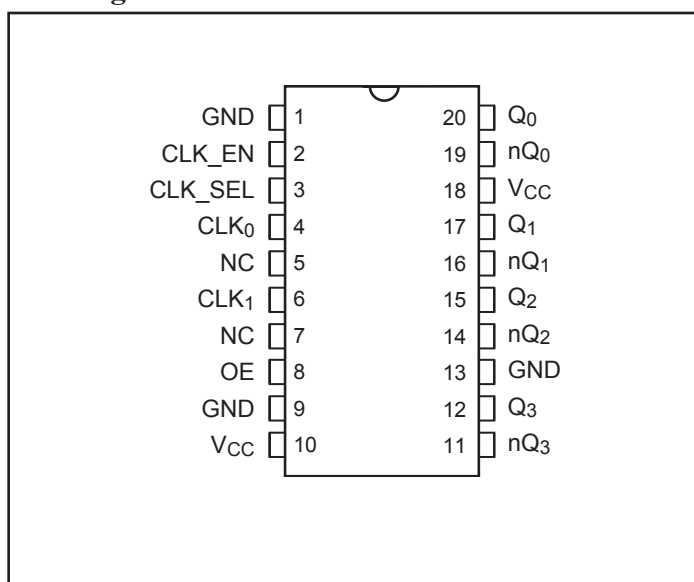
### Description

The PI6C48545 is a high-performance low-skew LVDS fanout buffer. PI6C48545 features two selectable single-ended clock inputs and translate to four LVDS outputs. The CLK<sub>0</sub> and CLK<sub>1</sub> inputs accept LVCMOS or LVTTL signals. The outputs are synchronized with input clock during asynchronous assertion/deassertion of CLK\_EN pin. PI6C48545 is ideal for single-ended LVTTL/LVCMOS to LVDS translations. Typical clock translation and distribution applications are data-communications and telecommunications.

### Block Diagram



### Pin Diagram



### Pin Description

Name	Pin #	Type	Description
GND	1, 9, 13	P	Connect to Ground
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 80kΩ pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK <sub>1</sub> input. When low, selects CLK <sub>0</sub> input. LVCMOS/LVTTL level with 80kΩ pull down.
CLK <sub>0</sub>	4	I_PD	LVCMOS / LVTTL clock input
CLK <sub>1</sub>	6	I_PD	LVCMOS / LVTTL clock input
NC	5, 7		No internal connection.
OE	8	I_PU	Output Enable. Controls outputs Q <sub>0</sub> , nQ <sub>0</sub> through Q <sub>3</sub> , nQ <sub>3</sub> .
V <sub>CC</sub>	10, 18	P	Connect to 3.3V.
Q <sub>3</sub> , nQ <sub>3</sub>	11, 12	O	Differential output pair, LVDS interface level.
Q <sub>2</sub> , nQ <sub>2</sub>	14, 15	O	Differential output pair, LVDS interface level.
Q <sub>1</sub> , nQ <sub>1</sub>	16, 17	O	Differential output pair, LVDS interface level.
Q <sub>0</sub> , nQ <sub>0</sub>	19, 20	O	Differential output pair, LVDS interface level.

#### Notes:

1. I = Input, O = Output, P = Power supply connection, I\_PD = Input with pull down, I\_PU = Input with pull up.

### Pin Characteristics

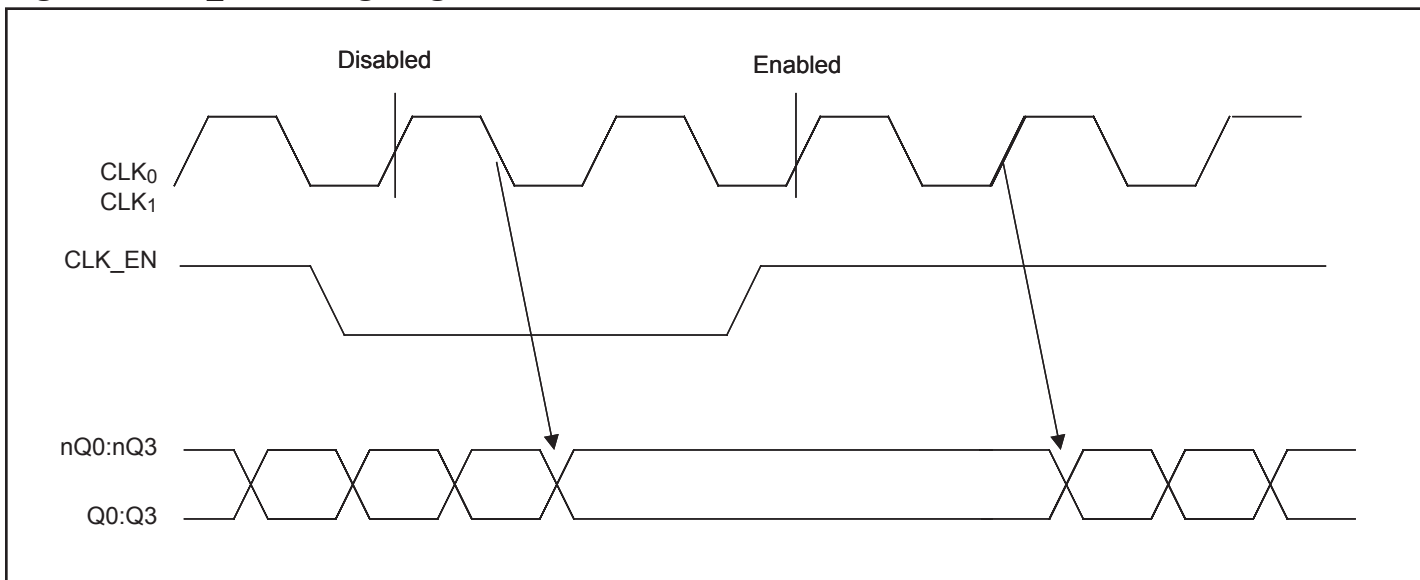
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance			6		pF
R <sub>pullup</sub>	Input Pullup Resistance			80		kΩ
R <sub>pulldown</sub>	Input Pulldown Resistance			80		

### Control Input Function Table

Inputs				Outputs	
OE	CLK_EN	CLK_SEL	Selected Source	Q <sub>0</sub> :Q <sub>3</sub>	nQ <sub>0</sub> :nQ <sub>3</sub>
1	0	0	CLK <sub>0</sub>	Diased: Low	Diased: High
1	0	1	CLK <sub>1</sub>	Diased: Low	Diased: High
1	1	0	CLK <sub>0</sub>	Enabled	Enabled
1	1	1	CLK <sub>1</sub>	Enabled	Enabled
0	x	x		HiZ	HiZ

#### Notes:

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

**Figure 1. CLK\_EN Timing Diagram**

**Clock Input Function Table**

Inputs	Outputs	
CLK <sub>0</sub> or CLK <sub>1</sub>	Q <sub>0</sub> :Q <sub>3</sub>	nQ <sub>0</sub> :nQ <sub>3</sub>
0	LOW	HIGH
1	HIGH	LOW

### Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>CC</sub>	Supply voltage	Referenced to GND			4.6	V
V <sub>IN</sub>	Input voltage	Referenced to GND	-0.5		V <sub>CC</sub> +0.5V	
V <sub>OUT</sub>	Output voltage	Referenced to GND	-0.5		V <sub>CC</sub> +0.5V	
T <sub>STG</sub>	Storage temperature		-65		150	°C

**Notes:**

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>CC</sub>	Power Supply Voltage		3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Temperature		-40		85	°C
I <sub>CC</sub>	Power Supply Current				60	mA

**LVCMOS/LVTTL DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.135\text{V}$  to  $3.465\text{V}$  unless otherwise stated below.)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage	CLK <sub>0</sub> , CLK <sub>1</sub> , CLK_EN, CLK_SE, OE		2		$V_{CC}+0.3$	V
$V_{IL}$	Input Low Voltage	CLK <sub>0</sub> , CLK <sub>1</sub>		-0.3		1.3	V
		CLK_EN, CLK_SEL, OE		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK <sub>0</sub> , CLK <sub>1</sub> , CLK_SEL	$V_{IN} = V_{CC} = 3.465\text{V}$			150	$\mu\text{A}$
		CLK_EN, OE	$V_{IN} = V_{CC} = 3.465\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK <sub>0</sub> , CLK <sub>1</sub> , CLK_SEL	$V_{IN} = 0\text{V}$ , $V_{CC} = 3.465\text{V}$	-5			$\mu\text{A}$
		CLK_EN, OE	$V_{IN} = 0\text{V}$ , $V_{CC} = 3.465\text{V}$	-150			$\mu\text{A}$

**LVDS DC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.135\text{V}$  to  $3.465\text{V}$  unless otherwise stated below.)

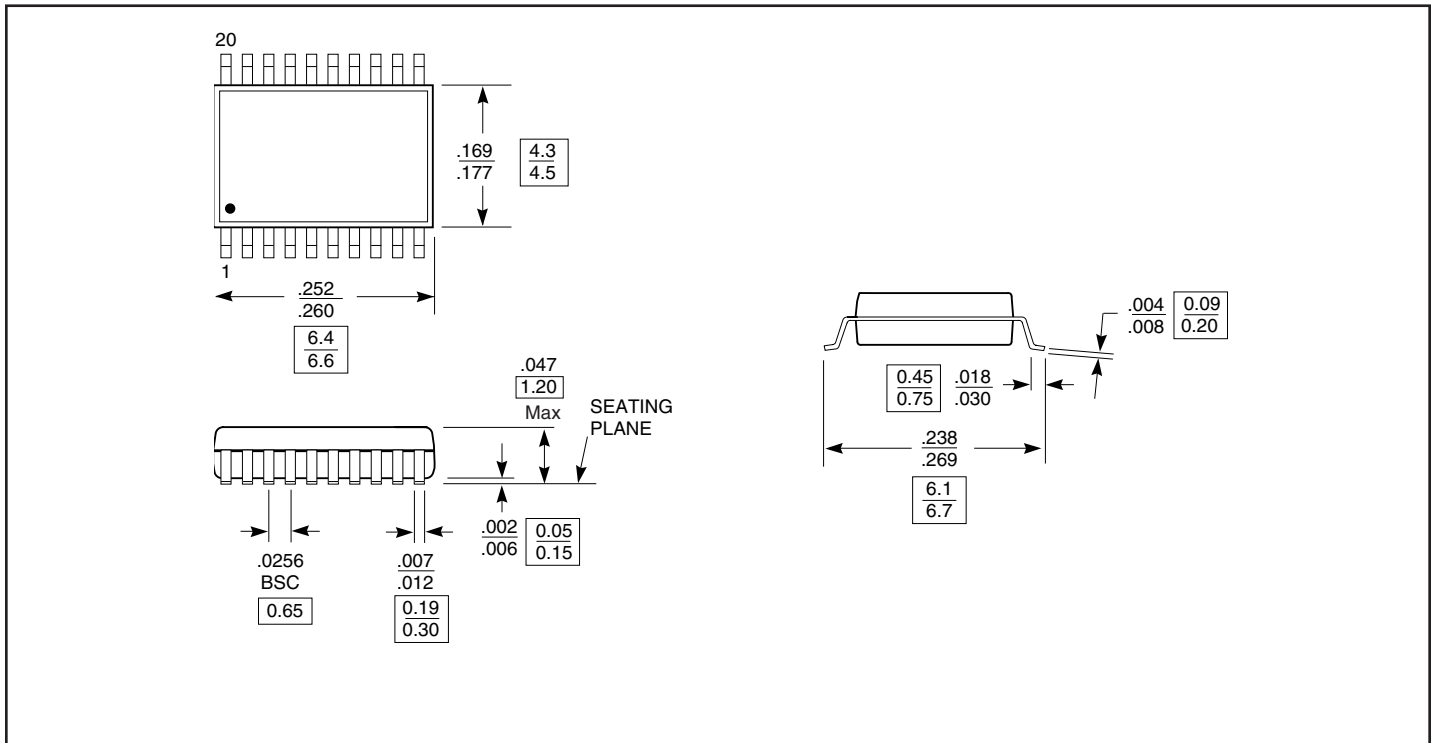
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{OD}$	Differential Output Voltage		200	280	360	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			0	40	
$V_{OS}$	Offset Voltage		1.125	1.3	1.475	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			5	25	mV
$I_{OZ}$	High Impedance Leakage Current		-10		+10	$\mu\text{A}$
$I_{OFF}$	Power OFF Leakage		-20	$\pm 1$	+20	
$I_{OSD}$	Differential Output Short Circuit Current			-3.5	-5	mA
$I_{OS}$	Output Short Circuit Current			-3.5	-5	
$V_{OH}$	Output Voltage High			1.34	1.6	V
$V_{OL}$	Output Voltage Low		0.9	1.06		

**AC Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 3.135\text{V}$  to  $3.465\text{V}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$f_{max}$	Output Frequency				650	MHz
$t_{pd}$	Propagation Delay <sup>(1)</sup>		0.8		2.2	ns
$T_{sk(o)}$	Output-to-output Skew <sup>(2)</sup>				40	ps
$T_{sk(pp)}$	Part-to-part Skew <sup>(3)</sup>				300	
$t_r/t_f$	Output Rise/Fall time	20% - 80%	100		300	
odc	Output duty cycle		48		52	%

**Notes:**

1. Measured from the  $V_{CC}/2$  of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. All parameters are measured at 500MHz unless noted otherwise

**Packaging Mechanical: 20-Pin TSSOP (L)**

**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C48545LE	L	Pb-free & Green 20-pin 173-mil wide TSSOP

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- Number of Transistors = TBD