

# Mobile Multimedia CODEC with 1W Speaker Driver

## **DESCRIPTION**

The WM8983 is a low power, high quality stereo CODEC designed for portable multimedia applications. Highly flexible analogue mixing functions enable new application features, combining hi-fi quality audio with voice communication.

The device integrates preamps for stereo differential mics, and includes drivers for speaker, headphone and differential or stereo line output. External component requirements are reduced as no separate microphone or headphone amplifiers are required.

Advanced on-chip digital signal processing includes a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. A programmable high pass filter in the ADC path is provided for wind noise reduction and an IIR with programmable coefficients can be used as a notch filter to suppress fixed-frequency noise.

The WM8983 digital audio interface can operate in master or slave mode, while an integrated PLL supports flexible clocking schemes. A-law and  $\mu$ -law companding are fully supported.

The WM8983 operates at analogue supply voltages from 2.5V to 3.3V, although the digital core can operate at voltages down to 1.71V to save power. Speaker supplies can operate up to 5V for increased speaker output power. Additional power management control enables individual sections of the chip to be powered down under software control.

## **FEATURES**

#### Stereo CODEC:

- DAC SNR 98dB, THD -84dB ('A' weighted @ 48kHz)
- ADC SNR 95dB, THD -84dB ('A' weighted @ 48kHz)
- Speaker driver (1W into 8Ω BTL with 5V supply)
  - SNR 90dB
  - PSRR 80dB
- Headphone driver with 'capless' option
  - 40mW/channel output power into  $16\Omega$  / 3.3V AVDD2
- Pop and click suppression

#### Mic Preamps:

- Stereo Differential or mono microphone Interfaces
- Programmable preamp gain
- Pseudo differential inputs with common mode rejection
- Programmable ALC / Noise Gate in ADC path
- · Low-noise bias supplied for electret microphones

#### Other Features:

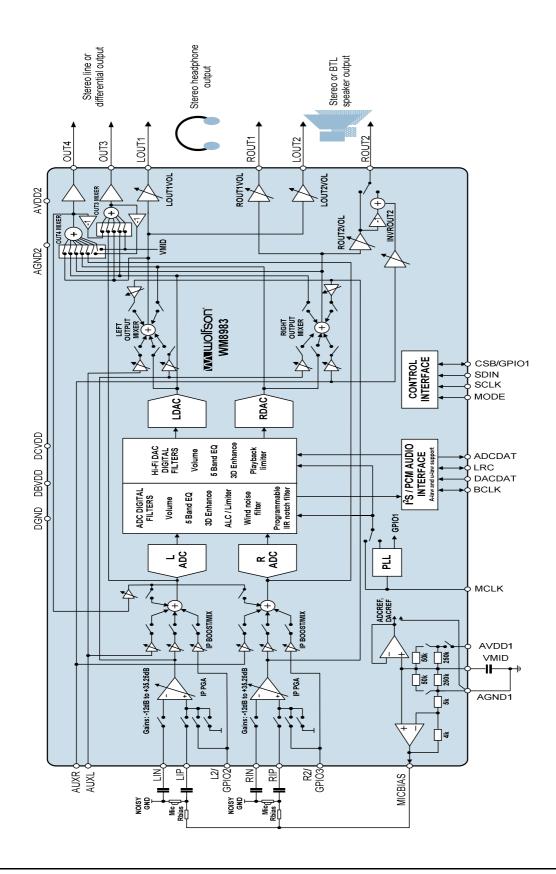
- Enhanced 3-D function for improved stereo separation
- Highly flexible mixing functions
- 5-band equaliser (ADC or DAC path)
- ADC Programmable high pass filter (wind noise reduction)
- ADC Programmable IIR notch filter
- · Aux inputs for stereo analog input signals or 'beep'
- PLL supporting various clocks between 8MHz-50MHz
- Sample rates supported (kHz): 8, 11.025, 16, 12, 16, 22.05, 24, 32, 44.1, 48
- 2.5V to 3.6V analogue supplies
- 1.71V to 3.6V digital supplies
- 2.5V to 5.5V speaker supplies
  - 5x5mm 32-lead QFN package

## **APPLICATIONS**

Multimedia mobile phones

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# **BLOCK DIAGRAM**





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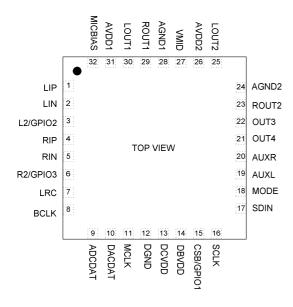
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# **PIN CONFIGURATION**



## **ORDERING INFORMATION**

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8983GEFL/V	-25°C to +85°C	32-lead QFN (5 x 5 mm) (pb-free)	MSL3	260°C
WM8983GEFL/RV	-25°C to +85°C	32-lead QFN (5 x 5 mm) (pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

# **PIN DESCRIPTION**

PIN	NAME	TYPE	DESCRIPTION
1	LIP	Analogue input	Left MIC pre-amp positive input
2	LIN	Analogue input	Left MIC pre-amp negative input
3	L2/GPIO2	Analogue input	Left channel line input/secondary mic pre-amp positive input/GPIO2 pin
4	RIP	Analogue input	Right MIC pre-amp positive input
5	RIN	Analogue input	Right MIC pre-amp negative input
6	R2/GPIO3	Analogue input	Right channel line input/secondary mic pre-amp positive input/GPIO3 pin
7	LRC	Digital Input / Output	DAC and ADC sample rate clock
8	BCLK	Digital Input / Output	Digital audio bit clock
9	ADCDAT	Digital Output	ADC digital audio data output
10	DACDAT	Digital Input	DAC digital audio data input
11	MCLK	Digital Input	Master clock input
12	DGND	Supply	Digital ground
13	DCVDD	Supply	Digital core logic supply
14	DBVDD	Supply	Digital buffer (I/O) supply
15	CSB/GPIO1	Digital Input / Output	3-Wire control interface chip Select / GPIO1 pin
16	SCLK	Digital Input	3-Wire control interface clock input / 2-wire control interface clock input
17	SDIN	Digital Input / Output	3-Wire control interface data input / 2-Wire control interface data input
18	MODE	Digital Input	Control interface selection
19	AUXL	Analogue input	Left auxillary input
20	AUXR	Analogue input	Right auxillary input
21	OUT4	Analogue Output	right line output or mono mix output
22	OUT3	Analogue Output	mono or left line output
23	ROUT2	Analogue Output	Headphone or line output right 2
24	AGND2	Supply	Analogue ground (feeds ROUT2/LOUT2 and OUT3/OUT4)
25	LOUT2	Analogue Output	Headphone or line output left 2
26	AVDD2	Supply	Analogue supply (feeds output amplifiers ROUT2/LOUT2 and OUT3/OUT4)
27	VMID	Reference	Decoupling for ADC and DAC reference voltage
28	AGND1	Supply	Analogue ground (feeds all input amplifiers, PLL, ADC and DAC, internal bias circuits, output amplifiers LOUT1, ROUT1)
29	ROUT1	Analogue Output	Headphone or line output right 1
30	LOUT1	Analogue Output	Headphone or line output left 1
31	AVDD1	Supply	Analogue supply (feeds all input amplifiers, PLL, ADC and DAC, internal bias circuits, output amplifiers LOUT1, LOUT2))
32	MICBIAS	Analogue Output	Microphone bias

## Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB. Refer to the application note WAN\_0118 on "Guidelines on How to Use QFN Packages and Create Associated PCB Footprints"



## **ABSOLUTE MAXIMUM RATINGS**

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD1 supply voltages	-0.3V	+4.5V
AVDD2 supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND1 -0.3V	AVDD1 +0.3V
	AGND2 -0.3V	AVDD2 +0.3V
Storage temperature prior to soldering	30°C max /	85% RH max
Storage temperature after soldering	-65°C	+150°C

#### Notes:

- 1. Analogue and digital grounds must always be within 0.3V of each other.
- 2. All digital and analogue supplies are completely independent from each other.
- 3. Analogue supply voltages should not be less than digital supply voltages.
- 4. In non-boosted mode AVDD2 should be  $\geq$  AVDD1. In boost mode, AVDD2 should be  $\geq$  1.5 x AVDD1.
- 5. DBVDD must be greater than or equal to DCVDD.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71		3.6	V
Digital supply range (Buffer)	DBVDD		1.71 <sup>2</sup>		3.6	V
Analogue supply range	AVDD1		2.5		3.6	V
Speaker supply range	AVDD2		2.5		5.5	V
Ground	DGND, AGND1, AGND2			0		V

## Notes:

- 1. Analogue supply voltages should not be less than digital supply voltages.
- 2. DBVDD should be  $\geq$  1.9V when using the PLL.



WM8983

Production Data

# **ELECTRICAL CHARACTERISTICS**

## **Test Conditions**

 $DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A=+25^{\circ}C, 1 kHz \ signal, fs=48 kHz, 24-bit \ audio \ data \ unless \ otherwise \ stated.$ 

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Input PGA Inputs (LIP,	LIN, RIP, RIN,	L2, R2)				
INPPGAVOLL, INPPGAVOLR, PGAI	BOOSTL and F	PGABOOSTR = 0dB				
Full-scale Input Signal Level – Single-ended input via LIN/RIN <sup>1</sup>				AVDD/3.3		$V_{\text{ms}}$
Full-scale Input Signal Level – Pseudo-differential input <sup>1,2</sup>				AVDD*0.7/ 3.3		$V_{ms}$
Input PGA equivalent input noise		INPPGAVOLL/R = +35.25dB No input signal 22Hz to 20kHz		150		μV
LIN, RIN input resistance		INPPGAVOLL and INPPGAVOLR = +35.25dB		1.7		kΩ
LIN, RIN input resistance		INPPGAVOLL and INPPGAVOLR = 0dB		47		kΩ
LIN, RIN input resistance		INPPGAVOLL and INPPGAVOLR = -12dB		76		kΩ
LIP, RIP input resistance		All gain settings		95		kΩ
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 1 L2_2BOOSTVOL and R2_2BOOSTVOL = 000		90		kΩ
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 0 L2_2BOOSTVOL and		11		kΩ
		R2_2BOOSTVOL = +6dB				
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 0		22		kΩ
		L2_2BOOSTVOL and R2_2BOOSTVOL = 0dB				
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 0		60		kΩ
		L2_2BOOSTVOL and R2_2BOOSTVOL = -12dB				
Input Capacitance		All analogue input pins		10		pF
Input PGA Programmable Gain		Gain adjusted by INPPGAVOLL and INPPGAVOLL	-12		+35.25	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Input PGA Mute Attenuation		INPPGAMUTEL and INPPGAMUTER = 1		100		dB
Input Gain Boost		PGABOOSTL and PGABOOSTR = 0		0		dB
Input Gain Boost		PGABOOSTL and PGABOOSTR = 1		+20		dB



## **Test Conditions**

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V,  $T_A = +25^{\circ}C$ , 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Auxiliary Analogue Inputs (AUXL, A	AUXR)					
Full-scale Input Signal Level <sup>2</sup>				AVDD/3.3		$V_{\text{ms}}$
Input Resistance		Left Input boost and mixer		4.3		kΩ
		enabled, at +6dB				
		Left Input boost and mixer		8.6		kΩ
		enabled, at 0dB gain				
		Left Input boost and mixer		39.1		kΩ
		enabled, at -12dB gain				
		Right Input boost, mixer enabled, at +6dB gain		3		kΩ
		Right Input boost, mixer		6		kΩ
		enabled, at 0dB gain		0		K32
		Right Input boost, mixer		29		kΩ
		enabled, at -12dB gain				
Input Capacitance		All analogue Inputs		10		pF
Gain range from AUXL and AUXR		Gain adjusted by	-12		+6	dB
input to left and right input PGA		AUXL2BOOSTVOL and				-
mixers		AUXR2BOOSTVOL				
AUXLBOOSTVOL and AUXRBOOSTVOL step size				3		dB
L2, R2 Line Input Programmable Ga	ain					
Gain range from L2/R2 input to left		Gain adjusted by	-12		+6	dB
and right input PGA mixers		L2_2BOOSTVOL and				
		R2_2BOOSTVOL				
L2/R2_2BOOSTVOL step size				3		dB
L2/R2_2BOOSTVOL mute				100		dB
attenuation						
OUT4 to left or right input boost red	ord path					
Gain range into left and right input		Gain adjusted by	-6		+12	dB
PGA mixers		OUT4_2ADCVOL				
OUT4_2ADCVOL gain step size				3		dB
OUT4_2ADCVOL mute attenuation				100		dB
Analogue to Digital Converter (ADC	) - Input from	LIN/P and RIN/P in differenti	al config	uration to inp	ut PGA	
INPPGAVOLL, INPPGAVOLR, PGA	BOOSTL, PGA	ABOOSTR, ADCLVOL and AD	CRVOL	= 0dB		
Signal to Noise Ratio <sup>3</sup>	SNR	A-weighted		93		dB
		AVDD1=AVDD2=3.3V				
		A-weighted		91.5		dB
		AVDD1=AVDD2=2.5V		00		~-
Total Harmonic Distortion 4	THD	-12dBV Input		-78		dBFS
Total Harmonic Distortion	'''	AVDD1=AVDD2=3.3V		-70		ט ועט
				7.5		4DE0
		-12dBV Input		-75		dBFS
	<b>+</b>	AVDD1=AVDD2=2.5V				
Total Harmonic Distortion + Noise <sup>5</sup>	THD+N	-12dBV Input		-75		dBFS
		AVDD1=AVDD2=3.3V				
		-12dBV Input		-72		dBFS
		AVDD1=AVDD2=2.5V	<u></u>			
Channel Separation <sup>6</sup>		1kHz full scale input signal		100		dBFS



## **Test Conditions**

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN TYP	MAX UNIT
Analogue to Digital Converter (ADC				2INPPGA = 0.
INPPGAVOLL, INPPGAVOLR, L2_2		2_2BOOSTVOL, ADCLVOL	and ADCRVOL = 0dB	T
Signal to Noise Ratio 3	SNR	A-weighted	95	dB
		AVDD1=AVDD2=3.3V		
		A-weighted	93	dB
		AVDD1=AVDD2=2.5V		
Total Harmonic Distortion <sup>4</sup>	THD	-3dBV Input	-86	dBFS
		AVDD1=AVDD2=3.3V		
		-3dBV Input	-78	dBFS
		AVDD1=AVDD2=2.5V		
Total Harmonic Distortion + Noise 5	THD+N	-3dBV Input	-80	dBFS
		AVDD1=AVDD2=3.3V		
		-3dBV Input	-76	dBFS
		AVDD1=AVDD2=2.5V		
Channel Separation <sup>6</sup>		1kHz input signal	100	dBFS
DAC to left and right mixers into 10	•			
LOUT1VOL, ROUT1VOL, DACLVOI	and DACRVO	DL = 0dB		
Full-scale output 1		LOUT1VOL and	AVDD1/3.3	V <sub>ms</sub>
		ROUTVOL = 0dB		
Signal to Noise Ratio <sup>3</sup>	SNR	A-weighted	100	dB
		AVDD1=AVDD2=3.3V		
		A-weighted	99	dB
		AVDD1=AVDD2=2.5V		
Total Harmonic Distortion 4	THD	0dBFS input	-84	dBFS
		AVDD1=AVDD2=3.3V		
		0dBFS input AVDD1=AVDD2=2.5V	-86	dBFS
Total Harmonic Distortion + Noise <sup>5</sup>	THD+N	0dBFS input AVDD1=AVDD2=3.3V	-83	dBFS
		0dBFS input AVDD1=AVDD2=2.5V	-84	dBFS
Channel Separation <sup>6</sup>		1kHz signal	100	dB
DAC to L/R mixer into 10kΩ / 50pF	load on L/ROU	T2		
LOUT2VOL, ROUT2VOL, DACLVOL	and DACRVO	L = 0dB		
Full-scale output 1			AVDD1/3.3	V <sub>ms</sub>
Signal to Noise Ratio 3	SNR	A-weighted	100	dB
-		AVDD1=AVDD2=3.3V		
		A-weighted	96	dB
		AVDD1=AVDD2=2.5V		
Total Harmonic Distortion <sup>4</sup>	THD	0dBFS input AVDD1=AVDD2=3.3V	-84	dBFS
		0dBFS input AVDD1=AVDD2=2.5V	-82	dBFS
Total Harmonic Distortion + Noise <sup>5</sup>	THD+N	0dBFS input AVDD1=AVDD2=3.3V	-82	dBFS
		0dBFS input AVDD1=AVDD2=2.5V	-80	dBFS
Channel Separation <sup>6</sup>		1kHz input signal	100	dB
DAC to OUT3 and OUT4 mixers to	OUT3/OUT4 or			
Full-scale output voltage	1		AVDD2/3.3	V <sub>ms</sub>
Signal to Noise Ratio <sup>3</sup>	SNR	A-weighted	101.5	dB
• · · · · · · · · · · · · · · · · · · ·		AVDD1=AVDD2=3.3V		
		, (VDD1 /(VDD2-0.0V	<u> </u>	1



## **Test Conditions**

 $DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A=+25^{\circ}C, 1 kHz \ signal, fs=48 kHz, 24-bit \ audio \ data \ unless \ otherwise \ stated.$ 

The file scale signal   AVDD14/OD2e3 3V   AVD	PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total Harmonic Distortion + Noise 3   THD+N   full-scale signal   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=3.5V   AVDD1=AVDD2=2.5V   AVDD1=AVDD2=3.5V   AV	Total Harmonic Distortion 4	THD	full-scale signal		-80		dBFS
AVDDI=AVDD2=2.5V   AVDDI=AVDD2			AVDD1=AVDD2=3.3V				
Total Harmonic Distortion + Noise   ThD+N   ADDI=AVDD2=3.3V   ADDI=AVDD2=3.3V   ADDI=AVDD2=3.3V   ADDI=AVDD2=3.3V   ADDI=AVDD2=3.3V   ADDI=AVDD2=2.5V   ADDI=AVDD2=2.5V   ADDI=AVDD2=2.5V   ADDI=AVDD2=2.5V   ADDI=AVDD2=2.5V   ADDI=AVDD2=3.3V   ADDI=AVDD2=3.3V   ADDI=AVDD2=3.5V   A			full-scale signal		-87		dBFS
AVDD1=AVDD2=3.3V   full-scale signal   -85   dBFS   AVDD1=AVDD2=2.5V   -85   dBFS   AVDD1=AVDD2=3.3V   -85   dBFS   AVDD1=AVDD2=3.3V   -85   dBFS   AVDD1=AVDD2=3.3V   -85   dBFS   -85   d			AVDD1=AVDD2=2.5V				
Authorization   Authorizati	Total Harmonic Distortion + Noise 5	THD+N	full-scale signal		-77		dBFS
AVDD1=AVDD2=2.5V			AVDD1=AVDD2=3.3V				
Channel Separation <sup>6</sup> 1kHz signal         100         dBFS           DAC to left and right mixer into headphone (16Ω load) on LOUT2 and ROUT2 LOUT2VOL, DACLVOL and DACRVOL = 0dB           Full-scale output         AVDD1/3.3         Vms.           Signal to Noise Ratio <sup>3</sup> SNR         A-weighted         98         dB           ADD1=AVDD2=3.3V         98         dB         dBFS           Total Harmonic Distortion <sup>4</sup> THD         P <sub>2</sub> = 29mW, RL=16Q         -76         dBFS           Total Harmonic Distortion + Noise <sup>5</sup> THD+N         Po = 20mW, RL=16Q         -76         dBFS           Channel Separation <sup>6</sup> 1kHz signal         100         dB           Bypass paths to left and right output mixers. BYPLZLMIX = 1 and BYPRZRMIX = 1         THD         PO = 20mW, RL=16Q         -72         dBFS           Channel Separation <sup>6</sup> Bipyass paths to left and right output mixers. BYPLZLMIX = 1 and BYPRZRMIX = 1         THD         THD+N         PO = 20mW, RL=16Q         -72         dBFS           Channel Separation mixer         Gain adjusted by BYPLZLMIX = 1 and BYPRZMIX = 1         -15         0         +6         dB           BYPLMIXVOL and BYPRMIXVOL gain step into mixer         BYPLZLMIX = 0         100         dB         dB           Mule attenuation			full-scale signal		-85		dBFS
DAC to left and right mixer into headphone (16Ω load) on LOUT2 and ROUT2			AVDD1=AVDD2=2.5V				
Full-scale output   A-weighted   AVDD1/3.3   V-me	Channel Separation <sup>6</sup>		1kHz signal		100		dBFS
Full-scale output							
Signal to Noise Ratio   Sig		and DACRVO	L = 0dB	1	1		T.
AVDD1=AVDD2=3.3V	•				AVDD1/3.3		V <sub>ms</sub>
Total Harmonic Distortion   THD   Po = 20mW, RL = 16Ω   -76   dBFS	Signal to Noise Ratio <sup>3</sup>	SNR	A-weighted		98		dB
Total Harmonic Distortion + Noise   ThD+N   Po = 20mW, RL=16Ω   -72   dBFS			AVDD1=AVDD2=3.3V				
Channel Separation	Total Harmonic Distortion <sup>4</sup>	THD	$P_o = 20$ mW, RL=16 $\Omega$		-76		dBFS
Channel Separation	Total Harmonic Distortion + Noise 5	THD+N	Po = 20mW RI =160		-72		dBES
Pypass paths to left and right output mixers. BYPL2LMIX = 1 and BYPR2RMIX = 1	Total Harmonic Bistortion - Noise	1115.11	10 2011111, 112 1032		, 2		ubi o
Pypass paths to left and right output mixers. BYPL2LMIX = 1 and BYPR2RMIX = 1	Observation 6		ALLIE elevat		400		.ID
PGA gain range into mixer			•	<u> </u>	100		aB
BYPLMIX/OL and BYPRMIXVOL and BYPRZMIX = 0		It mixers. BYF					I
gain step into mixer         BYPL2LMIX = 0 BYPR2RMIX = 0         100         dB           Analogue outputs (LOUT1, ROUT1, LOUT2, ROUT2)         BYPR2RMIX = 0         100         dB           Programmable Gain range         Gain adjusted by L/ROUT1VOL and L/ROUT2VOL         -57         0         +6         dB           Programmable Gain step size         Guaranteed         1         dB           Mute attenuation         1kHz, full scale signal L/ROUT1MUTE = 1 L/ROUT2MUTE = 1         85         dB           LIN and RIN input PGA to input boost stage into 10kΩ / 50pF load on OUT3/OUT4 outputs INPPGAVOLR, PGABOOSTL and PGABOOSTR = 0dB         AVDD2/3.3         V <sub>ms</sub> Full-scale output voltage, 0dB gain         A-weighted AVDD1=AVDD2=3.3V         90         98         dB           Signal to Noise Ratio 3         SNR A-weighted AVDD1=AVDD2=2.5V         96         dB         dB           AVDD1=AVDD2=3.3V         22Hz to 22kHz AVDD1=AVDD2=3.3V         93.5         dBFS           AVDD1=AVDD2=2.5V         4VDD1=AVDD2=2.5V         93.5         dBFS           Total Harmonic Distortion 4         THD full-scale signal AVDD1=AVDD2=3.3V         -82         dBFS           Total Harmonic Distortion + Noise 5         THD+N full-scale signal AVDD1=AVDD2=3.3V         -82         dBFS	PGA gain range into mixer		BYPLMIXVOL and	-15	0	+6	αВ
Mute attenuation					3		dB
Programmable Gain range					100		dB
Programmable Gain range	Analogue outputs (LOUT1, ROUT1,	LOUT2, ROUT	(2)	1			l
Programmable Gain step size			Gain adjusted by L/ROUT1VOL and	-57	0	+6	dB
Mute attenuation         1kHz, full scale signal L/ROUT1MUTE = 1 L/ROUT2MUTE = 1 L/ROUT2MUTE = 1         85         dB           LIN and RIN input PGA to input boost stage into 10kΩ / 50pF load on OUT3/OUT4 outputs INPPGAVOLL, INPPGAVOLR, PGABOOSTL and PGABOOSTR = 0dB         AVDD2/3.3         Vms           Full-scale output voltage, 0dB gain         SNR         A-weighted AVDD1=AVDD2=3.3V         90         98         dB           Signal to Noise Ratio 3         SNR         A-weighted AVDD1=AVDD2=3.3V         96         dB           A-weighted AVDD1=AVDD2=3.3V         96         dB         dB           AVDD1=AVDD2=2.5V         95.5         dBFS           AVDD1=AVDD2=3.3V         95.5         dBFS           AVDD1=AVDD2=3.3V         93.5         dBFS           Total Harmonic Distortion 4         THD         full-scale signal AVDD1=AVDD2=3.3V         -84         dBFS           Total Harmonic Distortion + Noise 5         THD+N         full-scale signal AVDD1=AVDD2=3.3V         -82         dBFS	Programmable Cain etch size				1		dD
L/ROUT1MUTE = 1	<u> </u>				+		
LIN and RIN input PGA to input boost stage into 10kΩ / 50pF load on OUT3/OUT4 outputs	mule alternation		L/ROUT1MUTE = 1		00		αв
Full-scale output voltage, 0dB gain	LIN and RIN input PGA to input boo	st stage into		UT4 outr	outs		
Signal to Noise Ratio 3   SNR		-	•				
Signal to Noise Ratio 3   SNR	Full-scale output voltage, 0dB gain				AVDD2/3.3		V <sub>ms</sub>
AVDD1=AVDD2=3.3V  A-weighted AVDD1=AVDD2=2.5V  22Hz to 22kHz AVDD1=AVDD2=3.3V  22Hz to 22kHz AVDD1=AVDD2=3.3V  22Hz to 22kHz AVDD1=AVDD2=3.3V  10HI-scale signal AVDD1=AVDD2=3.3V  full-scale signal AVDD1=AVDD2=3.3V  Total Harmonic Distortion + Noise 5  THD+N  full-scale signal AVDD1=AVDD2=2.5V  Total Harmonic Distortion + Noise 5  THD+N  full-scale signal AVDD1=AVDD2=3.3V  full-scale signal AVDD1=AVDD2=3.3V  AVDD1=AVDD2=3.3V		SNR	A-weighted	90			
A-weighted   96   dB	-		_				
AVDD1=AVDD2=2.5V  22Hz to 22kHz AVDD1=AVDD2=3.3V  22Hz to 22kHz AVDD1=AVDD2=3.3V  22Hz to 22kHz AVDD1=AVDD2=2.5V  Total Harmonic Distortion   THD  full-scale signal AVDD1=AVDD2=3.3V  full-scale signal AVDD1=AVDD2=2.5V  Total Harmonic Distortion + Noise  THD+N  full-scale signal AVDD1=AVDD2=3.3V  full-scale signal AVDD1=AVDD2=3.3V  full-scale signal AVDD1=AVDD2=3.3V  AVDD1=AVDD2=3.3V					96		dB
22Hz to 22kHz			_				
AVDD1=AVDD2=3.3V   22Hz to 22kHz   93.5   dBFS					95.5		dBFS
22Hz to 22kHz							
AVDD1=AVDD2=2.5V					93.5		dBFS
Total Harmonic Distortion 4         THD         full-scale signal AVDD1=AVDD2=3.3V         -84         dBFS           In the full-scale signal AVDD1=AVDD2=2.5V         -82         dBFS           In the full-scale signal AVDD1=AVDD2=2.5V         -82         dBFS           In the full-scale signal AVDD1=AVDD2=3.3V         -82         dBFS							
AVDD1=AVDD2=3.3V  full-scale signal	Total Harmonic Distortion <sup>4</sup>	THD			-84		dBFS
full-scale signal AVDD1=AVDD2=2.5V  Total Harmonic Distortion + Noise 5 THD+N full-scale signal AVDD1=AVDD2=3.3V  dBFS dBFS			_				
AVDD1=AVDD2=2.5V  Total Harmonic Distortion + Noise <sup>5</sup> THD+N full-scale signal AVDD1=AVDD2=3.3V  dBFS AVDD1=AVDD2=3.3V					-82		dBFS
Total Harmonic Distortion + Noise <sup>5</sup> THD+N full-scale signal AVDD1=AVDD2=3.3V -82 dBFS			_				
AVDD1=AVDD2=3.3V	Total Harmonic Distortion + Noise <sup>5</sup>	THD+N			-82		dBFS
			_				
I I I I I I I I I I I I I I I I I I I			full-scale signal		-80		dBFS



## **Test Conditions**

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		AVDD1=AVDD2=2.5V				
Channel Separation <sup>6</sup>				100		dB
LIN and RIN into input PGA Bypass			oads			
BYPLMIXVOL, BYPRMIXVOL, LOU	T1VOL and RO	UT1VOL = 0dB				1
Full-scale output voltage, 0dB gain				AVDD1/3.3		V <sub>ms</sub>
SIGNAL TO NOISE RATIO 3	SNR	A-weighted	90	100		dB
		AVDD1=AVDD2=3.3V				
		A-weighted		96		dB
		AVDD1=AVDD2=2.5V				
		22Hz to 22kHz		95.5		dB
		AVDD1=AVDD2=3.3V				
		22Hz to 22kHz		93.5		dB
4		AVDD1=AVDD2=2.5V				
Total Harmonic Distortion <sup>4</sup>	THD	full-scale signal		-87	-75	dBFS
		AVDD1=AVDD2=3.3V				
		full-scale signal		-69		dBFS
		AVDD1=AVDD2=2.5V				
Total Harmonic Distortion + Noise <sup>5</sup>	THD+N	full-scale signal		-85	-73	dBFS
		AVDD1=AVDD2=3.3V				
		full-scale signal		-68		dBFS
Cl		AVDD1=AVDD2=2.5V		100		I.D.
Channel separation <sup>6</sup>		1kHz full scale signal		100		dB
Sneaker Outnut /I OUT2 ROUT2 w	ith 80 hridge t	ied load INVROLIT2=1)				
Speaker Output (LOUT2, ROUT2 w	ith 8Ω bridge t			AVDD2/		Vrms
<b>Speaker Output (LOUT2, ROUT2 w</b> Full scale output voltage, 0dB gain. <sup>7</sup>	ith 8Ω bridge t	sed load, INVROUT2=1) SPKBOOST=0		AVDD2/		Vrms
	ith 8Ω bridge t	SPKBOOST=0		3.3		Vrms
	ith 8Ω bridge t			3.3 (AVDD2/		Vrms
Full scale output voltage, 0dB gain. <sup>7</sup>	_	SPKBOOST=0 SPKBOOST=1	ry closely	3.3 (AVDD2/ 3.3)*1.5	THD; see b	
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	SPKBOOST=0  SPKBOOST=1  Output power is ve	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with	ΓHD; see bo	elow
	_	SPKBOOST=0 SPKBOOST=1	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04	THD; see b	elow %
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	SPKBOOST=0  SPKBOOST=1  Output power is ve $P_{O}$ =200mW, $R_{L}$ = $8\Omega$ ,  AVDD2=3.3V	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with	ΓHD; see b	elow
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	SPKBOOST=0  SPKBOOST=1  Output power is ve $P_0 = 200$ mW, $R_L = 8\Omega$ ,	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68	THD; see be	elow % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	SPKBOOST=0  SPKBOOST=1  Output power is ve $P_0$ =200mW, $R_L$ = $8\Omega$ ,  AVDD2=3.3V $P_0$ =320mW, $R_L$ = $8\Omega$ ,  AVDD2=3.3V	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0	THD; see bo	elow % dB %
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	SPKBOOST=0  SPKBOOST=1  Output power is ve $P_0$ =200mW, $R_L$ = $8\Omega$ ,  AVDD2=3.3V $P_0$ =320mW, $R_L$ = $8\Omega$ ,	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40	ΓHD; see b	elow % dB % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74	ΓHD; see b	elow % dB % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve \\ P_O = 200mW, R_L = 8\Omega, \\ AVDD2=3.3V \\ P_O = 320mW, R_L = 8\Omega, \\ AVDD2=3.3V \\ P_O = 500mW, R_L = 8\Omega, \\ $	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02	ΓHD; see b	elow  % dB % dB % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power	P <sub>0</sub>	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega,$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0	ΓHD; see b	elow  % dB % dB % dB % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion	Po THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, \\ AVDD2=5V$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40	THD; see bi	elow  % dB % dB % dB % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion	Po THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $AVDD2=5V$ $AVDD2=3.3V,$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40	ΓHD; see b	elow  % dB % dB % dB % dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion	Po THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $AVDD2=3.3V, \\ R_{L} = 8\Omega$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90	ΓHD; see b	elow  dB  % dB  % dB  % dB  dB  dB  dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion  Signal to Noise Ratio	Po THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $AVDD2=3.3V, \\ R_{L} = 8\Omega$ $AVDD2=5V,$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90	ΓHD; see b	elow  dB  % dB  % dB  % dB  dB  dB  dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion  Signal to Noise Ratio	P <sub>0</sub> THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, AVDD2=5V$ $AVDD2=5V$ $AVDD2=3.3V, R_{L} = 8\Omega$ $AVDD2=5V, R_{L} = 8\Omega$ $R_{L} = 8\Omega BTL$ $R_{L} = 8\Omega BTL$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90	ΓHD; see b	elow  % dB % dB % dB dB dB dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion  Signal to Noise Ratio  Power Supply Rejection Ratio (50Hz-22kHz)	P <sub>0</sub> THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, \\ AVDD2=3.3V$ $P_{O} = 500mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, \\ AVDD2=5V$ $AVDD2=5V$ $AVDD2=5V$ $AVDD2=5V, \\ R_{L} = 8\Omega, \\ R_{L} =$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90 90	ΓHD; see b	elow  % dB % dB % dB dB dB dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion  Signal to Noise Ratio  Power Supply Rejection Ratio (50Hz-22kHz)  Microphone Bias	P <sub>0</sub> THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{0} = 200mW, R_{L} = 8\Omega, AVDD2=3.3V$ $P_{0} = 320mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{0} = 500mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{0} = 860mW, R_{L} = 8\Omega, AVDD2=5V$ $AVDD2=3.3V, R_{L} = 8\Omega$ $AVDD2=5V, R_{L} = 8\Omega$ $AVDD2=5V, R_{L} = 8\Omega$ $R_{L} = 8\Omega BTL$ $R_{L} = 8\Omega BTL$ $R_{L} = 8\Omega BTL AVDD2=5V$ $(boost)$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90 90 80 69	ΓHD; see b	elow  dB  % dB  % dB  % dB  dB  dB  dB  dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion  Signal to Noise Ratio  Power Supply Rejection Ratio (50Hz-22kHz)	P <sub>0</sub> THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{O} = 200mW, R_{L} = 8\Omega, AVDD2=3.3V$ $P_{O} = 320mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{O} = 500mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{O} = 860mW, R_{L} = 8\Omega, AVDD2=5V$ $AVDD2=3.3V, R_{L} = 8\Omega$ $AVDD2=5V, R_{L} = 8\Omega$ $R_{L} = 8\Omega$ $R_{L} = 8\Omega$ $R_{L} = 8\Omega$ $R_{L} = 8\Omega$ BTL $R_{L} = 8\Omega$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90 90 80 69	THD; see b	elow  % dB % dB % dB dB dB dB dB
Full scale output voltage, 0dB gain. <sup>7</sup> Output Power  Total Harmonic Distortion  Signal to Noise Ratio  Power Supply Rejection Ratio (50Hz-22kHz)  Microphone Bias	P <sub>0</sub> THD	$SPKBOOST=0$ $SPKBOOST=1$ $Output power is ve$ $P_{0} = 200mW, R_{L} = 8\Omega, AVDD2=3.3V$ $P_{0} = 320mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{0} = 500mW, R_{L} = 8\Omega, AVDD2=5V$ $P_{0} = 860mW, R_{L} = 8\Omega, AVDD2=5V$ $AVDD2=3.3V, R_{L} = 8\Omega$ $AVDD2=5V, R_{L} = 8\Omega$ $AVDD2=5V, R_{L} = 8\Omega$ $R_{L} = 8\Omega BTL$ $R_{L} = 8\Omega BTL$ $R_{L} = 8\Omega BTL AVDD2=5V$ $(boost)$	ry closely	3.3 (AVDD2/ 3.3)*1.5 correlated with 0.04 -68 1.0 -40 0.02 -74 1.0 -40 90 90 80 69	ΓHD; see b	elow  dB  % dB  % dB  % dB  dB  dB  dB  dB



#### **Test Conditions**

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T<sub>A</sub> = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output						
Input HIGH Level	V <sub>IH</sub>		0.7×DBV DD			V
Input LOW Level	$V_{IL}$				0.3×DBVDD	V
Output HIGH Level	V <sub>OH</sub>	I <sub>OL</sub> =1mA	0.9×DBV DD			V
Output LOW Level	$V_{OL}$	I <sub>OH</sub> =1mA			0.1xDBVDD	V
Input Capacitance		All digital pins		10		pF

## **TERMINOLOGY**

- Full-scale input and output levels scale in relation to AVDD or AVDD2 depending upon the input or output used. For example, when AVDD = 3.3V, 0dBFS = 1V<sub>rms</sub> (0dBV). When AVDD < 3.3V the absolute level of 0dBFS will decrease with a linear relationship to AVDD.
- 2. Input level to RIP and LIP in differential configurations is limited to a maximum of -3dB or performance will be reduced.
- 3. Signal-to-noise ratio (dBFS) SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
- 4. Total Harmonic Distortion (dBFS) THD is the difference in level between a reference full scale output signal and the first seven odd harmonics of the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven harmonics is calculated.
- 5. Total Harmonic Distortion plus Noise (dBFS) THD+N is the difference in level between a reference full scale output signal and the sum of the harmonics, wide-band noise and interference on the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the total harmonics, wide-band noise and interference is calculated.
- 6. Channel Separation (dB) Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- 7. The maximum output voltage can be limited by the speaker power supply. If SPKBOOST is set then AVDD2 should be 1.5xAVDD to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).



## SPEAKER OUTPUT THD VERSUS POWER

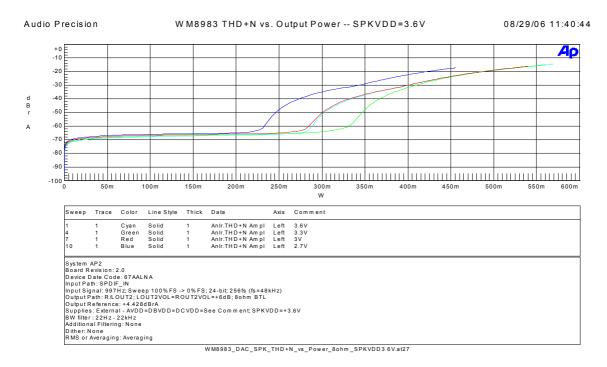


Figure 1 Speaker THD+N vs Output Power (Boost Disabled: SPKVDD=3.6V; SPKBOOST=0; AVDD Range =3.6-2.7V)



Figure 2 Speaker THD+N vs Output Power (Boost Disabled: SPKVDD=4.2V; SPKBOOST=0; AVDD Range =3.6-2.7V)



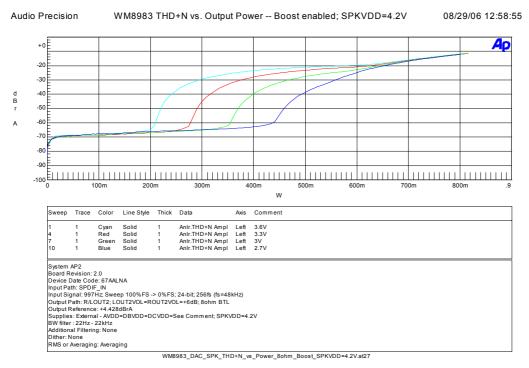


Figure 3 Speaker THD+N vs Output Power (Boost Mode: SPKVDD=4.2V; SPKBOOST=1; AVDD Range =3.6-2.7V)

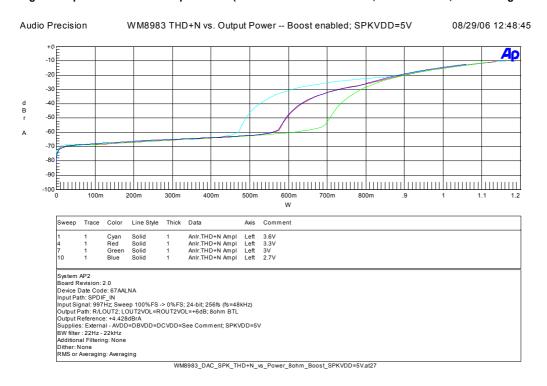


Figure 4 Speaker THD+N vs Output Power (Boost Mode: SPKVDD=5V; SPKBOOST=1; AVDD Range =3.6-2.7V)

# **POWER CONSUMPTION**

## **TYPICAL SCENARIOS**

Estimated current consumption for typical scenarios are shown below.

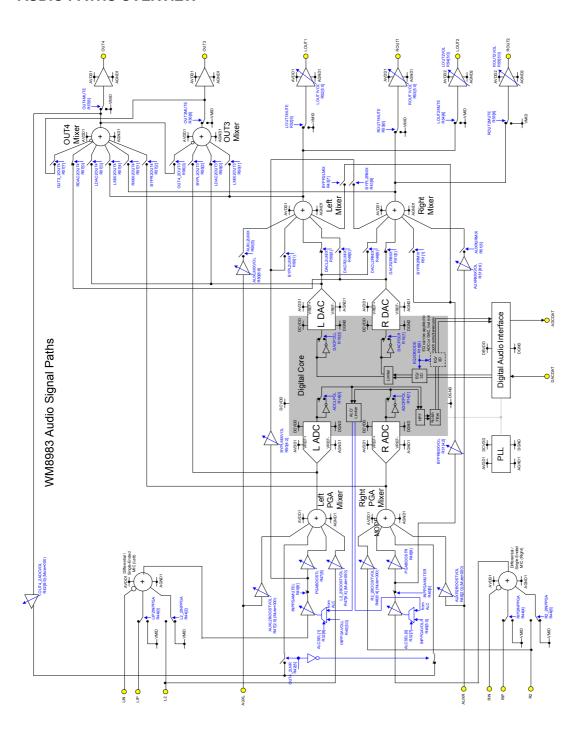
Power delivered to the load is not included.

MODE	I <sub>AVDD1</sub> mA (3.3V)	I <sub>AVDD2</sub> mA (3.3V)	I <sub>DCVDD</sub> mA (1.8V)	I <sub>DBVDD</sub> mA (1.8V)	TOTAL mW
Off (No clocks, temperature sensor disabled)	0.010	0.010	0.001	0.002	0.071
Sleep (VREF maintained)	0.100	0.001	0.012	0.003	0.360
Mono Record from Differential MIC (8kHz, PLL enabled)	4.000	0.001	0.400	0.030	13.97
Stereo HP Playback (44.1kHz, PLL enabled)	3.700	0.950	2.100	0.100	19.31

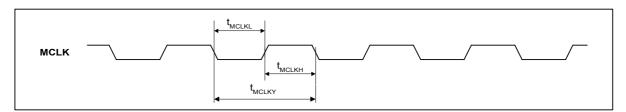
**Table 1 Power Consumption** 



# **AUDIO PATHS OVERVIEW**



# SIGNAL TIMING REQUIREMENTS SYSTEM CLOCK TIMING



**Figure 5 System Clock Timing Requirements** 

#### **Test Conditions**

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V, T<sub>A</sub> = +25°C, Slave Mode

PARAMETER	SYMBOL	MBOL CONDITIONS		TYP	MAX	UNIT
System Clock Timing Information						
MCLK avalatima	T <sub>MCLKY</sub>	MCLK=SYSCLK (=256fs)	81.38			ns
MCLK cycle time		MCLK input to PLL Note 1	20			ns
MCLK duty cycle	T <sub>MCLKDS</sub>		60:40		40:60	

#### Note:

## **AUDIO INTERFACE TIMING - MASTER MODE**

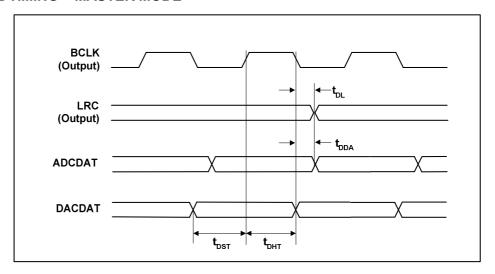


Figure 6 Digital Audio Data Timing – Master Mode (see Control Interface)

<sup>1.</sup> PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

## **Test Conditions**

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V,  $T_A$ =+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC propagation delay from BCLK falling edge	t <sub>DL</sub>			10	ns
ADCDAT propagation delay from BCLK falling edge	t <sub>DDA</sub>			25	ns
DACDAT setup time to BCLK rising edge	t <sub>DST</sub>	10			ns
DACDAT hold time from BCLK rising edge	t <sub>DHT</sub>	10			ns

## **AUDIO INTERFACE TIMING – SLAVE MODE**

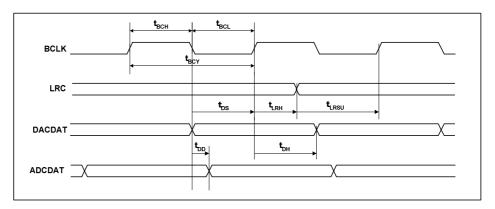


Figure 7 Digital Audio Data Timing - Slave Mode

## **Test Conditions**

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V,  $T_A$ =+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t <sub>BCY</sub>	50			ns
BCLK pulse width high	t <sub>BCH</sub>	20			ns
BCLK pulse width low	t <sub>BCL</sub>	20			ns
LRC set-up time to BCLK rising edge	t <sub>LRSU</sub>	10			ns
LRC hold time from BCLK rising edge	t <sub>LRH</sub>	10			ns
DACDAT hold time from BCLK rising edge	t <sub>DH</sub>	10			ns
DACDAT set-up time to BCLK rising edge	t <sub>DS</sub>	10			ns
ADCDAT propagation delay from BCLK falling edge	t <sub>DD</sub>			25	ns

#### Note:

BCLK period should always be greater than or equal to MCLK period.

## **CONTROL INTERFACE TIMING – 3-WIRE MODE**

3-wire mode is selected by connecting the MODE pin high.

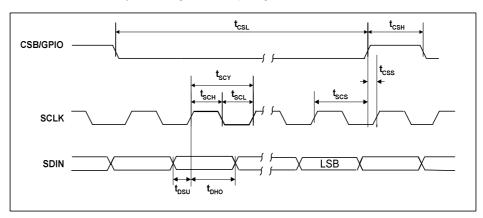


Figure 8 Control Interface Timing - 3-Wire Serial Control Mode

## **Test Conditions**

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V,  $T_A$ =+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT				
Program Register Input Information									
SCLK rising edge to CSB rising edge	t <sub>scs</sub>	80			ns				
SCLK pulse cycle time	tscy	200			ns				
SCLK pulse width low	t <sub>scl</sub>	80			ns				
SCLK pulse width high	t <sub>scн</sub>	80			ns				
SDIN to SCLK set-up time	t <sub>DSU</sub>	40			ns				
SCLK to SDIN hold time	$t_{DHO}$	40			ns				
CSB pulse width low	t <sub>CSL</sub>	40			ns				
CSB pulse width high	t <sub>сsн</sub>	40			ns				
CSB rising to SCLK rising	t <sub>css</sub>	40			ns				
Pulse width of spikes that will be suppressed	t <sub>ps</sub>	0		5	ns				



## **CONTROL INTERFACE TIMING - 2-WIRE MODE**

2-wire mode is selected by connecting the MODE pin low.

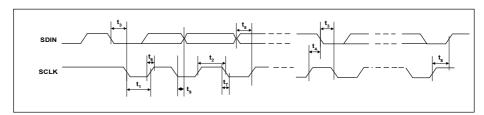


Figure 9 Control Interface Timing – 2-Wire Serial Control Mode

## **Test Conditions**

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V,  $T_A$ =+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT			
Program Register Input Information								
SCLK Frequency		0		526	kHz			
SCLK Low Pulse-Width	t <sub>1</sub>	1.3			us			
SCLK High Pulse-Width	t <sub>2</sub>	600			ns			
Hold Time (Start Condition)	t <sub>3</sub>	600			ns			
Setup Time (Start Condition)	t <sub>4</sub>	600			ns			
Data Setup Time	t <sub>5</sub>	100			ns			
SDIN, SCLK Rise Time	t <sub>6</sub>			300	ns			
SDIN, SCLK Fall Time	t <sub>7</sub>			300	ns			
Setup Time (Stop Condition)	t <sub>8</sub>	600			ns			
Data Hold Time	t <sub>9</sub>			900	ns			
Pulse width of spikes that will be suppressed	t <sub>ps</sub>	0		5	ns			



## INTERNAL POWER ON RESET CIRCUIT

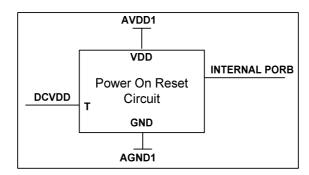


Figure 10 Internal Power on Reset Circuit Schematic

The WM8983 includes an internal Power-On-Reset Circuit, as shown in Figure 10, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD1 and monitors DCVDD. It asserts PORB low if AVDD1 or DCVDD is below a minimum threshold.

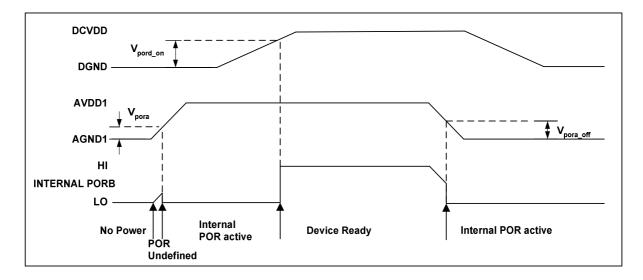


Figure 11 Typical Power up Sequence where AVDD1 is Powered before DCVDD

Figure 11 shows a typical power-up sequence where AVDD1 comes up first. When AVDD1 goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD1 is at full supply level. Next DCVDD rises to  $V_{pord\_on}$  and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD1 falls first, PORB is asserted low whenever AVDD1 drops below the minimum threshold  $V_{\text{pora.off}}$ .



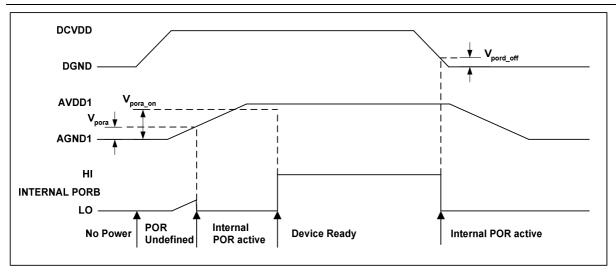


Figure 12 Typical Power up Sequence where DCVDD is Powered before AVDD1

Figure 12 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD1 goes above the minimum threshold,  $V_{pora}$ , there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD1 rises to  $V_{pora\_on}$ , PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold  $V_{pord\_off}$ .

SYMBOL	MIN	TYP	MAX	UNIT
$V_{pora}$	0.4	0.6	8.0	V
V <sub>pora_on</sub>	0.9	1.2	1.6	V
$V_{pora\_off}$	0.4	0.6	8.0	V
$V_{pord\_on}$	0.5	0.7	0.9	V
$V_{pord\ off}$	0.4	0.6	0.8	V

Table 2 Typical POR Operation (Typical Simulated Values)

#### Notes:

- If AVDD1 and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V<sub>pora\_off</sub> or V<sub>pord\_off</sub>) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
- 2. The chip will enter reset at power down when AVDD1 or DCVDD falls below  $V_{pora\_off}$  or  $V_{pord\_off}$ . This may be important if the supply is turned on and off frequently by a power management system.
- 3. The minimum  $t_{\text{por}}$  period is maintained even if DCVDD and AVDD1 have zero rise time. This specification is guaranteed by design rather than test.

## RECOMMENDED POWER UP/DOWN SEQUENCE

In order to minimise output pop and click noise, it is recommended that the WM8983 device is powered up and down under control using the following sequences:

#### Power Up

- Turn on external power supplies. Wait for supply voltage to settle.
- Set low bias mode, BIASCUT = 1.
- Mute all Outputs and set PGAs to minimum gain, R52 to R57 = 0x140h.
- Enable VMID independent current bias, POBCTRL = 1, DELEN = 1.
- Enable required outputs, DACs and mixers.
- Enable analogue bias, BIASEN, and VMID with required charge time e.g. VMIDSEL=01 = 100kΩ.
- Setup digital interface, input amplifiers, PLL, ADCs and DACs for desired operation.
- Unmute L/ROUT1 and set desired volume, e.g. for 0dB R52 and R53 = 0x139h.
- Unmute L/ROUT2 and set desired volume, e.g. for 0dB R54 and R55 = 0x139h.
- Disable VMID independent current bias, POBCTRL = 0, DELEN = 0.

#### Power Down:

- Disable Thermal shutdown
- Disable VMIDSEL=00 and BIASEN=0
- Wait for VMID to discharge
- Power off registers R1, R2, R3 = 0x000h
- · Remove external power supplies

## Note:

Charging time constant is determined by impedance selected by VMIDSEL and the value of decoupling capacitor connected to VMID pin.



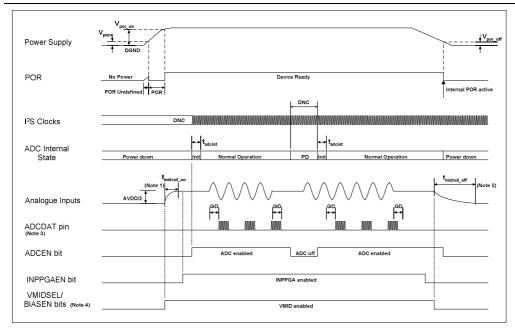


Figure 13 ADC Power Up and Down Sequence (not to scale)

SYMBOL	MIN	TYPICAL	MAX	UNIT
t <sub>midrail_on</sub>		300		ms
t <sub>midrail_off</sub>		>6		s
t <sub>adcint</sub>		2/fs		n/fs
ADC Group Delay		29/fs		n/fs

Table 3 Typical POR Operation (typical simulated values)

#### Notes:

- The analogue input pin charge time, t<sub>midrail\_on</sub>, is determined by the VMID pin charge time. This
  time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance
  and AVDD power supply rise time.
- The analogue input pin discharge time, t<sub>midrail\_off</sub>, is determined by the analogue input coupling capacitor discharge time. The time, t<sub>midrail\_off</sub>, is measured using a 1μF capacitor on the analogue input but will vary dependent upon the value of input coupling capacitor.
- 3. While the ADC is enabled there will be LSB data bit activity on the ADCDAT pin due to system noise but no significant digital output will be present.
- 4. The VMIDSEL and BIASEN bits must be set to enable analogue input midrail voltage and for normal ADC operation.
- 5. ADCDAT data output delay from power up with power supplies starting from 0V is determined primarily by the VMID charge time. ADC initialisation and power management bits may be set immediately after POR is released; VMID charge time will be significantly longer and will dictate when the device is stabilised for analogue input.
- 6. ADCDAT data output delay at power up from device standby (power supplies already applied) is determined by ADC initialisation time, 2/fs.

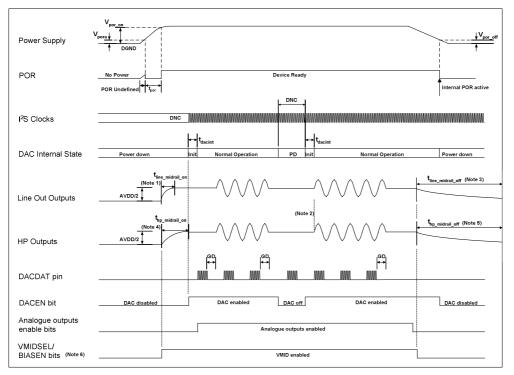


Figure 14 DAC Power Up and Down Sequence (not to scale)

SYMBOL	MIN	TYPICAL	MAX	UNIT
t <sub>line_midrail_on</sub>		300		ms
t <sub>line_midrail_off</sub>		>6		s
t <sub>hp_midrail_on</sub>		300		ms
t <sub>hpmidrail_off</sub>		>6		s
t <sub>dacint</sub>		2/fs		n/fs
DAC Group Delay		29/fs		n/fs

Table 4 Typical POR Operation (typical simulated values)



## Notes:

 The lineout charge time, t<sub>line\_midrall\_on</sub>, is determined by the VMID pin charge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time. The values above were measured using a 4.7µF capacitor.

- It is not advisable to allow DACDAT data input during initialisation of the DAC. If the DAC data
  value is not zero at point of initialisation, then this is likely to cause a pop noise on the analogue
  outputs. The same is also true if the DACDAT is removed at a non-zero value, and no mute
  function has been applied to the signal beforehand.
- 3. The lineout discharge time, t<sub>line\_midrail\_off</sub>, is determined by the VMID pin discharge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance. The values above were measured using a 4.7µF capacitor.
- The headphone charge time, t<sub>hp\_midrail\_on</sub>, is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time. The values above were measured using a 4.7μF VMID decoupling capacitor.
- The headphone discharge time, t<sub>hp\_midrall\_off</sub>, is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance. The values above were measured using a 4.7μF VMID decoupling capacitor.
- 6. The VMIDSEL and BIASEN bits must be set to enable analogue output midrail voltage and for normal DAC operation.

## RECOMMENDED L/ROUT1 ENABLE SEQUENCE

In order to minimise click noise, it is recommended that the WM8983 headphone outputs are enabled using the following sequence:

- Activate dual enable function DELEN = 1 (R42).
- Enable L/ROUT1 amplifier core, LOUT1EN = 1, ROUT1EN = 1 (R2).
- Enable output FETs, OUT1DEL = 1 (R42).
- Disable DELEN = 0.
- Reset OUT1DEL = 0.

### Notes:

All outputs on WM8983 can also be enabled with a single write to enable bits in registers 2 and 3 without click minimisation. Disabling outputs does not require click minimisation.



## **DEVICE DESCRIPTION**

## INTRODUCTION

The WM8983 is a low power audio CODEC combining a high quality stereo audio DAC and ADC, with flexible line and microphone input and output processing.

#### **FEATURES**

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

### **MICROPHONE INPUTS**

Two pairs of stereo microphone inputs are provided, allowing a pair of stereo microphones to be pseudo-differentially connected, with user defined gain. The provision of the common mode input pin for each stereo input allows for rejection of common mode noise on the microphone inputs (level depends on gain setting chosen). A microphone bias is output from the chip which can be used to bias both microphones. The signal routing can be configured to allow manual adjustment of mic levels, or to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone paths of up to +55.25dB can be selected.

#### **PGA AND ALC OPERATION**

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

#### LINE INPUTS (AUXL, AUXR)

AUXL and AUXR, can be used as a stereo line input or as an input for warning tones (or 'beeps') etc. These inputs can be summed into the record paths, along with the microphone preamp outputs, so allowing for mixing of audio with 'backing music' etc as required.

#### **ADC**

The stereo ADC uses a 24-bit high-order oversampling architecture to deliver optimum performance with low power consumption.

## HI-FI DAC

The hi-fi DAC provides high quality audio playback suitable for all portable audio hi-fi type applications, including MP3 players, portable multimedia devices and portable disc players of all types.

## **OUTPUT MIXERS**

Flexible mixing is provided on the outputs of the device. A stereo mixer is provided for the stereo headphone or line outputs, LOUT1/ROUT1, and additional summers on the OUT3/OUT4 outputs allow for an optional differential or stereo line output on these pins. Gain adjustment PGAs are provided for the LOUT1/ROUT1 and LOUT2/ROUT2 outputs, and signal switching is provided to allow for all possible signal combinations.



OUT3 and OUT4 can be configured to provide an additional stereo or mono differential lineout from the output of the DACs, the mixers or the input microphone boost stages. They can also provide a midrail reference for pseudo differential inputs to external amplifiers.

#### **AUDIO INTERFACES**

The WM8983 has a standard audio interface, to support the transmission of stereo data to and from the chip. This interface is a 3 wire standard audio interface which supports a number of audio data formats including:

- I<sup>2</sup>S
- DSP/PCM Mode (a burst mode in which LRC sync plus 2 data packed words are transmitted)
- MSB-First, left justified
- MSB-First, right justified

The interface can operate in master or slave modes.

#### **CONTROL INTERFACES**

To allow full software control over all features, the WM8983 offers a choice of 2 or 3 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

Selection of the mode is via the MODE pin. In 2 wire mode, the address of the device is fixed as 0011010.

#### **CLOCKING SCHEMES**

WM8983 offers the normal audio DAC clocking scheme operation, where 256fs MCLK is provided to the DAC and ADC.

A PLL is included which may be used to generate these clocks in the event that they are not available from the system controller. This PLL can accept a range of common input clock frequencies between 8MHz and 50MHz to generate high quality audio clocks. If this PLL is not required for generation of these clocks, it can be reconfigured to generate alternative clocks which may then be output on the GPIO pins and used elsewhere in the system.

## **POWER CONTROL**

The design of the WM8983 has given much attention to power consumption without compromising performance. It operates at very low voltages, includes the ability to power off any unused parts of the circuitry under software control, and includes standby and power off modes.

## **AUXILIARY ANALOG INPUT SUPPORT**

Additional stereo analog signals might be connected to the Line inputs of WM8983 (e.g. melody chip or FM radio), and the stereo signal listened to via headphones, or recorded, simultaneously if required.



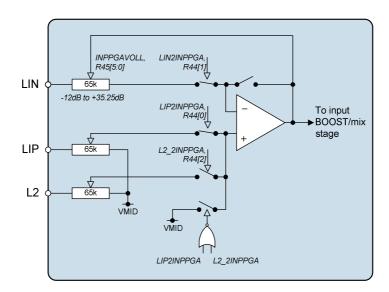
## **INPUT SIGNAL PATH**

The WM8983 has a number of flexible analogue inputs. There are two input channels, Left and Right, each of which consists of an input PGA stage followed by a boost/mix stage which drives into the hi-fi ADC. Each input path has three input pins which can be configured in a variety of ways to accommodate single-ended, differential or dual differential microphones. There are two auxiliary input pins which can be fed into to the input boost/mix stage as well as driving into the output path. A bypass path exists from the output of the boost/mix stage into the output left/right mixers.

## **MICROPHONE INPUTS**

The WM8983 can accommodate a variety of microphone configurations including single ended and pseudo differential inputs. The inputs to the left pseudo differential input PGA are LIP and L2. The inputs to the right pseudo differential input PGA are RIP and R2. LIN and RIN are used for a.c. coupled ground inputs.

In single-ended microphone input configuration the microphone signal should be input to LIN or RIN and the non-inverting input of the input PGA clamped to VMID.



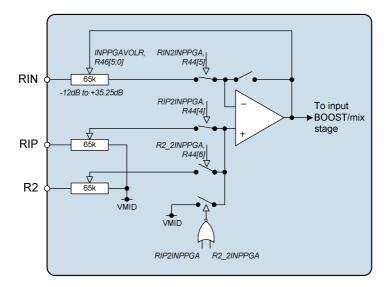


Figure 15 Microphone Input PGA Circuit



The input PGAs are enabled by the INPPGAENL and INPPGAENR register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2	2	INPPGAENL	0	Left channel input PGA enable
Power				0 = disabled
Management				1 = enabled
2	3	INPPGAENR	0	Right channel input PGA enable
				0 = disabled
				1 = enabled

Table 5 Input PGA Enable Register Settings

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input	0	LIP2INPPGA	1	Connect LIP pin to left channel input PGA amplifier positive terminal.
Control				0 = LIP not connected to input PGA
				1 = input PGA amplifier positive terminal connected to LIP (constant input impedance)
	1	LIN2INPPGA	1	Connect LIN pin to left channel input PGA negative terminal.
				0 = LIN not connected to input PGA
				1 = LIN connected to input PGA amplifier negative terminal.
	2	L2_2INPPGA	0	Connect L2 pin to left channel input PGA positive terminal.
				0 = L2 not connected to input PGA
				1 = L2 connected to input PGA amplifier positive terminal (constant input impedance).
	4	RIP2INPPGA	1	Connect RIP pin to right channel input PGA amplifier positive terminal.
				0 = RIP not connected to input PGA
				1 = right channel input PGA amplifier positive terminal connected to RIP (constant input impedance)
	5	RIN2INPPGA	1	Connect RIN pin to right channel input PGA negative terminal.
				0 = RIN not connected to input PGA
				1 = RIN connected to right channel input PGA amplifier negative terminal.
	6	R2_2INPPGA	0	Connect R2 pin to right channel input PGA positive terminal.
				0 = R2 not connected to input PGA
				1 = R2 connected to input PGA amplifier positive terminal (constant input impedance).

**Table 6 Input PGA Control** 

## **INPUT PGA VOLUME CONTROLS**

The input microphone PGAs have a gain range from -12dB to +35.25dB in 0.75dB steps. The gain from the LIN/RIN input to the PGA output and from the L2/R2 amplifier to the PGA output are always common and controlled by the register bits INPPGAVOLL/R[5:0]. These register bits also affect the LIP pin when LIP2INPPGA=1, the L2 pin when L2\_2INPPGA=1, the RIP pin when RIP2INPPGA=1 and the L2 pin when L2\_2INPPGA=1.

When the Automatic Level Control (ALC) is enabled the input PGA gains are controlled automatically and the INPPGAVOLL/R bits should not be used.



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Left channel input PGA volume control	5:0	INPPGAVOLL	010000	Left channel input PGA volume 000000 = -12dB 000001 = -11.25db 010000 = 0dB 111111 = +35.25dB
	6	INPPGAMUTEL	0	Mute control for left channel input PGA:  0 = Input PGA not muted, normal operation  1 = Input PGA muted (and disconnected from the following input BOOST stage).
	7	INPPGAZCL	0	Left channel input PGA zero cross enable:  0 = Update gain when gain register changes  1 = Update gain on 1 <sup>st</sup> zero cross after gain register write.
	8	INPPGAVU	Not latched	INPPGA left and INPPGA right volume do not update until a 1 is written to INPPGAVU (in reg 45 or 46) (See "Volume Updates" below)
R46 Right channel input PGA volume control	5:0	INPPGAVOLR	010000	Right channel input PGA volume 000000 = -12dB 000001 = -11.25db 010000 = 0dB 111111 = +35.25dB
	6	INPPGAMUTER	0	Mute control for right channel input PGA: 0 = Input PGA not muted, normal operation 1 = Input PGA muted (and disconnected from the following input BOOST stage).
	7	INPPGAZCR	0	Right channel input PGA zero cross enable:  0 = Update gain when gain register changes  1 = Update gain on 1 <sup>st</sup> zero cross after gain register write.
	8	INPPGAVU	Not latched	INPPGA left and INPPGA right volume do not update until a 1 is written to INPPGAVU (in reg 45 or 46) (See "Volume Updates" below)
R32 ALC control 1	8:7	ALCSEL	00	ALC function select:  00 = ALC off  01 = ALC right only  10 = ALC left only  11 = ALC both on

**Table 7 Input PGA Volume Control** 



## **VOLUME UPDATES**

Volume settings will not be applied to the PGAs until a '1' is written to one of the INPPGAVU bits. This is to allow left and right channels to be updated at the same time, as shown in Figure 16.

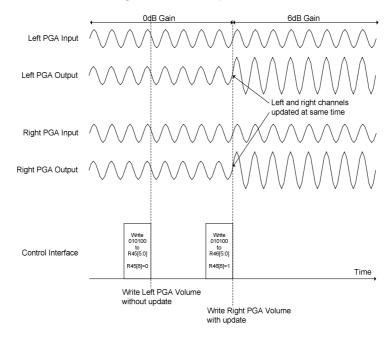


Figure 16 Simultaneous Left and Right Volume Updates

If the volume is adjusted while the signal is a non-zero value, an audible click can occur as shown in Figure 17.

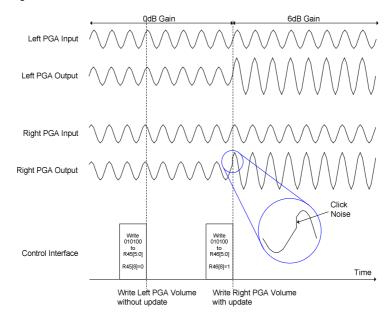


Figure 17 Click Noise during Volume Update

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 18.

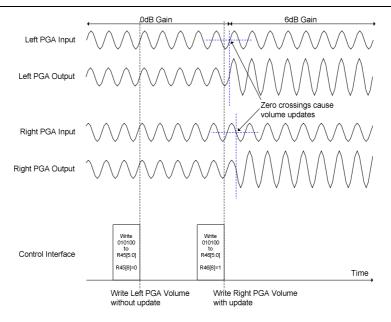


Figure 18 Volume Update Using Zero Cross Detection

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8983 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the INPPGAVU bit is set as shown in Figure 19.

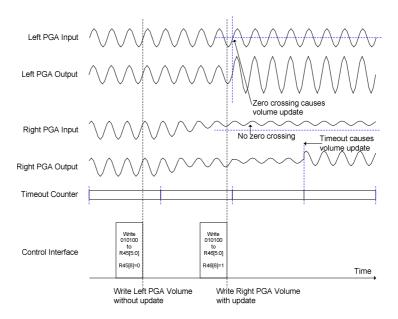


Figure 19 Volume Update after Timeout

## **AUXILLIARY INPUTS**

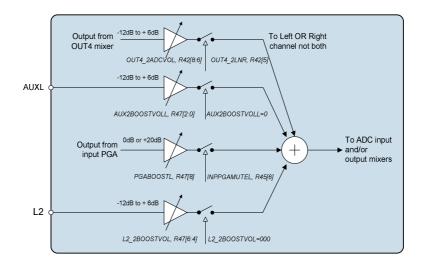
There are two auxiliary inputs, AUXL and AUXR which can be used for a variety of purposes such as stereo line inputs or as a 'beep' input signal to be mixed with the outputs.

As signal inputs, AUXL/R inputs can be used as a line input to the input BOOST stage which has adjustable gain of -12dB to +6dB in 3dB steps, with an additional "off" state (i.e. not connected to ADC input). See the INPUT BOOST section for further details.

The AUXL/R inputs can also be mixed into the output channel mixers, with a gain of -15dB to +6dB plus off.

## **INPUT BOOST**

Each of the stereo input PGA stages is followed by an input BOOST circuit. The input BOOST circuit has 3 selectable inputs: the input microphone PGA output, the AUX amplifier output and the L2/R2 input pin (can be used as a line input, bypassing the input PGA). These three inputs can be mixed together and have individual gain boost/adjust as shown in Figure 20.



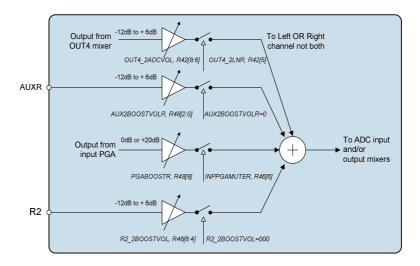


Figure 20 Input Boost Stage



The input PGA paths can have a  $\pm 20$ dB boost (PGABOOSTL/R=1) , a 0dB pass through (PGABOOSTL/R=0) or be completely isolated from the input boost circuit (INPPGAMUTEL/R=1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 Left Input	8	PGABOOSTL	1	Boost enable for left channel input PGA:
BOOST control				0 = PGA output has +0dB gain through input BOOST stage.
				1 = PGA output has +20dB gain through input BOOST stage.
R48 Right Input	8	PGABOOSTR	1	Boost enable for right channel input PGA:
BOOST control				0 = PGA output has +0dB gain through input BOOST stage.
				1 = PGA output has +20dB gain through input BOOST stage.

#### **Table 8 Input BOOST Stage Control**

The Auxilliary amplifier path to the BOOST stages is controlled by the AUXL2BOOSTVOL[2:0] and AUXR2BOOSTVOL[2:0] register bits. When AUXL2BOOSTVOL/AUXR2BOOSTVOL=000 this path is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

The L2/R2 path to the BOOST stage is controlled by the LIP2BOOSTVOL[2:0] and the RIP2BOOSTVOL[2:0] register bits. When L2\_2BOOSTVOL/R2\_2BOOSTVOL=000 the L2/R2 input pin is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R42 OUT4 to ADC	8:6	OUT4_2ADCVOL	000	Controls the OUT4 to ADC input boost stage:  000 = Path disabled (disconnected)  001 = -12dB gain  010 = -9dB gain  011 = -6dB gain  100 = -3dB gain  101 = +0dB gain  111 = +6dB gain
	5	OUT4_2LNR	0	OUT4 to L or R ADC input  0 = Right ADC input  1 = Left ADC input
R47 Left channel Input BOOST control	2:0	AUXL2BOOSTVOL	000	Controls the auxiliary amplifier to the left channel input boost stage:  000 = Path disabled (disconnected)  001 = -12dB gain  010 = -9dB gain  011 = -6dB gain  100 = -3dB gain  101 = +0dB gain  111 = +6dB gain
	6:4	L2_2BOOSTVOL	000	Controls the L2 pin to the left channel input boost stage:  000 = Path disabled (disconnected)  001 = -12dB gain  010 = -9dB gain  011 = -6dB gain  100 = -3dB gain  101 = +0dB gain  111 = +6dB gain
R48 Right channel Input BOOST control	2:0	AUXR2BOOSTVOL	000	Controls the auxiliary amplifier to the right channel input boost stage:  000 = Path disabled (disconnected)  001 = -12dB gain  010 = -9dB gain  011 = -6dB gain  100 = -3dB gain  101 = +0dB gain  111 = +6dB gain



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REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	6:4	R2_2BOOSTVOL	000	Controls the R2 pin to the right channel input boost stage:  000 = Path disabled (disconnected)  001 = -12dB  010 = -9dB gain  011 = -6dB gain  100 = -3dB gain  101 = +0dB gain  111 = +6dB gain  111 = +6dB gain

Table 9 Input BOOST Stage Control

The BOOST stage is enabled under control of the BOOSTEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2	4	BOOSTENL	0	Left channel Input BOOST enable
Power				0 = Boost stage OFF
management				1 = Boost stage ON
2	5	BOOSTENR	0	Right channel Input BOOST enable
				0 = Boost stage OFF
				1 = Boost stage ON

**Table 10 Input BOOST Enable Control** 

## MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBVSEL register bit. When MBVSEL=0, MICBIAS=0.9\*AVDD1 and when MBVSEL=1, MICBIAS=0.65\*AVDD1. The output can be enabled or disabled using the MICBEN control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1	4	MICBEN	0	Microphone Bias Enable
Power				0 = OFF (high impedance output)
management 1				1 = ON

**Table 11 Microphone Bias Enable Control** 

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44	8	MBVSEL	0	Microphone Bias Voltage Control
Input control				0 = 0.9 * AVDD1
				1 = 0.65 * AVDD1

Table 12 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 21. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.



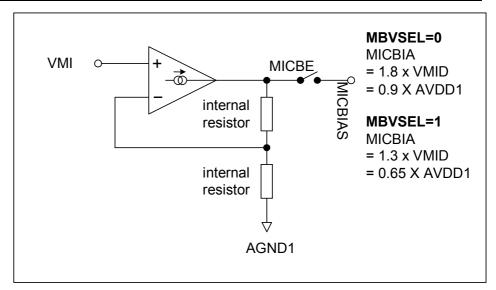


Figure 21 Microphone Bias Schematic

# **ANALOGUE TO DIGITAL CONVERTER (ADC)**

The WM8983 uses stereo multi-bit, oversampled sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD1. With a 3.3V supply voltage, the full scale level is 1.0V<sub>rms</sub>. Any voltage greater than full scale may overload the ADC and cause distortion.

# **ADC DIGITAL FILTERS**

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path for each ADC channel is illustrated in Figure 22.

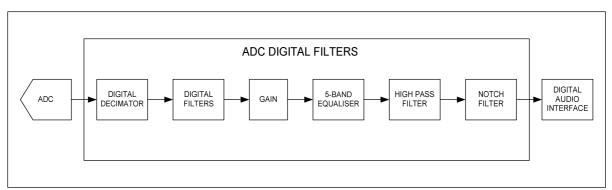


Figure 22 ADC Digital Filter Path

The ADCs are enabled by the ADCENL/R register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2	0	ADCENL	0	Enable ADC left channel:
Power				0 = ADC disabled
management 2				1 = ADC enabled
	1	ADCENR	0	Enable ADC right channel:
				0 = ADC disabled
				1 = ADC enabled

Table 13 ADC Enable Control



The polarity of the output signal can also be changed under software control using the ADCLPOL/ADCRPOL register bit. The oversampling rate of the ADC can be adjusted using the ADCOSR register bit. With ADCOSR=0 the oversample rate is 64x which gives lowest power operation and when ADCOSR=1 the oversample rate is 128x which gives best performance.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14	0	ADCLPOL	0	ADC left channel polarity adjust:
ADC Control				0 = normal
				1 = inverted
	1	ADCRPOL	0	ADC right channel polarity adjust:
				0 = normal
				1 = inverted
	3	ADCOSR	0	ADC oversample rate select:
				0 = 64x (lower power)
				1 = 128x (best performance)

Table 14 ADC Control

### SELECTABLE HIGH PASS FILTER

A selectable high pass filter is provided. To disable this filter set HPFEN=0. The filter has two modes controlled by HPFAPP. In Audio Mode (HPFAPP=0) the filter is first order, with a cut-off frequency of 3.7Hz. In Application Mode (HPFAPP=1) the filter is second order, with a cut-off frequency selectable via the HPFCUT register. The cut-off frequencies when HPFAPP=1 are shown in Table 15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	8	HPFEN	1	High Pass Filter Enable 0 = disabled 1 = enabled
	7	HPFAPP	0	Select audio mode or application mode 0 = Audio mode (1 <sup>st</sup> order, fc = ~3.7Hz) 1 = Application mode (2 <sup>nd</sup> order, fc = HPFCUT)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 16 for details.

Table 15 ADC Enable Control

HPFCUT	S	SR=101/100			SR=011/010			SR=001/000		
[2:0]					fs (kHz)					
	•	•	•	•	•	•	•	•	•	
		1.025	2	6	2.05	4	2	4.1	8	
000	82	113	122	82	113	122	82	113	122	
001	102	141	153	102	141	153	102	141	153	
010	131	180	156	131	180	156	131	180	196	
011	163	225	245	163	225	245	163	225	245	
100	204	281	306	204	281	306	204	281	306	
101	261	360	392	261	360	392	261	360	392	
110	327	450	490	327	450	490	327	450	490	
111	408	563	612	408	563	612	408	563	612	

Table 16 High Pass Filter Cut-off Frequencies (HPFAPP=1)

Note that the High Pass filter values (when HPFAPP=1) are calculated on the assumption that the SR register bits are set correctly for the actual sample rate as shown in Table 16. Sampling rate (SR) is enabled by register bits R7[1:3].



## PROGRAMMABLE IIR NOTCH FILTER

A programmable notch filter is provided. This filter has a variable centre frequency and bandwidth, programmable via two coefficients,  $a_0$  and  $a_1$ .  $a_0$  and  $a_1$  are represented by the register bits NFA0[13:0] and NFA1[13:0]. Because these coefficient values require four register writes to setup there is an NFU (Notch Filter Update) flag which should be set only when all four registers are setup.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27	6:0	NFA0[13:7]	0	Notch Filter a₀ coefficient, bits [13:7]
Notch Filter 1	7	NFEN 0		Notch filter enable: 0 = Disabled 1 = Enabled
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R28	6:0	NFA0[6:0]	0	Notch Filter a₀ coefficient, bits [6:0]
Notch Filter 2	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R29	6:0	NFA1[13:7]	0	Notch Filter a₁ coefficient, bits [13:7]
Notch Filter 3	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R30	0-6	NFA1[6:0]	0	Notch Filter a₁ coefficient, bits [6:0]
Notch Filter 4	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.

**Table 17 Notch Filter Function** 

The coefficients are calculated as follows:

$$a_0 = \frac{1 - \tan(w_b/2)}{1 + \tan(w_b/2)}$$

$$a_1 = -(1 + a_0)\cos(w_0)$$

Where:

$$w_0 = 2\pi f_c / f_s$$

$$w_h = 2\pi f_h / f_s$$

 $f_c$  = centre frequency in Hz,  $f_b$  = -3dB bandwidth in Hz,  $f_s$  = sample frequency in Hz

The actual register values can be determined from the coefficients as follows:

NFA0 = 
$$-a_0 \times 2^{13}$$

NFA1 = 
$$-a_1 \times 2^{12}$$

## **NOTCH FILTER WORKED EXAMPLE**

The following example illustrates how to calculate the  $a_0$  and  $a_1$  coefficients for a desired centre frequency and -3dB bandwidth.

$$F_c = 1000 \text{ Hz}$$

$$f_b = 100 \text{ Hz}$$

$$f_s = 48000 \text{ Hz}$$

$$w_0 = \frac{2\pi f_c}{f_s} = 2\pi \left(\frac{1000}{48000}\right) = 0.1308996939 rads$$

$$w_b = \frac{2\pi f_b}{f_s} = 2\pi \left(\frac{100}{48000}\right) = 0.01308996939 rads$$

$$a_0 = \frac{1 - \tan{(w_b/2)}}{1 + \tan{(w_b/2)}} = \frac{1 - \tan{(0.01308996939/2)}}{1 + \tan{(0.01308996939/2)}} = 0.9869949627$$

$$a_1 = -(1 + a_0)\cos(w_0) = -(1 + 0.9869949627)\cos(0.1308996939) = -1.969995945$$

NFA0 =  $-a_0 \times 2^{13} = -8085$  (rounded to nearest whole number)

NFA1 =  $-a_1 \times 2^{12}$  = 8069 (rounded to nearest whole number)

These values are then converted to a 2's complement notation:

NFA0[13:0] = 14'h1F95; Converting to 2's complement NFA0 = 14'h4000 - 14'h1F95 = 14'h206B

NFA1[13:0] = 14'h1F85; Converting to 2's complement NFA0 = 14'h1F85

# DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally attenuated over a range from -127dB to 0dB in 0.5dB steps. The gain for a given eight-bit code X is given by:

 $0.5 \times (G-255)$  dB for  $1 \le G \le 255$ ; MUTE for G = 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15	7:0	ADCLVOL	11111111	Left ADC Digital Volume Control
Left channel		[7:0]	( 0dB )	0000 0000 = Digital Mute
ADC Digital				0000 0001 = -127dB
Volume				0000 0010 = -126.5dB
				0.5dB steps up to
				1111 1111 = 0dB
	8	ADCVU	Not latched	ADC left and ADC right volume do not update until a 1 is written to ADCVU (in reg 15 or 16)
R16	7:0	ADCRVOL	11111111	Right ADC Digital Volume Control
Right channel		[7:0]	( 0dB )	0000 0000 = Digital Mute
ADC Digital				0000 0001 = -127dB
Volume				0000 0010 = -126.5dB
				0.5dB steps up to
				1111 1111 = 0dB
	8	ADCVU	Not latched	ADC left and ADC right volume do not update until a 1 is written to ADCVU (in reg 15 or 16)

Table 18 ADC Digital Volume Control

# INPUT LIMITER / AUTOMATIC LEVEL CONTROL (ALC)

The WM8983 has an automatic PGA gain control circuit, which can function as an input peak limiter or as an automatic level control (ALC).

The Automatic Level Control (ALC) provides continuous adjustment of the input PGA in response to the amplitude of the input signal. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level (ALCLVL).

If the signal is below the threshold, the ALC will increase the gain of the PGA at a rate set by ALCDCY. If the signal is above the threshold, the ALC will reduce the gain of the PGA at a rate set by ALCATK.

The ALC has two modes selected by the ALCMODE register: normal mode and peak limiter mode. The ALC/limiter function is enabled by settings the register bits R32[8:7] ALCSEL.

REGISTER	BIT	LABEL	DEFAULT	DESCRIPTION
ADDRESS				
R32 (20h)	2:0	ALCMIN	000 (-12dB)	Set minimum gain of PGA
ALC Control		[2:0]		000 = -12dB
1				001 = -6dB
				010 = 0dB
				011 = +6dB
				100 = +12dB
				101 = +18dB
				110 = +24dB
				111 = +30dB
	5:3	ALCMAX	111	Set Maximum Gain of PGA
		[2:0]	(+35.25dB)	111 = +35.25dB
				110 = +29.25dB
				101 = +23.25dB
				100 = +17.25dB
				011 = +11.25dB
				010 = +5.25dB
				001 = -0.75dB
				000 = -6.75dB
	8:7	ALCSEL	00	ALC function select
				00 = ALC disabled
				01 = Right channel ALC enabled
				10 = Left channel ALC enabled
				11 = Both channels ALC enabled
R33 (21h)	3:0	ALCLVL	1011	ALC target – sets signal level at ADC
ALC Control		[3:0]	(-6dB)	input
2				1111 = -1.5dBFS
				1110 = -1.5dBFS 1101 = -3dBFS
				1100 = -4.5dBFS
				1011 = -6dBFS
				1010 = -7.5dBFS 1001 = -9dBFS
				1001 = -9dBFS 1000 = -10.5dBFS
				0111 = -12dBFS
				0110 = -13.5dBFS
				0101 = -15dBFS 0100 = -16.5dBFS
				0011 = -18dBFS
				0010 = -19.5dBFS
				0001 = -21dBFS
				0000 = -22.5dBFS



REGISTER ADDRESS	BIT	LABEL	DEFAULT		DESC	RIPTION	
ADDRESS	7:4	ALCHLD [3:0]	0000 (0ms)	increas 0000 = 0001 = 0010 = 0011 = 0100 = 0101 =	0ms 2.67ms 5.33ms 10.66ms 21.32ms 42.64ms 85.28ms 0.17s 0.34s 0.68s 1.36s 2.7s 5.4s 10.9s 21.8 s	ore gain is	
R34 (22h) ALC Control 3	8	ALCMODE	0	operation operation	on:	C mode of	
	7:4	ALCDCY [3:0]	0011 (13ms/6dB)	,	(gain ramp- ODE ==0)	-up) time	
					Per step	Per 6dB	90% of range
				0000	410us 820us	3.3ms 6.6ms	24ms 48ms
				0010	1.64ms	13.1ms	192ms
				1010 or	420ms	vith every s	24.576s
			0011	-	(gain ramp	-up) time	
			(2.9ms/6dB)	(ALCIVI	ODE ==1) Per	Per	90% of
					step	6dB	range
				0000	90.8us	726.4us	5.26ms
				0001	181.6us	1.453ms	10.53m s
				0010	363.2us	2.905ms	21.06m s
				(time	e doubles w	ith every s	tep)
				1010	93ms	744ms	5.39s
	3:0	ALCATK [3:0]	0010 (832us/6dB)		tack (gain r ODE == 0)	amp-down)	
					Per step	Per 6dB	90% of range
				0000	104us	832us	6ms
				0001	208us	1.66ms	12ms
				0010	416us	3.32ms	24.1ms
				(time	106ms	vith every st 852ms	(ep) 6.18s
				or	1001115	UJZIIIS	0.105
				higher			



REGISTER ADDRESS	BIT	LABEL	DEFAULT		DESC	RIPTION	
			0010	ALC at	tack (gain r	amp-down)	time
			(182us/6dB)	(ALCM	ODE == 1)		
					Per	Per	90% of
					step	6dB	range
				0000	22.7us	182.4us	1.31ms
				0001	45.4us	363.2us	2.62ms
				0010	90.8us	726.4us	5.26ms
				(time	e doubles w	ith every s	tep)
				1010	23.2ms	186ms	1.348s

Table 19 ALC Control Registers

When the ALC is disabled, the input PGA remains at the last controlled value of the ALC. An input gain update must be made by writing to the INPPGAVOLL/R register bits.

## **NORMAL MODE**

In normal mode, the ALC will attempt to maintain a constant signal level by increasing or decreasing the gain of the PGA. The following diagram shows an example of this.

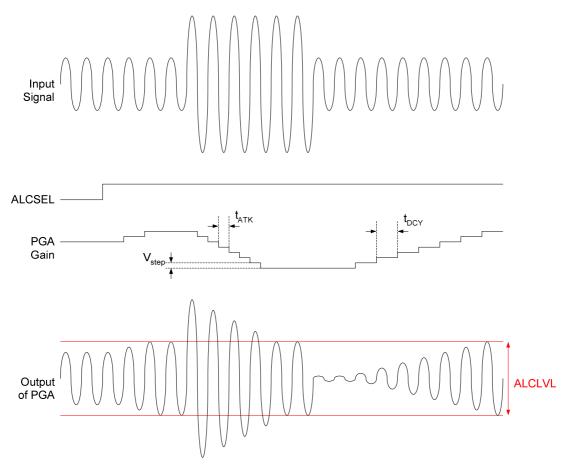


Figure 23 ALC Normal Mode Operation

# LIMITER MODE

In limiter mode, the ALC will reduce peaks that go above the threshold level, but will not increase the PGA gain beyond the starting level. The starting level is the PGA gain setting when the ALC is enabled in limiter mode. If the ALC is started in limiter mode, this is the gain setting of the PGA at startup. If the ALC is switched into limiter mode after running in ALC mode, the starting gain will be the gain at switchover. The diagram below shows an example of limiter mode.

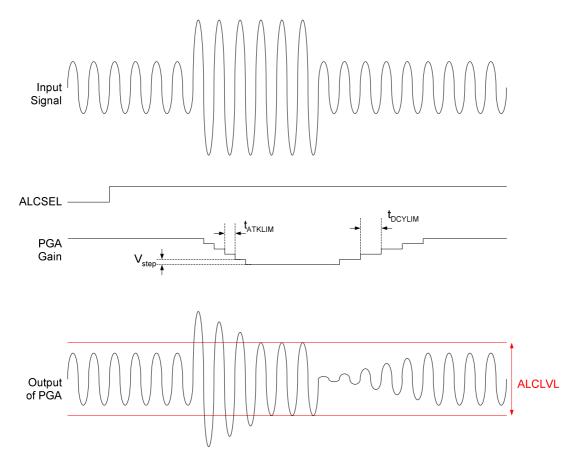


Figure 24 ALC Limiter Mode Operation

# **ALC LIMITER MODE INITIALISATION SEQUENCE**

In order to correctly initialise the ALC in limiter mode, the following sequence of register writes is required. MCLK must be applied during the initialisation sequence

- 1. R-5 Set left input PGA gain (INPPGAVOLL) to level required for operation.
- 2. R-6 Set right input PGA gain (INPPGAVOLR) to level required for operation.
- 3. R-4 Enable analogue inputs as required.
- 4. -2 Disable input PGA (INPPGAEN = 0).
- 5. R59 = 0x00-3 Enable ALC test mode.
- 6. R-2 Set ALCMAXGAIN and ALCMINGAIN to the level required for operation.
- 7. R-3 Set limiter level (ALCLVL) to the level required for operation.
- 8. R34 = 0x00-0 Enable ALC mode (ALCMODE = 0).
- 9. Insert 1ms delay to allow input PGA gain update by the limiter circuit.

- 10. R34 = 0x01-0 Enable Limiter mode (ALCMODE = 1).
- 11. Insert 1ms delay to allow input PGA gain update by the limiter circuit.
- 12. R59 = 0x00-0 Turn off ALC test mode.
- 13. -2 Enable input PGA (INPPGAENL/R = 1).

**Note:** R32, R33, R45 and R46 register settings above need to be changed to reflect settings required in the target application.

## ATTACK AND DECAY TIMES

The attack and decay times set the update times for the PGA gain. The attack time is the time constant used when the gain is reducing. The decay time is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode. The time constants are shown below in terms of a single gain step, a change of 6dB and a change of 90% of the PGAs gain range.

Note that, these times will vary slightly depending on the sample rate used (specified by the SR register).

# **NORMAL MODE**

ALCMODE =	ALCMODE = 0 (Normal Mode)						
	Attack Time (s)						
ALCATK	t <sub>ATK</sub>	t <sub>ATK6dB</sub>	t <sub>ATK90%</sub>				
0000	104µs	832µs	6ms				
0001	208µs	1.66ms	12ms				
0010	416µs	3.33ms	24ms				
0011	832µs	6.66ms	48ms				
0100	1.66ms	13.32ms	96ms				
0101	3.33ms	26.64ms	192ms				
0110	6.66ms	53.28ms	384ms				
0111	13.32ms	106.6ms	768ms				
1000	26.64ms	213.2ms	1.53s				
1001	53.28ms	426.4ms	3.07s				
1010	106.6ms	852.8ms	6.14s				

ALCMODE =	ALCMODE = 0 (Normal Mode)					
	Decay Time (s)					
ALCDCY	t <sub>DCY</sub>	t <sub>DCY6dB</sub>	t <sub>DCY90%</sub>			
0000	410µs	3.3ms	24ms			
0001	820µs	6.6ms	48ms			
0010	1.64ms	13.1ms	96ms			
0011	3.28ms	26.2ms	192ms			
0100	6.56ms	52.5ms	384ms			
0101	13.12ms	105ms	768ms			
0110	26.24ms	210ms	1.53s			
0111	52.5ms	420ms	3.07s			
1000	105ms	840ms	6.14s			
1001	210ms	1.68s	12.28s			
1010	420ms	3.36s	24.57s			

Table 20 ALC Normal Mode (Attack and Decay times)



# LIMITER MODE

ALCMODE =	ALCMODE = 1 (Limiter Mode)						
		Attack Time (s)					
ALCATK	t <sub>ATKLIM</sub>	t <sub>ATKLIM6dB</sub>	t <sub>ATKLIM90%</sub>				
0000	22.7µs	182.4µs	1.31ms				
0001	45.4µS	363.2µs	2.62ms				
0010	90.8µS	726.4µs	5.24ms				
0011	182µS	1.45ms	10.48ms				
0100	363µS	2.9ms	20.9ms				
0101	726µS	5.81ms	41.9ms				
0110	1.45ms	11.62ms	83.8ms				
0111	2.9ms	23.2ms	167.7ms				
1000	5.81ms	46.5ms	335.4ms				
1001	11.62ms	93ms	670.8ms				
1010	23.2ms	186ms	1.34s				

ALCMODE =	ALCMODE = 1 (Limiter Mode)						
		Attack Time (s)					
ALCDCY	t <sub>DCYLIM</sub>	t <sub>DCYLIM6dB</sub>	t <sub>DCYLIM90%</sub>				
0000	90.8µs	726.4µs	5.24ms				
0001	182µS	1.45ms	10.48ms				
0010	363µS	2.9ms	20.9ms				
0011	726µS	5.81ms	41.9ms				
0100	1.45ms	11.62ms	83.8ms				
0101	2.9ms	23.2ms	167.7ms				
0110	5.81ms	46.5ms	335.4ms				
0111	11.62ms	93ms	670.8ms				
1000	23.2ms	186ms	1.34s				
1001	46.4ms	372ms	2.68s				
1010	92.8ms	744ms	5.36s				

Table 21 ALC Limiter Mode (Attack and Decay times)

# **MINIMUM AND MAXIMUM GAIN**

The ALCMIN and ALCMAX register bits set the minimum/maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32	5:3	ALCMAX	111	Set Maximum Gain of PGA
ALC Control 1	2:0	ALCMIN	000	Set minimum gain of PGA

Table 22 ALC Max/Min Gain

In normal mode, ALCMAX sets the maximum boost which can be applied to the signal. In limiter mode, ALCMAX will normally have no effect (assuming the starting gain value is less than the maximum gain specified by ALCMAX) because the maximum gain is set at the starting gain level.

ALCMIN sets the minimum gain value which can be applied to the signal.

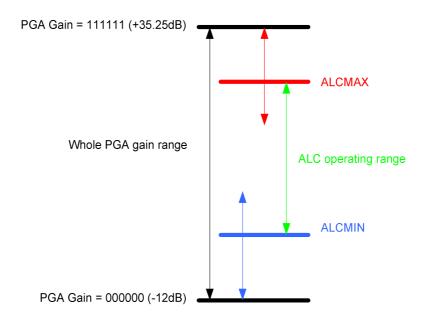


Figure 25 ALC Min/Max Gain

ALCMAX	Maximum Gain (dB)
111	35.25
110	29.25
101	23.25
100	17.25
011	11.25
010	5.25
001	-0.75
000	-6.75

Table 23 ALC Max Gain Values



ALCMIN	Minimum Gain (dB)
000	-12
001	-6
010	0
011	6
100	12
101	18
110	24
111	30

## Table 24 ALC Min Gain Values

Note that if the ALC gain setting strays outside the ALC operating range, either by starting the ALC outside of the range or changing the ALCMAX or ALCMIN settings during operation, the ALC will immediately adjust the gain to return to the ALC operating range. It is recommended that the ALC starting gain is set between the ALCMAX and ALCMIN limits.

# ALC HOLD TIME (NORMAL MODE ONLY)

In Normal mode, the ALC has an adjustable hold time which sets a time delay before the ALC begins its decay phase (gain increasing). The hold time is set by the ALCHLD register.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R33	7:4	ALCHLD	0000	ALC hold time before gain is increased.
ALC Control 2				

Table 25 ALC Hold Time

If the hold time is exceeded this indicates that the signal has reached a new average level and the ALC will increase the gain to adjust for that new average level. If the signal goes above the threshold during the hold period, the hold phase is abandoned and the ALC returns to normal operation.



WM8983 Production Data

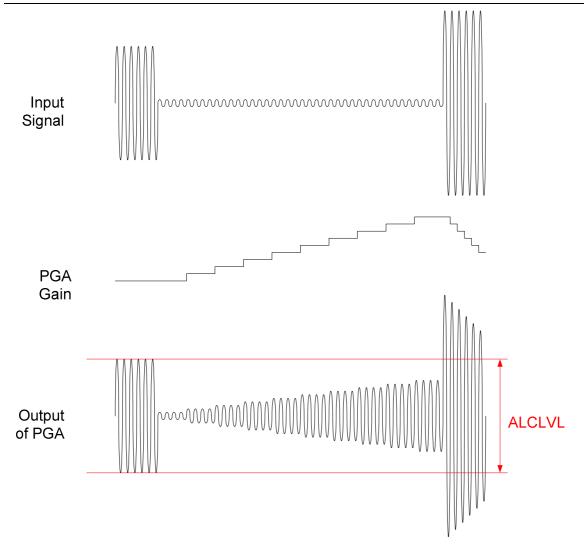


Figure 26 ALCLVL

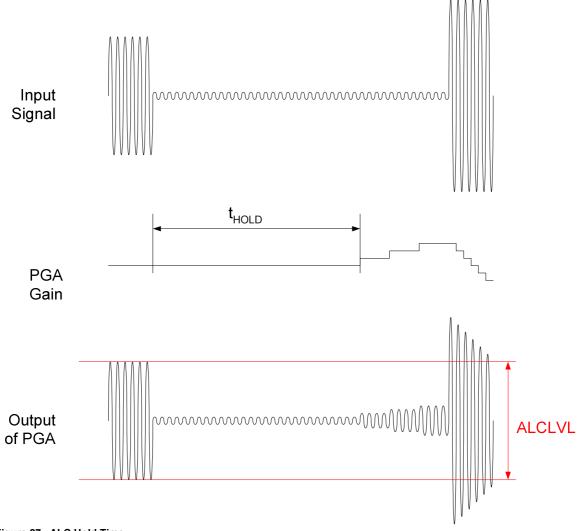


Figure 27 ALC Hold Time

ALCHLD	t <sub>HOLD</sub> (s)
0000	0
0001	2.67ms
0010	5.34ms
0011	10.7ms
0100	21.4ms
0101	42.7ms
0110	85.4ms
0111	171ms
1000	342ms
1001	684ms
1010	1.37s

Table 26 ALC Hold Time Values

## **PEAK LIMITER**

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (-1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ALCATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

**Note:** If ALCATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

# **NOISE GATE (NORMAL MODE ONLY)**

When the signal is very quiet and consists mainly of noise, the ALC function may cause "noise pumping", i.e. loud hissing noise during silence periods. The WM8985 has a noise gate function that prevents noise pumping by comparing the signal level at the input pins against a noise gate threshold, NGTH. The noise gate cuts in when:

Signal level at ADC [dBFS] < NGTH [dBFS] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

Signal level at input pin [dBFS] < NGTH [dBFS]

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 6dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set—up of the function. The noise gate only operates in conjunction with the ALC and cannot be used in limiter mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 (23h)	2:0	NGTH	000	Noise gate threshold:
ALC Noise Gate				000 = -39dB
Control				001 = -45dB
				010 = -51db
				011 = -57dB
				100 = -63dB
				101 = -70dB
				110 = -76dB
				111 = -81dB
	3	NGATEN	0	Noise gate function enable
				1 = enable
				0 = disable

**Table 27 ALC Noise Gate Control** 



The diagrams below show the response of the system to the same signal with and without noise gate.

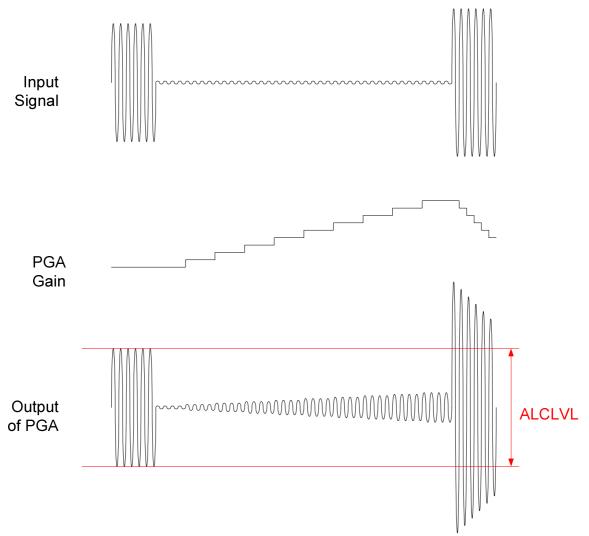


Figure 28 ALC Operation Above Noise Gate Threshold

WM8983 Production Data

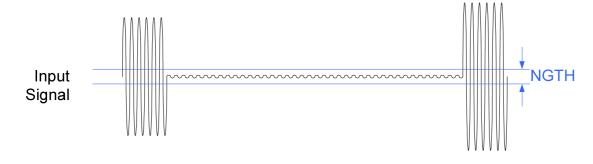






Figure 29 Noise Gate Operation

# **OUTPUT SIGNAL PATH**

The WM8983 output signal paths consist of digital application filters, up-sampling filters, stereo Hi-Fi DACs, analogue mixers, stereo headphone and stereo line/mono/midrail output drivers. The digital filters and DAC are enabled by register bits DACENL And DACENR. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8983, irrespective of whether the DACs are running or not.

The WM8983 DACs receive digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control
- Graphic equaliser
- A digital peak limiter.
- Sigma-Delta Modulation

High performance sigma-delta audio DAC converts the digital data into an analogue signal.

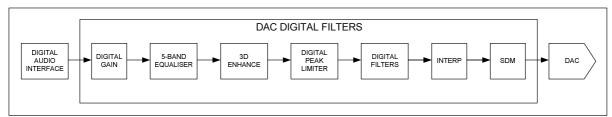


Figure 30 DAC Digital Filter Path



The analogue outputs from the DACs can then be mixed with the aux analogue inputs and the ADC analogue inputs. The mix is fed to the output drivers for headphone (LOUT1/ROUT1, LOUT2/ROUT2) or line (OUT3/OUT4). OUT3 and OUT4 have additional mixers which allow them to output different signals to the headphone and line outputs.

### **DIGITAL PLAYBACK (DAC) PATH**

Digital data is passed to the WM8983 via the flexible audio interface and is then passed through a variety of advanced digital filters as shown in Figure 30 to the hi-fi DACs. The DACs are enabled by the DACENL/R register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3	0	DACENL	0	Left channel DAC enable
Power				0 = DAC disabled
Management 3				1 = DAC enabled
	1	DACENR	0	Right channel DAC enable
				0 = DAC disabled
				1 = DAC enabled

#### **Table 28 DAC Enable Control**

The WM8983 also has a Soft Mute function, which when enabled, gradually attenuates the volume of the digital signal to zero. When disabled, the gain will ramp back up to the digital gain setting. This function is enabled by default. To play back an audio signal, it must first be disabled by setting the SOFTMUTE bit to zero.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10	0	DACPOL	0	Left DAC output polarity:
DAC Control				0 = non-inverted
				1 = inverted (180 degrees phase shift)
	1	DACRPOL	0	Right DAC output polarity:
				0 = non-inverted
				1 = inverted (180 degrees phase shift)
	2	AMUTE	0	Automute enable
				0 = Amute disabled
				1 = Amute enabled
	3	DACOSR	0	DAC oversampling rate:
				0 = 64x (lowest power)
				1 = 128x (best performance)
	6	SOFTMUTE	0	Softmute enable:
				0 = Enabled
				1 = Disabled

# Table 29 DAC Control Register

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters the multi-bit, sigma-delta DACs, which convert it to a high quality analogue audio signal. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

The DAC output phase defaults to non-inverted. Setting DACLPOL will invert the DAC output phase on the left channel and DACRPOL inverts the phase on the right channel.

### **AUTO-MUTE**

The DAC has an auto-mute function which applies an analogue mute when 1024 consecutive zeros are detected. The mute is released as soon as a non-zero sample is detected. Auto-mute can be disabled using the AMUTE control bit.



# **DIGITAL HI-FI DAC VOLUME (GAIN) CONTROL**

The signal volume from each Hi-Fi DAC can be controlled digitally. The gain range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

 $0.5 \times (X-255)$  dB for  $1 \le X \le 255$ ; MUTE for X = 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11	7:0	DACLVOL	11111111	Left DAC Digital Volume Control
Left DAC		[7:0]	( 0dB )	0000 0000 = Digital Mute
Digital Volume				0000 0001 = -127dB
				0000 0010 = -126.5dB
				0.5dB steps up to
				1111 1111 = 0dB
	8	DACVU	Not	DAC left and DAC right volume do
			latched	not update until a 1 is written to
				DACVU (in reg 11 or 12)
R12	7:0	DACRVOL	11111111	Right DAC Digital Volume Control
Right DAC		[7:0]	( 0dB )	0000 0000 = Digital Mute
Digital Volume				0000 0001 = -127dB
				0000 0010 = -126.5dB
				0.5dB steps up to
				1111 1111 = 0dB
	8	DACVU	Not	DAC left and DAC right volume do
			latched	not update until a 1 is written to
				DACVU (in reg 11 or 12)

**Table 30 DAC Digital Volume Control** 

**Note:** An additional gain of up to 12dB can be added using the gain block embedded in the digital peak limiter circuit (see DAC OUTPUT LIMITER section).

### **5-BAND EQUALISER**

A 5-band graphic equaliser function which can be used to change the output frequency levels to suit the environment. This can be applied to the ADC or DAC path and is described in the 5-BAND EQUALISER section for further details on this feature.

### **3-D ENHANCEMENT**

The WM8983 has an advanced digital 3-D enhancement feature which can be used to vary the perceived stereo separation of the left and right channels. Like the 5-band equaliser this feature can be applied to either the ADC record path or the DAC playback path but not both simultaneously. Refer to the 3-D STEREO ENHANCEMENT section for further details on this feature.

# **DAC DIGITAL OUTPUT LIMITER**

The WM8983 has a digital output limiter function. The operation of this is shown in Figure 31. In this diagram the upper graph shows the envelope of the input/output signals and the lower graph shows the gain characteristic.



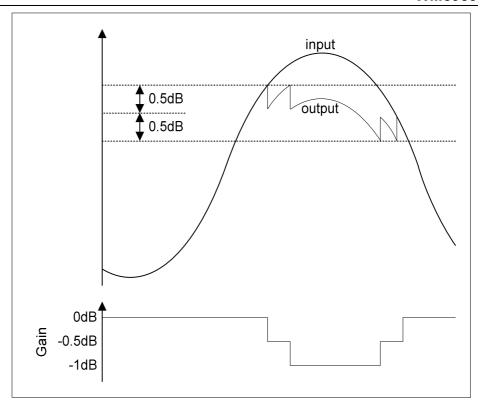


Figure 31 DAC Digital Limiter Operation

The limiter has a programmable upper threshold which is close to 0dB. Referring to Figure 31, in normal operation (LIMBOOST=000 => limit only) signals below this threshold are unaffected by the limiter. Signals above the upper threshold are attenuated at a specific attack rate (set by the LIMATK register bits) until the signal falls below the threshold. The limiter also has a lower threshold 1dB below the upper threshold. When the signal falls below the lower threshold the signal is amplified at a specific decay rate (controlled by LIMDCY register bits) until a gain of 0dB is reached. Both threshold levels are controlled by the LIMLVL register bits. The upper threshold is 0.5dB above the value programmed by LIMLVL and the lower threshold is 0.5dB below the LIMLVL value.

# **VOLUME BOOST**

The limiter has programmable upper gain which boosts signals below the threshold to compress the dynamic range of the signal and increase its perceived loudness. This operates as an ALC function with limited boost capability. The volume boost is from 0dB to +12dB in 1dB steps, controlled by the LIMBOOST register bits.

The output limiter volume boost can also be used as a stand alone digital gain boost when the limiter is disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 DAC digital limiter control 1	3:0	LIMATK	0010	Limiter Attack time (per 6dB gain change) for 44.1kHz sampling. Note that these are proportionally related to sample rate.  0000 = 94us 0001 = 188s 0010 = 375us 0011 = 750us 0100 = 1.5ms 0101 = 3ms 0110 = 6ms 0111 = 12ms 1000 = 24ms 1001 = 48ms 1010 = 96ms 1011 to 1111 = 192ms
	7:4	LIMDCY	0011	Limiter Decay time (per 6dB gain change) for 44.1kHz sampling. Note that these are proportionally related to sample rate:  0000 = 750us  0001 = 1.5ms  0010 = 3ms  0011 = 6ms  0100 = 12ms  0101 = 24ms  0110 = 48ms  0111 = 96ms  1000 = 192ms  1001 = 384ms  1010 = 768ms  1011 to 1111 = 1.536s
	8	LIMEN	0	Enable the DAC digital limiter: 0 = disabled 1 = enabled
R25 DAC digital limiter control 2	3:0	LIMBOOST	0000	Limiter volume boost (can be used as a stand alone volume boost when LIMEN=0): 0000 = 0dB 0001 = +1dB 0010 = +2dB 0011 = +3dB 0100 = +4dB 0110 = +5dB 0110 = +6dB 0111 = +7dB 1000 = +8dB 1001 = +9dB 1010 = +10dB 1011 = +11dB 1100 = +12dB 1101 to 11111 = reserved
	6:4	LIMLVL	000	Programmable signal threshold level (determines level at which the limiter starts to operate)  000 = -1dB  001 = -2dB  010 = -3dB  011 = -4dB  100 = -5dB  101 to 111 = -6dB

Table 31 DAC Digital Limiter Control



# **5-BAND GRAPHIC EQUALISER**

A 5-band graphic equaliser is provided, which can be applied to the ADC or DAC path, together with 3D enhancement, under control of the EQ3DMODE register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 EQ Control 1	8	EQ3DMODE	1	0 = Equaliser and 3D Enhancement applied to ADC path
				1 = Equaliser and 3D Enhancement applied to DAC path

Table 32 EQ and 3D Enhancement DAC or ADC Path Select

Note: The ADCs and DACs must be disabled before changing the EQ3DMODE bit.

The equaliser consists of low and high frequency shelving filters (Band 1 and 5) and three peak filters for the centre bands. Each has adjustable cut-off or centre frequency, and selectable boost (+/-12dB in 1dB steps). The peak filters have selectable bandwidth.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18	4:0	EQ1G	01100	Band 1 Gain Control. See Table 38 for
EQ Band 1			(0dB)	details.
Control	6:5	EQ1C	01	Band 1 Cut-off Frequency:
				00 = 80Hz
				01 = 105Hz
				10 = 135Hz
				11 = 175Hz

Table 33 EQ Band 1 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 EQ Band 2	4:0	EQ2G	01100 (0dB)	Band 2 Gain Control. See Table 38 for details.
Control	6:5	EQ2C	01	Band 2 Centre Frequency: 00 = 230Hz 01 = 300Hz 10 = 385Hz 11 = 500Hz
	8	EQ2BW	0	Band 2 Bandwidth Control 0 = narrow bandwidth 1 = wide bandwidth

Table 34 EQ Band 2 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 EQ Band 3	4:0	EQ3G	01100 (0dB)	Band 3 Gain Control. See Table 38 for details.
Control	6:5	EQ3C	01	Band 3 Centre Frequency: 00 = 650Hz 01 = 850Hz 10 = 1.1kHz 11 = 1.4kHz
	8	EQ3BW	0	Band 3 Bandwidth Control 0 = narrow bandwidth 1 = wide bandwidth

Table 35 EQ Band 3 Control



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 EQ Band 4	4:0	EQ4G	01100 (0dB)	Band 4 Gain Control. See Table 38 for details
Control	6:5	EQ4C	01	Band 4 Centre Frequency: 00 = 1.8kHz 01 = 2.4kHz 10 = 3.2kHz 11 = 4.1kHz
	8	EQ4BW	0	Band 4 Bandwidth Control 0 = narrow bandwidth 1 = wide bandwidth

Table 36 EQ Band 4 Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R22 EQ Band 5	4:0	EQ5G	01100 (0dB)	Band 5 Gain Control. See Table 38 for details.
Gain Control	6:5	EQ5C	01	Band 5 Cut-off Frequency: 00 = 5.3kHz 01 = 6.9kHz 10 = 9kHz 11 = 11.7kHz

Table 37 EQ Band 5 Control

GAIN REGISTER	GAIN			
00000	+12dB			
00001	+11dB			
00010	+10dB			
00011	+9dB			
00100	+8dB			
00101	+7dB			
00110	+6dB			
00111	+5dB			
01000	+4dB			
01001	+3dB			
01010	+2dB			
01011	+1dB			
01100	0dB			
01101	-1dB			
11000	-12dB			
11001 to 11111	Reserved			

Table 38 Gain Register Table

See also Figure 60 to Figure 77 for equaliser and high pass filter responses.

# **3D STEREO ENHANCEMENT**

The WM8983 has a digital 3D enhancement option to increase the perceived separation between the left and right channels. Selection of 3D for record or playback is controlled by register bit EQ3DMODE. Switching this bit from record to playback or from playback to record may only be done when ADC and DAC are disabled. The WM8983 control interface will only allow EQ3DMODE to be changed when ADC and DAC are disabled (ie ADCENL = 0, ADCENR = 0, DACENL = 0 and DACENR = 0).

The DEPTH3D setting controls the degree of stereo expansion.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h)	3:0	DEPTH3D[3:0]	0000	Stereo depth
3D Control				0000 = Disabled
				0001 = 6.67%
				0010 = 13.3%
				0011 = 20%
				0100 = 26.7%
				0101 = 33.3%
				0110 = 40%
				0111 = 46.6%
				1000 = 53.3%
				1001 = 60%
				1010 = 66.7%
				1011 = 73.3%
				1100 = 80%
				1101 = 86.7%
				1110 = 93.3%
				1111 = 100% (maximum 3D effect)

Table 39 3D Stereo Enhancement Function

**Note:** When 3D enhancement is used, it may be necessary to attenuate the signal by 6dB to avoid limiting.

## **ANALOGUE OUTPUTS**

The WM8983 has three sets of stereo analogue outputs. These are:

- LOUT1 and ROUT1 which are normally used to drive a headphone load.
- LOUT2 and ROUT2 which can be used as speaker, headphone or line drivers.
- OUT3 and OUT4 can be configured as a stereo line out (OUT3 is left output and OUT4 is right output). OUT4 can also be used to provide a mono mix of left and right channels.

The outputs LOUT2, ROUT2 OUT3 and OUT4 are powered from AVDD2 and are capable of driving a 1V rms signal (AVDD1/3.3) in non-boost mode and AVDD1\*1.5/3.3 in boost mode.

LOUT1 and ROUT1 are supplied from AVDD1 and can drive out a 1V rms signal (AVDD1/3.3).

LOUT1, ROUT1, LOUT2 and ROUT2 have individual analogue volume PGAs with -57dB to +6dB gain ranges.

There are four output mixers in the output signal path, the left and right channel mixers which control the signals to headphone (and optionally the line outputs) and also dedicated OUT3 and OUT4 mixers.



# LEFT AND RIGHT OUTPUT CHANNEL MIXERS

The left and right output channel mixers are shown in Figure 32. These mixers allow the AUX inputs, the ADC bypass and the DAC left and right channels to be combined as desired. This allows a mono mix of the DAC channels to be performed as well as mixing in external line-in from the AUX or speech from the input bypass path.

The AUX and bypass inputs have individual volume control from -15dB to +6dB and the DAC volume can be adjusted in the digital domain if required. The output of these mixers is connected to the headphone outputs (LOUT1, ROUT1, LOUT2 and ROUT2) and can optionally be connected to the OUT3 and OUT4 mixers.

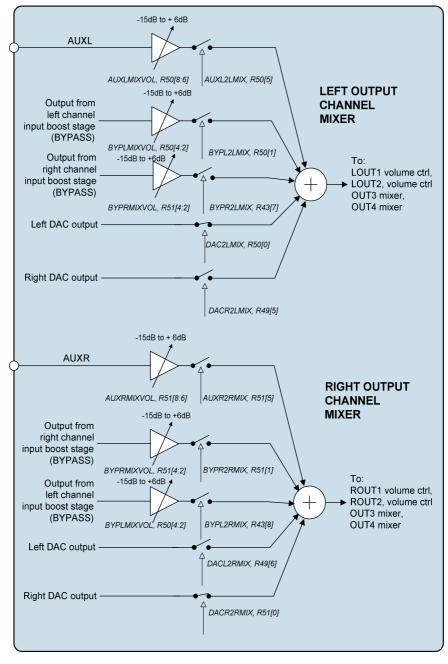


Figure 32 Left/Right Output Channel Mixers



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 Output mixer control	8	BYPL2RMIX	0	Left bypass path (from the Left channel input PGA stage) to right output mixer  0 = not selected
				1 = selected
R43 Output mixer control	7	BYPR2LMIX	0	Right bypass path (from the right channel input PGA stage) to Left output mixer  0 = not selected
				1 = selected
R49 Output mixer control	5	DACR2LMIX	0	Right DAC output to left output mixer 0 = not selected 1 = selected
	6	DACL2RMIX	0	Left DAC output to right output mixer 0 = not selected 1 = selected
R50 Left channel output mixer	0	DACL2LMIX	1	Left DAC output to left output mixer 0 = not selected 1 = selected
control	1	BYPL2LMIX	0	Left bypass path (from the left channel input PGA stage) to left output mixer  0 = not selected  1 = selected
	4:2	BYPLMIXVOL	000	Left bypass volume control to output channel mixer: 000 = -15dB 001 = -12dB 010 = -9dB 011 = -6dB 100 = -3dB 101 = 0dB 110 = +3dB 111 = +6dB
	5	AUXL2LMIX	0	Left Auxilliary input to left channel output mixer:  0 = not selected  1 = selected
	8:6	AUXLMIXVOL	000	Aux left channel input to left mixer volume control:  000 = -15dB  001 = -12dB  010 = -9dB  011 = -6dB  100 = -3dB  101 = 0dB  110 = +3dB  111 = +6dB



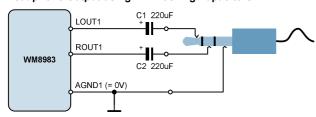
REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 Right channel	0	DACR2RMIX	1	Right DAC output to right output mixer
output mixer				0 = not selected
control				1 = selected
	1	BYPR2RMIX	0	Right bypass path (from the right channel input PGA stage) to right output mixer
				0 = not selected
				1 = selected
	4:2	BYPRMIXVOL	000	Right bypass volume control to output channel mixer:
				000 = -15dB
				001 = -12dB
				010 = -9dB
				011 = -6dB
				100 = -3dB
				101 = 0dB
				110 = +3dB
			_	111 = +6dB
	5	AUXR2RMIX	0	Right Auxiliary input to right channel output mixer:
				0 = not selected
				1 = selected
	8:6	AUXRMIXVOL	000	Aux right channel input to right mixer volume control:
				000 = -15dB
				001 = -12dB
				010 = -9dB
				011 = -6dB
				100 = -3dB
				101 = 0dB
				110 = +3dB
				111 = +6dB
R3	2	LMIXEN	0	Left output channel mixer enable:
Power				0 = disabled
management 3				1 = enabled
3	3	RMIXEN	0	Right output channel mixer enable:
				0 = disabled
				1 = enabled

Table 40 Left and Right Output Mixer Control

## **HEADPHONE OUTPUTS (LOUT1 AND ROUT1)**

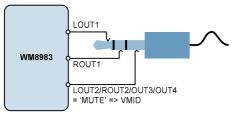
The headphone outputs LOUT1 and ROUT1 can drive a  $16\Omega$  or  $32\Omega$  headphone load, either through DC blocking capacitors, or DC-coupled to a buffered midrail reference as shown in Figure 33. OUT3, OUT4, LOUT2 or ROUT2 could be used as this buffered reference if one of these outputs is not being used, saving decoupling capacitors, at the expense of increased power consumption. For fully independent left and right channels, two separate midrail references can be used, eliminating crosstalk caused by headphone ground impedances, at the expense of increased power consumption.

### Headphone Output using DC Blocking Capacitors:



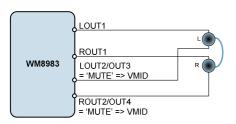
Lowest power consumption (Two outputs enabled); Large and expensive capacitors; Bass response may be reduced for smaller capacitors; Impedance in common ground may introduce crosstalk.

### **DC Coupled Headphone Output:**



Higher power consumption (Three outputs enabled); Improved PSRR if AVDD2 connected to AVDD1; Impedance in common ground may introduce crosstalk; Improved bass response (DC connection).

## DC Coupled with Fully Independent Left / Right Drive:



Highest power consumption (Four outputs enabled); Improved PSRR if AVDD2 connected to AVDD1; Independent L/R pseudo-ground eliminates crosstalk; Improved bass response (DC connection); Non-standard headphone connection may not be suitable for some applications.

Figure 33 Recommended Headphone Output Configurations

Each headphone output has an analogue volume control PGA with a gain range of -57dB to +6dB.

When DC blocking capacitors are used, their capacitance and the load resistance together determine the lower cut-off frequency of the output signal,  $f_c$ . Increasing the capacitance lowers  $f_c$ , improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a  $16\Omega$  load and C1, C2 =  $220\mu F$ :

 $f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu F) = 45 Hz$ 

In the DC coupled configuration, the headphone "ground" is connected to the VMID pin. The OUT3/4 pins can be configured as a DC output driver by setting the OUT3MUTE and OUT4MUTE register bit. The DC voltage on VMID in this configuration is equal to the DC offset on the LOUT1 and ROUT1 pins therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

Note that LOUT2, ROUT2, OUT3 and OUT4 have an optional output boost of 1.5x. When these are configured in this output boost mode (SPKBOOST/OUT3BOOST/OUT4BOOST=1) then the VMID value of these outputs will be equal to 1.5xAVDD/2 and will not match the VMID of the headphone drivers. Do not use the DC coupled output mode in this configuration.

It is recommended to connect the DC coupled outputs only to headphones, and not to the line input of another device. Although the built-in short circuit protection will prevent any damage to the headphone outputs, such a connection may be noisy, and may not function properly if the other device is grounded.



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R52 LOUT1	7	LOUT1ZC	0	Headphone volume zero cross enable:
Volume control				1 = Change gain on zero cross only 0 = Change gain immediately
	6	LOUT1MUTE	0	Left headphone output mute: 0 = Normal operation 1 = Mute
	5:0	LOUT1VOL	111001	Left headphone output volume: 000000 = -57dB 000001 = -56dB  111001 = 0dB  111111 = +6dB
	8	HPVU	Not latched	LOUT1 and ROUT1 volumes do not update until a 1 is written to OUT1VU (in reg 52 or 53)
R53 ROUT1 Volume control	7	ROUT1ZC	0	Headphone volume zero cross enable:  1 = Change gain on zero cross only  0 = Change gain immediately
	6	ROUT1MUTE	0	Right headphone output mute: 0 = Normal operation 1 = Mute
	5:0	ROUT1VOL	111001	Right headphone output volume: 000000 = -57dB 000001 = -56dB  111001 = 0dB  111111 = +6dB
	8	HPVU	Not latched	LOUT1 and ROUT1 volumes do not update until a 1 is written to OUT1VU (in reg 52 or 53)

**Table 41 OUT1 Volume Control** 

# **SPEAKER OUTPUTS (LOUT2 AND ROUT2)**

The outputs LOUT2 and ROUT2 are designed to drive an  $8\Omega$  BTL speaker but can optionally drive two headphone loads of  $16\Omega/32\Omega$  or a line output (see Headphone Output and Line Output sections, respectively). Each output has an individual volume control PGA, an output boost/level shift bit, a mute and an enable as shown in Figure 34. LOUT2 and ROUT2 output the left and right channel mixer outputs respectively.

The ROUT2 signal path also has an optional invert. The amplifier used for this invert can be used to mix in the AUXR signal with an adjustable gain range of -15dB -> +6dB. This allows a 'beep' signal to be applied only to the speaker output without affecting the HP or line outputs.



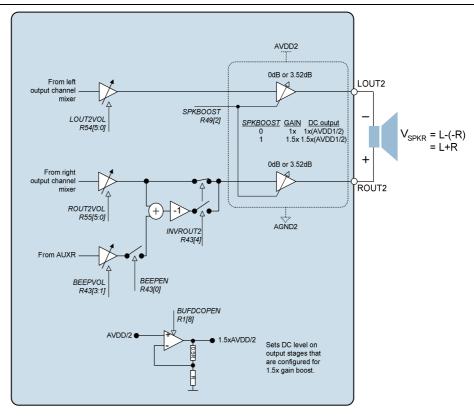


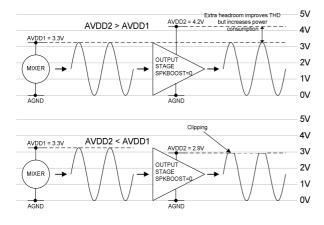
Figure 34 Speaker Outputs LOUT2 and ROUT2

WM8983

### **SPEAKER BOOST MODE**

To support speaker boost mode, AVDD2 should be at least 1.5\*AVDD1. A higher AVDD2 will improve THD performance at the expense of power consumption while lower AVDD2 will cause clipping.

Variations in AVDD1 and AVDD2 should be taken into account when using speaker boost mode as shown in Figure 35 and Figure 36.



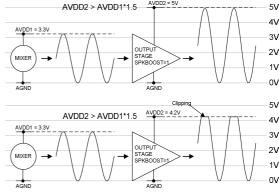


Figure 35 Non-Boost Mode Output Operation

Figure 36 Boost Mode Output Operation

LOUT2 and ROUT2 outputs can be connected directly to a Lithium battery to improve THD performance in non-boost mode. When using a 4.2V lithium battery maximum power output is achieved without using speaker boost and by setting ADVV1 = 3.6V.

Although direct battery connection is also possible in boost mode, the discharge characteristic of the battery can lead to clipping after a relatively short period of time as shown in Figure 37. Reducing the maximum permitted volume and keeping AVDD1 to a minimum will allow boost mode to operate for longer.

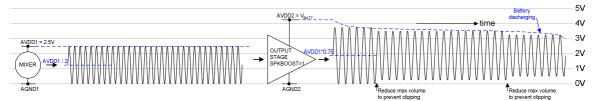


Figure 37 Output Boost Mode with Direct Battery Connection

As the full scale output falls close to AVDD1, it becomes more effective to use non-boost mode to generate a louder output, although SPKBOOST should NOT be changed while the speaker output is driving out a signal. As a general rule:

- if AVD-2 (AVDD1 \* 0.75) > AVDD1 / 2 boost mode provides more power output;
- if AVD-2 (AVDD1 \* 0.75) < AVDD1 / 2 non-boost mode provides more power output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R54	7	LOUT2ZC	0	LOUT2 volume zero cross enable:
LOUT2				1 = Change gain on zero cross only
Volume				0 = Change gain immediately
control	6	LOUT2MUTE	0	Left output mute:
				0 = Normal operation
				1 = Mute
	5:0	LOUT2VOL	111001	Left output volume:
				000000 = -57dB
				000001 = -56dB
				111001 = 0dB
				111111 = +6dB
	8	SPKVU	Not latched	LOUT2 and ROUT2 volumes do not
				update until a 1 is written to OUT2VU (in reg 54 or 55)
R55	7	ROUT2ZC	0	ROUT2 volume zero cross enable:
ROUT2 Volume	<b>'</b>	1001220	U	1 = Change gain on zero cross only
				0 = Change gain immediately
control	6	ROUT2MUTE	0	Right output mute:
		TOOTZINOTE		0 = Normal operation
				1 = Mute
	5:0	ROUT2VOL	111001	Right output volume:
				000000 = -57dB
				000001 = -56dB
				111001 = 0dB
				111111 = +6dB
	8	SPKVU	Not latched	LOUT2 and ROUT2 volumes do not
				update until a 1 is written to
				OUT2VU (in reg 54 or 55)

Table 42 OUT2 Volume Control

The signal output on LOUT2/ROUT2 comes from the Left/Right Mixer circuits and can be any combination of the DAC output, the Bypass path (output of the input boost stage) and the AUX input. The LOUT2/ROUT2 volume is controlled by the LOUT2VOL/ ROUT2VOL register bits. Gains over 0dB may cause clipping if the signal is large. The LOUT2MUTE/ ROUT2MUTE register bits cause the speaker outputs to be muted (the output DC level is driven out). The output pins remain at the same DC level (DCOP), so that no click noise is produced when muting or un-muting

The speaker output stages also have a selectable gain boost of 1.5x (3.52dB). When this boost is enabled the output DC level is also level shifted (from AVDD1/2 to 1.5xAVDD1/2) to prevent the signal from clipping. A dedicated amplifier BUFDCOP, as shown in Figure 34, is used to perform the DC level shift operation. This buffer must be enabled using the BUFDCOPEN register bit for this operating mode. It should also be noted that if AVDD2 is not equal to or greater than 1.5xAVDD1 this boost mode may result in signals clipping. Table 44 summarises the effect of the SPKBOOST control bits.



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49	2	SPKBOOST	0	0 = speaker gain = -1;
Output control				DC = AVDD1 / 2
				1 = speaker gain = +1.5;
				DC = 1.5 x AVDD1 / 2
R1 Power management 1	8	BUFDCOPEN	0	Dedicated buffer for DC level shifting output stages when in 1.5x gain boost configuration.  0 = Buffer disabled
				1 = Buffer enabled (required for 1.5x gain boost)

**Table 43 Speaker Boost Stage Control** 

SPKBOOST	OUTPUT STAGE GAIN	OUTPUT DC LEVEL	OUTPUT STAGE CONFIGURATION
0	1x (0dB)	AVDD1/2	Inverting
1	1.5x (3.52dB)	1.5xAVDD1/2	Non-inverting

**Table 44 Output Boost Stage Details** 

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43	5	MUTERPGA2INV	0	Mute input to INVROUT2 mixer
Beep control	4	INVROUT2	0	Invert ROUT2 output
	3:1	BEEPVOL	000	AUXR input to ROUT2 inverter gain
				000 = -15dB
				001 = -12dB
				010 = -9dB
				011 = -6dB
				100 = -3dB
				101 = 0dB
				110 = +3dB
				111 = +6dB
	0	BEEPEN	0	0 = mute AUXR beep input
				1 = enable AUXR beep input

Table 45 AUXR - ROUT2 BEEP Mixer Function

# **ZERO CROSS TIMEOUT**

A zero-cross timeout function is provided so that if zero cross is enabled on the input or output PGAs the gain will automatically update after a timeout period if a zero cross has not occurred. This is enabled by setting SLOWCLKEN. The timeout period is dependent on the clock input to the digital and is equal to  $2^{21}$  \* SYSCLK period.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7	0	SLOWCLKEN	0	Slow clock enable.
Additional				0 = slow clock disabled
Control				1 = slow clock enabled

**Table 46 Timeout Clock Enable Control** 

Note: SLOWCLKEN is also used for the jack insert detect debounce circuit



# **OUT3/OUT4 MIXERS AND OUTPUT STAGES**

The OUT3/OUT4 pins provide an additional stereo line output, a mono output, or a pseudo ground connection for headphones. There is a dedicated analogue mixer for OUT3 and one for OUT4 as shown in Figure 38.

The OUT3 and OUT4 output stages are powered from AVDD2 and AGND2. These individually-controllable outputs also incorporate an optional 1.5x boost and level shifting stage.

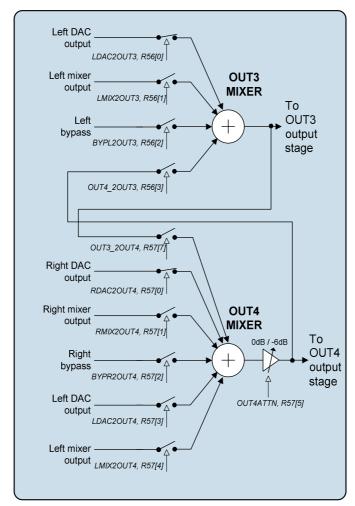


Figure 38 OUT3 and OUT4 Mixers

OUT3 can provide a midrail reference, a left line output, or a mono mix line output

OUT4 can provide a midrail reference, a right line output, or a mono mix line output.

A 6dB attenuation function is provided for OUT4, to prevent clipping during mixing of left and right signals. This function is enabled by the OUT4ATTN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R56 OUT3 mixer control	6	OUT3MUTE	0	0 = Output stage outputs OUT3 mixer 1 = Output stage muted – drives out VMID. Can be used as VMID reference in this mode.
	3	OUT4_2OUT3	0	OUT4 mixer output to OUT3 0 = disabled 1 = enabled
	2	BYPL2OUT3	0	Left ADC input to OUT3 0 = disabled 1 = enabled
	1	LMIX2OUT3	0	Left DAC mixer to OUT3 0 = disabled 1= enabled
	0	LDAC2OUT3	1	Left DAC output to OUT3 0 = disabled 1 = enabled
R57 OUT4 mixer control	7	OUT3_2OUT4	0	OUT3 mixer output to OUT4 0 = disabled 1= enabled
	6	OUT4MUTE	0	0 = Output stage outputs OUT4 mixer 1 = Output stage muted – drives out VMID. Can be used as VMID reference in this mode.
	5	OUT4ATTN	0	0 = OUT4 normal output 1 = OUT4 attenuated by 6dB
	4	LMIX2OUT4	0	Left DAC mixer to OUT4 0 = disabled 1 = enabled
	3	LDAC2OUT4	0	Left DAC to OUT4 0 = disabled 1 = enabled
	2	BYPR2OUT4	0	Right ADC input to OUT4  0 = disabled  1 = enabled
	1	RMIX2OUT4	0	Right DAC mixer to OUT4 0 = disabled 1 = enabled
	0	RDAC2OUT4	1	Right DAC output to OUT4 0 = disabled 1 = enabled

# Table 47 OUT3/OUT4 Mixer Registers

The OUT3 and OUT4 output stages each have a selectable gain boost of 1.5x (3.52dB). When this boost is enabled the output DC level is also level shifted (from AVDD1/2 to 1.5xAVDD1/2) to prevent the signal from clipping. A dedicated amplifier BUFDCOP, as shown in Figure 39, is used to perform the DC level shift operation. This buffer must be enabled using the BUFDCOPEN register bit for this operating mode. It should also be noted that if AVDD2 is not equal to or greater than 1.5xAVDD1 this boost mode may result in signals clipping. Table 44 summarises the effect of the OUT3BOOST and OUT4BOOST control bits.



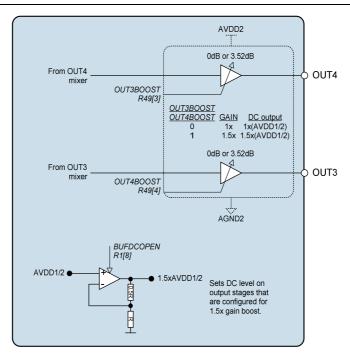


Figure 39 Outputs OUT3 and OUT4

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49	3	OUT3BOOST	0	0 = OUT3 output gain = -1;
Output control				DC = AVDD1 / 2
				1 = OUT3 output gain = +1.5
				DC = 1.5 x AVDD1 / 2
	4	OUT4BOOST	0	0 = OUT4 output gain = -1;
				DC = AVDD1 / 2
				1 = OUT4 output gain = +1.5
				DC = 1.5 x AVDD1 / 2
R1	8	BUFDCOPEN	0	Dedicated buffer for DC level shifting
Power management				output stages when in 1.5x gain boost configuration.
1				0=Buffer disabled
				1=Buffer enabled (required for 1.5x gain boost)

Table 48 OUT3 and OUT4 Boost Stages Control

OUT3BOOST/ OUT4BOOST	OUTPUT STAGE GAIN	OUTPUT DC LEVEL	OUTPUT STAGE CONFIGURATIO N
0	1x	AVDD1/2	Inverting
1	1.5x	1.5xAVDD1/2	Non-inverting

Table 49 OUT3 and OUT4 Output Boost Stage Details

## **OUTPUT PHASING**

The relative phases of the analogue outputs will depend upon the following factors:

- 1. DACLPOL and DACRPOL invert bits: Setting these bits to 1 will invert the DAC output.
- 2. Mixer configuration: The polarity of the signal will depend upon the route through the mixer path. For example, DACL can be directly input to the OUT3 mixer, giving a 180° phase shift at the OUT3 mixer output. However, if DACL is input to the OUT3 mixer via the left mixer, an additional phase shift will be introduced, giving 0° phase shift at the OUT3 mixer output.
- Output boost set-up: When 1.5x boost is enabled on an output, no phase shift occurs. When 1.5x boost is not enabled, a 180° phase shift occurs.

Figure 32 shows where these phase inversions can occur in the output signal path.

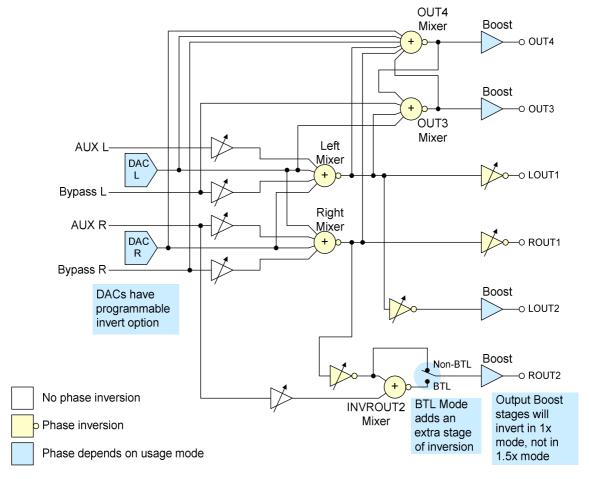


Figure 40 Output Signal Path Phasing

Table 50 shows the polarities of the outputs in various configurations.

Unless otherwise stated, polarity is shown with respect to left DAC output in non-inverting mode.

Note that only registers relating to the mixer paths are shown here (Mixer enables, volume settings, output enables etc are not shown).

CONFIGURATION	DACLPOL	DACRPOL	INVROUT2	SPKBOOST	оитзвоост	OUT4BOOST	MIXER PATH REGISTERS DIFFERENT FROM DEFAULT	OUT4 PHASE / MAG	OUT3 PHASE / N	LOUT1 PHASE/N	ROUT1 PHASE / N	LOUT2 PHASE / MAG	ROUT2 PHASE / MAG
		•		ä	TS	TS		/AG	:/MAG	/ MAG	:/MAG	1AG	1AG
Default: Stereo DAC playback	0	0	0	0	0	0		0°	0°	0°	0°	180°	180°
to LOUT1/ROUT1, LOUT2/ROUT2 and OUT4/OUT3								1	1	1	1	1	1
DACs inverted	1	1	0	0	0	0		180°	180°	180°	180°	0°	0°
								1	1	1	1	1	1
Stereo DAC playback	0	0	0	1	0	0		0°	0°	0°	0°	0°	0°
to LOUT1/ROUT1 and LOUT2/ROUT2 and OUT4/OUT3								1	1	1	1	1.5	1.5
(Speaker boost enabled)													
Stereo DAC playback to LOUT1/ROUT1 and LOUT2/ROUT2 and	0	0	0	0	1	1		180°	180°	0°	0°	180°	180°
OUT4/OUT3								1.5	1.5	1	1	1	1
(OUT3 and OUT4 boost enabled)													
Stereo playback to OUT3/OUT4 (DACs	0	0	0	0	0	0	LDAC2OUT3=0 RDAC2OUT4=0	180°	180°	0°	0°	180°	180°
input to OUT3/OUT4 mixers via left/right mixers)							LMIX2OUT3=1 RMIX2OUT4=1	1	1	1	1	1	1
Differential output of right bypass path via	0	0	0	0	0	0	BYPR2OUT4=1 OUT4_2OUT3=1	180°	0°	Х	Х	Х	Х
OUT3/OUT4 (Phase shown relative to right bypass)								1	1				
Differential output of mono mix of DACs via	0	0	1	0	0	0		0°	0°	0°	0°	180°	0°
LOUT2/ROUT2 (e.g. BTL speaker drive)								1	1	1	1	1	1
High power speaker drive	0	0	1	1	0	0		0°	0°	0°	0°	0°	180°
								1	1	1	1	1.5	1.5

Table 50 Relative Output Phases

Note that differential output should not be set up by combining outputs in boost mode with outputs which are not in boost mode as this would cause a DC offset current on the outputs.

## **ENABLING THE OUTPUTS**

Each analogue output of the WM8983 can be independently enabled or disabled. The analogue mixer associated with each output has a separate enable bit. All outputs are disabled by default. To save power, unused parts of the WM8983 should remain disabled.

Outputs can be enabled at any time, but it is not recommended to do so when BUFIO is disabled (BUFIOEN=0), as this may cause pop noise (see "Power Management" and "Applications Information" sections).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R1	2	BUFIOEN	0	Unused input/output bias buffer enable	
Power	6	OUT3MIXEN	0	OUT3 mixer enable	
Management	7	OUT4MIXEN	0	OUT4 mixer enable	
'	8	BUFDCOPEN	0	Output stage 1.5xAVDD/2 driver enable	
R2	8	ROUT1EN	0	ROUT1 output enable	
Power	7	LOUT1EN	0	LOUT1 output enable	
Management	6	SLEEP	0	0 = Normal device operation	
2				1 = Supply current reduced in device standby mode if clocks are still running	
R3	2	LMIXEN	0	Left mixer enable	
Power	3	RMIXEN	0	Right mixer enable	
Management 3	5	ROUT2EN	0	ROUT2 output enable	
3	6	LOUT2EN	0	LOUT2 output enable	
	7	OUT3EN	0	OUT3 enable	
	8	OUT4EN	0	OUT4 enable	
R42	1	DELEN	0	2 <sup>nd</sup> enable bit for L/ROUT1	
Output ctrl1	0	OUT1DEL	0	2 stage enable for L/ROUT1	
Note: All "Enable" bits are 1 = ON, 0 = OFF					

**Table 51 Output Stages Power Management Control** 

OUT1DEL and OUT2DEL enable lower pop noise power-up option. See start-up sequences. (in 2 stage enable method, normal enable bit is set, followed shortly later by the delayed enable DELEN)

## THERMAL SHUTDOWN

To protect the WM8983 from overheating a thermal shutdown circuit is included. If the device temperature reaches approximately 125°C and the thermal shutdown circuit is enabled (TSDEN=1) the L/ROUT2 amplifiers will be disabled. The thermal shutdown may also be configured to generate an interrupt. See the GPIO and Interrupt Controller section for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49	1	TSDEN	1	Thermal Shutdown Enable
Output Control				0 : thermal shutdown disabled
				1 : thermal shutdown enabled

**Table 52 Thermal Shutdown** 



## **UNUSED ANALOGUE INPUTS/OUTPUTS**

Whenever an analogue input/output is disabled, it remains connected to a voltage source (either AVDD1/2 or 1.5xAVDD1/2 as appropriate) through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between the voltage buffer and the output pins can be controlled using the VROI control bit. The default impedance is low, so that any capacitors on the outputs can charge up quickly at start-up. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about  $30k\Omega$ .

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49	0	VROI	0	VREF (AVDD1/2 or 1.5xAVDD/2) to analogue output resistance
				0: approx 1kΩ
				1: approx 30 kΩ

Table 53 Disabled Outputs to VREF Resistance

A dedicated buffer is available for biasing unused analogue I/O pins as shown in Figure 41. This buffer can be enabled using the BUFIOEN register bit.

If the SPKBOOST, OUT3BOOST or OUT4BOOST bits are set then the relevant outputs will be tied to the output of the DC level shift buffer at 1.5xAVDD/2 when disabled.

Figure 41 summarises the bias options for the output pins.

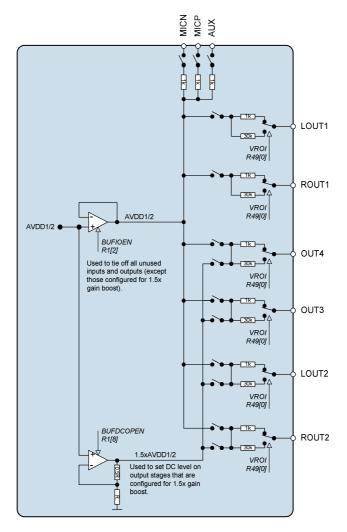


Figure 41 Unused Input/Output Pin Tie-off Buffers

L/ROUT2EN/ OUT3/4EN	OUT3BOOST/ OUT4BOOST/ SPKBOOST	VROI	OUTPUT CONFIGURATION
0	0	0	1kΩ tie-off to AVDD1/2
0	0	1	30kΩ tie-off to AVDD1/2
0	1	0	1kΩ tie-off to 1.5xAVDD1/2
0	1	1	30kΩ tie-off to 1.5xAVDD1/2
1	0	X	Output enabled (DC level=AVDD1/2)
1	1	Х	Output enabled (DC level=1.5xAVDD1/2)

**Table 54 Unused Output Pin Bias Options** 

# **DIGITAL AUDIO INTERFACES**

The audio interface has four pins:

ADCDAT: ADC data outputDACDAT: DAC data input

LRC: Data Left/Right alignment clock
 BCLK: Bit clock, for synchronisation

The clock signals BCLK, and LRC can be outputs when the WM8983 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Five different audio data formats are supported:

- · Left justified
- Right justified
- I<sup>2</sup>S
- DSP mode early
- DSP mode late

All of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

## **MASTER AND SLAVE MODE OPERATION**

The WM8983 audio interface may be configured as either master or slave. As a master interface device the WM8983 generates BCLK and LRC and thus controls sequencing of the data transfer on ADCDAT and DACDAT. To set the device to master mode register bit MS should be set high. In slave mode (MS=0), the WM8983 responds with data to clocks it receives over the digital audio interfaces.

## **AUDIO DATA FORMATS**

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRC transition.

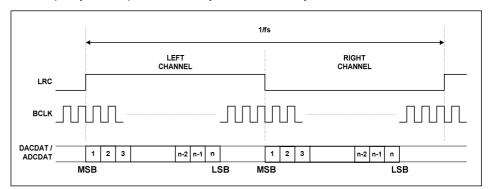


Figure 42 Left Justified Audio Interface (assuming n-bit word length)



In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRC transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRC transition.

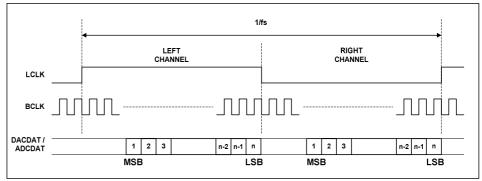


Figure 43 Right Justified Audio Interface (assuming n-bit word length)

In  $l^2S$  mode, the MSB is available on the second rising edge of BCLK following a LRC transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

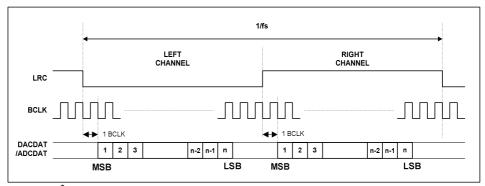


Figure 44 12S Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1<sup>st</sup> (mode B) or 2<sup>nd</sup> (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the LRC pulse shown in Figure 45 and Figure 46. In device slave mode, Figure 47 and Figure 48, it is possible to use any length of LRC pulse less than 1/fs, providing the falling edge of the LRC pulse occurs greater than one BCLK period before the rising edge of the next LRC pulse.

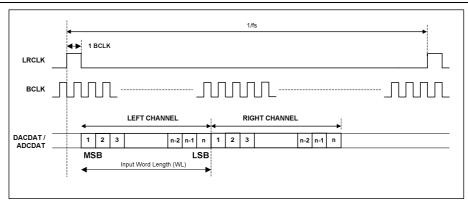


Figure 45 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

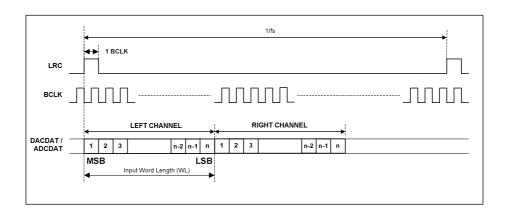


Figure 46 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

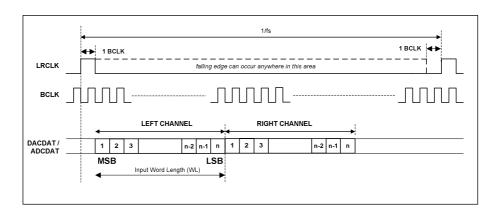


Figure 47 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

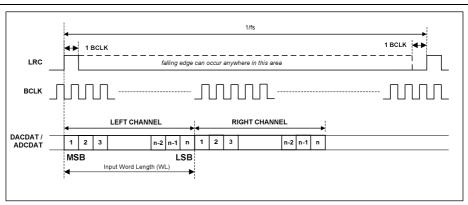


Figure 48 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 Audio	0	MONO	0	Selects between stereo and mono device operation:
Interface				0 = Stereo device operation
Control				1 = Mono device operation. Data appears in 'left' phase of LRC.
	1	ADCLRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of LRC clock:
				0=ADC left data appear in 'left' phase of LRC and right data in 'right' phase
				1=ADC left data appear in 'right ' phase of LRC and right data in 'left' phase
	2	DACLRSWAP	0	Controls whether DAC data appears in 'right' or 'left' phases of LRC clock:
				0=DAC left data appear in 'left' phase of LRC and right data in 'right' phase
				1=DAC left data appear in 'right' phase of LRC and right data in 'left' phase
	4:3	FMT	10	Audio interface Data Format Select:
				00=Right Justified
				01=Left Justified
				10=I <sup>2</sup> S format
				11= DSP/PCM mode
	6:5	WL	10	Word length
				00=16 bits
				01=20 bits
				10=24 bits
				11=32 bits (see note)
	7	LRP	0	LRC clock polarity
				0=normal
				1=inverted
	8	BCP	0	BCLK polarity
				0=normal
				1=inverted
R5	0	LOOPBACK	0	Digital loopback function
				0=No loopback
				1=Loopback enabled, ADC data output is fed directly into DAC data input.

**Table 55 Audio Interface Control** 

**Note:** Right Justified Mode will only operate with a maximum of 24 bits. If 32-bit mode is selected the device will operate in 24-bit mode.

## **AUDIO INTERFACE CONTROL**

The register bits controlling audio format, word length and master / slave mode are summarised below.

Register bit MS selects audio interface operation in master or slave mode. In Master mode BCLK and LRC are outputs. The frequencies of BCLK and LRC in master mode are controlled using MCLKDIV; these clocks are divided down versions of PLL output clock (SYSCLK). The MCLKDIV default setting provides a SYSCLK/256 division rate for the LRC output clock.

It is possible to divide down the BCLK rate using BCLKDIV; care must be taken in choosing the correct BCLKDIV rate to maintain sufficient BCLK pulses per LRC period for the chosen data word length. The BCLKDIV default setting provides a BCLK = SYSCLK clock.



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 Clock Generation Control	0	MS	0	Sets the chip to be master over LRC and BCLK  0=BCLK and LRC clock are inputs (Slave mode)
				1=BCLK and LRC clock are outputs generated by the WM8983 (Master mode)
	4:2	BCLKDIV	000	Configures the BCLK and LRC output frequency, for use when the chip is in Master mode.
				000=divide by 1 (BCLK=SYSCLK)
				001=divide by 2 (BCLK=SYSCLK/2)
				010=divide by 4
				011=divide by 8
				100=divide by 16
				101=divide by 32
				110=reserved
				111=reserved
	7:5	MCLKDIV	010	Sets the division for either the MCLK or PLL clock output (selected by CLKSEL)
				000=divide by 1
				001=divide by 1.5
				010=divide by 2 (LRC=SYSCLK/256)
				011=divide by 3
				100=divide by 4
				101=divide by 6
				110=divide by 8
				111=divide by 12
	8	CLKSEL	1	Controls the source of the clock for all internal operation:
				0=MCLK
				1=PLL output

# Table 56 Clock Control

The CKLSEL bit selects the internal source of the Master clock from the PLL (CLKSEL=1) or from MCLK (CLKSEL=0). When the internal clock is switched from one source to another using the CLKSEL bit, the clock originally selected must generate at least one falling edge after the CLKSEL has changed for the switching of clocks to be successful. For example the sequence for switching between the PLL and MCLK should be;

- 1. Change CLKSEL 1 -> 0
- 2. Wait for at least one falling edge from PLL generated clock
- 3. Disable the PLL (PLLEN=0)

# **AUDIO SAMPLE RATES**

The WM8983 filter characteristics for the ADCs and the DACs are set using the SR register bits; these bits do not change the rate of the audio interface output clocks in Master mode. The cut-offs for the digital filters and the ALC attack/decay times stated are determined using these values and assume a 256fs master clock rate.

If a sample rate is required which is not explicitly supported by the SR register settings, then the closest SR value to that sample rate should be chosen, the filter characteristics and the ALC attack, decay and hold times will scale appropriately.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 Additional Control	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters):  000 = 48kHz  001 = 32kHz  010 = 24kHz  011 = 16kHz  100 = 12kHz  101 = 8kHz  110-111 = reserved

**Table 57 Sample Rate Control** 

# MASTER CLOCK AND PHASE LOCKED LOOP (PLL)

The WM8983 has an on-chip phase-locked loop (PLL) circuit that can be used to:

Generate master clocks for the WM8983 audio functions from another external clock, e.g. in telecoms applications.

Generate and output (on pin CSB/GPIO1) a clock for another part of the system that is derived from an existing audio master clock.

Figure 49 shows the PLL and internal clocking on the WM8983.

The PLL can be enabled or disabled by the PLLEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1	5	PLLEN	0	PLL enable
Power				0 = PLL off
management 1				1 = PLL on

**Table 58 PLLEN Control Bit** 



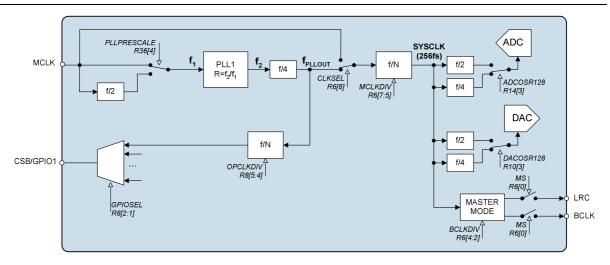


Figure 49 PLL and Clock Select Circuit

The PLL frequency ratio R =  $f_2/f_1$  (see Figure 49) can be set using the register bits PLLK and PLLN. R should be chosen to ensure 5 < PLLN < 13:

PLLN = int R PLLK = int  $(2^{24} (R-PLLN))$ 

## To calculate R:

There is a fixed divide by 4 in the PLL, f/4, and a selectable divide by N after the PLL, MCLKDIV.

- f<sub>2</sub> = SYSCLK x 4 x MCLKDIV
- R = f<sub>2</sub> / (MCLK / PRESCALE) = R
- PLLN = int R
- $k = int (2^{24} x (R intR)) convert k to hex for PLLK$

# **EXAMPLE:**

MCLK=26MHz, required clock = 12.288MHz.

R should be chosen to ensure 5 < PLLN < 13.

MCLKDIV = 2 sets the required division rate;

- $f_2 = 4 \times 2 \times 12.288MHz = 98.304MHz$ .
- R = 98.304 / (26/2) = 7.561846
- PLLN = int R = 7
- $k = int (2^{24} x (7.561846 7)) = 9426214_{dec}$

Convert k to hex:

PLLK = 8FD526h

Convert PLLK to R36, R37, R38 and R39 hex values:

R36 = 7h; R37 = 23h; R38 = 1EAh; R39 = 126h

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R36	4	PLLPRESCALE	0	0 = MCLK input not divided (default)
PLL N value				1 = Divide MCLK by 2 before input to PLL
	3:0	PLLN	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.
R37 PLL K value 1	5:0	PLLK [23:18]	0Ch	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).
R38 PLL K Value 2	8:0	PLLK [17:9]	093h	
R39 PLL K Value 3	8:0	PLLK [8:0]	0E9h	

Table 59 PLL Frequency Ratio Control

The PLL performs best when  $f_2$  is around 90MHz. Its stability peaks at N=8. Some example settings are shown in Table 60.

MCLK (MHz)	DESIRED OUTPUT	F2 (MHz)	PRESCALE	MCLKDIV	R	PLLN R36	K (Hex)	PLLK [23:18]	PLLK [17:9]	PLLK [8:0]
(F1)	(MHz)	(1411 12)	511152			(Hex)	(HCX)	R37 (Hex)	R38 (Hex)	R39 (Hex)
12	11.29	90.3168	1	2	7.5264	7	86C226	21	161	26
12	12.288	98.304	1	2	8.192	8	3126E8	С	93	E9
13	11.29	90.3168	1	2	6.947446	6	F28BD4	3C	145	1D4
13	12.288	98.304	1	2	7.561846	7	8FD525	23	1EA	126
14.4	11.29	90.3168	1	2	6.272	6	45A1CA	11	D0	1CA
14.4	12.288	98.304	1	2	6.826667	6	D3A06E	34	1D0	6D
19.2	11.29	90.3168	2	2	9.408	9	6872AF	1A	39	B0
19.2	12.288	98.304	2	2	10.24	Α	3D70A3	F	B8	A3
19.68	11.29	90.3168	2	2	9.178537	9	2DB492	В	DA	92
19.68	12.288	98.304	2	2	9.990243	9	FD809F	3F	C0	9F
19.8	11.29	90.3168	2	2	9.122909	9	1F76F7	7	1BB	F8
19.8	12.288	98.304	2	2	9.929697	9	EE009E	3B	100	9E
24	11.29	90.3168	2	2	7.5264	7	86C226	21	161	26
24	12.288	98.304	2	2	8.192	8	3126E8	С	93	E9
26	11.29	90.3168	2	2	6.947446	6	F28BD4	3C	145	1D4
26	12.288	98.304	2	2	7.561846	7	8FD525	23	1EA	126
27	11.29	90.3168	2	2	6.690133	6	BOAC93	2C	56	94
27	12.288	98.304	2	2	7.281778	7	482296	12	11	96

Table 60 PLL Frequency Examples for Common MCLK Rates

# **LOOPBACK**

Setting the LOOPBACK register bit enables digital loopback. When this bit is set the output data from the ADC audio interface is fed directly into the DAC data input.



# **COMPANDING**

The WM8983 supports A-law and  $\mu$ -law companding on both transmit (ADC) and receive (DAC) sides. Companding can be enabled on the DAC or ADC audio interfaces by writing the appropriate value to the DAC\_COMP or ADC\_COMP register bits respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5	2:1	ADC_COMP	0	ADC companding
Companding				00 = off
Control				01 = reserved
				10 = μ-law
				11 = A-law
	4:3	DAC_COMP	0	DAC companding
				00 = off
				01 = reserved
				10 = μ-law
				11 = A-law
	5	WL8	0	0 = off
				1 = device operates in 8-bit mode.

**Table 61 Companding Control** 

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

 $\mu$ -law (where  $\mu$ =255 for the U.S. and Japan):

$$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$$
  $-1 \le x \le 1$ 

law (where A=87.6 for Europe):

$$F(x) = A|x| / (1 + InA)$$
 } for  $x \le 1/A$ 

$$F(x) = (1 + InA|x|) / (1 + InA)$$
 } for  $1/A \le x \le 1$ 

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for  $\mu$ -law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits ( $\mu$ -law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

Setting the WL8 register bit allows the device to operate with 8-bit data. In this mode it is possible to use 8 BCLK's per LRC frame. When using DSP mode B, this allows 8-bit data words to be output consecutively every 8 BCLK's and can be used with 8-bit data words using the A-law and u-law companding functions.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 62 8-bit Companded Word Composition



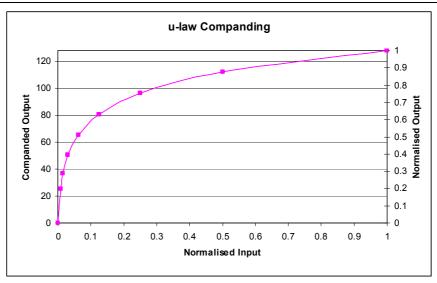


Figure 50 µ-Law Companding

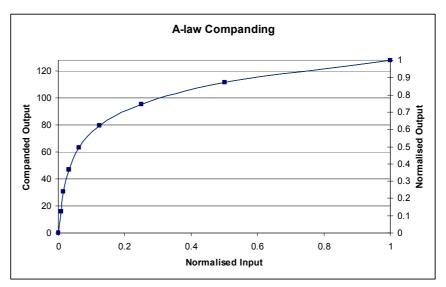


Figure 51 A-Law Companding

## **GENERAL PURPOSE INPUT/OUTPUT**

The WM8983 has three dual purpose input/output pins.

- CSB/GPIO1: CSB / GPIO1 pin
- L2/GPIO2: Left channel line input / headphone detection input
- R2/GPIO3: Right channel line input / headphone detection input

The GPIO2 and GPIO3 functions are provided for use as jack detection inputs.

The GPIO1 and GPIO2 functions are provided for use as jack detection inputs or general purpose outputs.

The default configuration for the CSB/GPIO1 is to be an input.

When setup as an input, the CSB/GPIO1 pin can either be used as CSB or for jack detection, depending on how the MODE pin is set.

Table 63 illustrates the functionality of the GPIO1 pin when used as a general purpose output.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8	2:0	GPIO1SEL	000	CSB/GPIO1 pin function select:
GPIO				000= input (CSB/jack detection:
Control				depending on MODE setting)
				001 = reserved
				010 = Temp ok
				011 = Amute active
				100 = PLL clk output
				101 = PLL lock
				110 = logic 0
				111 = logic 1
	3	GPIO1POL	0	GPIO1 Polarity invert
				0 = Non inverted
				1 = Inverted
	5:4	OPCLKDIV	00	PLL Output clock division ratio
				00 = divide by 1
				01 = divide by 2
				10 = divide by 3
				11 = divide by 4

### **Table 63 CSB/GPIO Control**

Note: If MODE is set to 3 wire mode, CSB/GPIO1 is used as CSB input irrespective of the GPIO1SEL[2:0] bits.

For further details of the jack detect operation see the OUTPUT SWITCHING section.

# **OUTPUT SWITCHING (JACK DETECT)**

When the device is operated using a 2-wire interface the CSB/GPIO1 pin can be used as a switch control input to automatically disable one set of outputs and enable another; the most common use for this functionality is as jack detect circuitry. The L2/GPIO2 and R2/GPIO3 pins can also be used for this purpose.

The GPIO pins have an internal de-bounce circuit when in this mode in order to prevent the output enables from toggling multiple times due to input glitches. This de-bounce circuit is clocked from a slow clock with period  $2^{21}$  x MCLK and is enabled by the SLOWCLKEN bit.

### Notes:

- 1. The SLOWCLKEN bit must be enabled for the jack detect circuitry to operate.
- The GPIOPOL bit is not relevant for jack detection, it is the signal detected at the pin which is used.



Switching on/off of the outputs is fully configurable by the user. Each output, OUT1, OUT2, OUT3 and OUT4 has 2 associated enables. OUT1\_EN\_0, OUT2\_EN\_0, OUT3\_EN\_0 and OUT4\_EN\_0 are the output enable signals which are used if the selected jack detection pin is at logic 0 (after debounce). OUT1\_EN\_1, OUT2\_EN\_1, OUT3\_EN\_1 and OUT4\_EN\_1 are the output enable signals which are used if the selected jack detection pin is at logic 1 (after de-bounce).

The jack detection enables operate as follows:

All OUT\_EN signals have an AND function performed with their normal enable signals (in Table 51). When an output is normally enabled at per Table 51, the selected jack detection enable (controlled by selected jack detection pin polarity) is set 0; it will turn the output off. If the normal enable signal is already OFF (0), the jack detection signal will have no effect due to the AND function.

During jack detection if the user desires an output to be un-changed whether the jack is in or not, both the JD\_EN settings, i.e. JD\_EN0 and JD\_EN1, should be set to 0000.

If jack detection is not enabled (JD\_EN=0), the output enables default to all 1's, allowing the outputs to be controlled as normal via the normal output enables found in Table 51.

REGISTER	BIT	LABEL	DEFAULT	DESCRIPTION
ADDRESS				
R9 (09h)	5:4	JD_SEL	00	Pin selected as jack detection input
GPIO control				00 = GPIO1
				01 = GPIO2
				10 = GPIO3
				11 = Reserved
	6	JD_EN	0	Jack Detection Enable
				0 = disabled
				1 = enabled
R13 (0Dh)	3:0	JD_EN0	0000	Output enables when selected jack
				detection input is logic 0.
				[0]= OUT1_EN_0
				[1]= OUT2_EN_0
				[2]= OUT3_EN_0
				[3]= OUT4_EN_0
	7:4	JD_EN1	0000	Output enables when selected jack
				detection input is logic 1
				[4]= OUT1_EN_1
				[5]= OUT2_EN_1
				[6]= OUT3_EN_1
				[7]= OUT4_EN_1

Table 64 Jack Detect Register Control Bits



## **CONTROL INTERFACE**

## **SELECTION OF CONTROL MODE AND 2-WIRE MODE ADDRESS**

The control interface can operate as either a 3-wire or 2-wire control interface. The MODE pin determines the 2 or 3 wire mode as shown in Table 65.

The WM8983 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are register address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 data bits in each control register.

MODE	INTERFACE FORMAT
Low	2 wire
High	3 wire

**Table 65 Control Interface Mode Selection** 

#### 3-WIRE SERIAL CONTROL MODE

In 3-wire mode, every rising edge of SCLK clocks in one data bit from the SDIN pin. A rising edge on CSB/GPIO latches in a complete control word consisting of the last 16 bits.

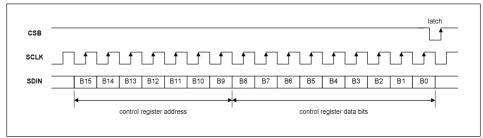


Figure 52 3-Wire Serial Control Interface

## 2-WIRE SERIAL CONTROL MODE

The WM8983 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit device address (this is not the same as the 7-bit address of each register in the WM8983).

The WM8983 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8983, the WM8983 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1' when operating in write only mode, the WM8983 returns to the idle condition and waits for a new start condition and valid address.

During a write, once the WM8983 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8983 register address plus the first bit of register data). The WM8983 then acknowledges the first data byte by driving SDIN low for one clock cycle. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8983 acknowledges again by pulling SDIN low.

Transfer is complete when there is a low to high transition on SDIN while SCLK is high. After a complete sequence the WM8983 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the control interface returns to the idle condition.

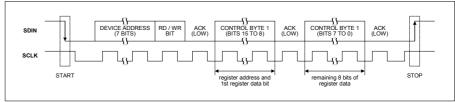


Figure 53 2-Wire Serial Control Interface

In 2-wire mode the WM8983 has a fixed device address, 0011010.



# **RESETTING THE CHIP**

The WM8983 can be reset by performing a write of any value to the software reset register (address 0h). This will cause all register values to be reset to their default values. In addition to this there is a Power-On Reset (POR) circuit which ensures that the registers are initially set to default when the device is powered up.

### **POWER SUPPLIES**

The WM8983 requires four separate power supplies:

AVDD1 and AGND1: Analogue supply, powers all internal analogue functions and output drivers LOUT1 and ROUT1. AVDD1 must be between 2.5V and 3.6V and has the most significant impact on overall power consumption (except for power consumed in the headphones). Higher AVDD1 will improve audio quality.

AVDD2 and AGND2: Output driver supplies, power LOUT2, ROUT2, OUT3 and OUT4. AVDD2 must be between 2.5V and 5.5V. AVDD2 can be tied to AVDD1, but it requires separate layout and decoupling capacitors to curb harmonic distortion.

DCVDD: Digital core supply, powers all digital functions except the audio and control interfaces. DCVDD must be between 1.71V and 3.6V, and has no effect on audio quality. The return path for DCVDD is DGND, which is shared with DBVDD.

DBVDD must be between 1.71V and 3.6V. DBVDD return path is through DGND.

It is possible to use the same supply voltage for all four supplies. However, digital and analogue supplies should be routed and decoupled separately on the PCB to keep digital switching noise out of the analogue signal paths.

### POWER MANAGEMENT

## SAVING POWER BY REDUCING OVERSAMPLING RATE

The default mode of operation of the ADC and DAC digital filters is in 64x oversampling mode. Under the control of ADCOSR128 and DACOSR128 the oversampling rate may be doubled. 64x oversampling results in a slight decrease in noise performance compared to 128x but lowers the power consumption of the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 DAC control	3	DACOSR128	0	DAC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)
R14 ADC control	3	ADCOSR128	0	ADC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)

Table 66 ADC and DAC Oversampling Rate Selection

# VMID

The analogue circuitry will not operate unless VMID is enabled. The impedance of the VMID resistor string, together with the decoupling capacitor on the VMID pin will determine the start-up time of the VMID circuit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1	1:0	VMIDSEL	00	Reference string impedance to VMID pin
Power				(Determines startup time):
management 1				00 = off (250kΩ VMID to AGND1)
				01 = 100kΩ
				10 = 500kΩ
				11 = 10kΩ total (for fast start-up)

**Table 67 VMID Impedance Control** 



# **BIASEN**

The analogue amplifiers will not operate unless BIASEN is enabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1	3	BIASEN	0	Analogue amplifier bias control
Power				0 = disabled
management 1				1 = enabled

Table 68 Analogue Bias Control

## **BIAS CONTROL**

Control of the analog bias values is possible using register 61 and 62

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R61 Bias control	8	BIASCUT	0	Global bias control 0 = normal
Bias Control				1 = 0.5x
	7:0		000 0000	Reserved

Table 69 Analogue Bias Control

Note that these bits must be used with care and may cause degradation in analog performance. For example, if both BIASCUT and HALFDACI are used at same time, the playback THD will be poor.



# **REGISTER MAP**

	DR 5:9]	REGISTER NAME	В8	В7	В6	В5	В4	В3	В2	В1	В0	DEF'T VAL
D E C	H E X											(HEX)
0	00	Software Reset		<u> </u>		S	oftware reset	t		<u> </u>		(
1	01	Power manage't 1	BUFDC OPEN	OUT4 MIXEN					000			
2	02	Power manage't 2	ROUT1 EN	LOUT1 EN	SLEEP	BOOST ENR	BOOST ENL	INPGA ENR	INPPGA ENL	ADC ENR	ADC ENL	000
3	03	Power manage't 3	OUT4EN	OUT3EN	LOUT2 EN	ROUT2 EN	0	RMIXEN	LMIXEN	DAC ENR	DAC ENL	000
4	04	Audio Interface	ВСР	LRP	WL[	[1:0]	FMT	[1:0]	DLR SWAP	ALR SWAP	MONO	050
5	05	Companding ctrl	0	0	0	WL8	DAC_C	OMP[1:0]	ADC_C0	OMP[1:0]	LOOP BACK	000
6	06	Clock Gen ctrl	CLKSEL	N	/CLKDIV[2:0	]		BCLKDIV[2:0	)]	0	MS	140
7	07	Additional ctrl	0	0	0	0	0		SR[2:0]		SLOWC LK EN	000
8	08	GPIO Control	0	0	0	OPCLK	DIV[1:0]	GPIO1P OL	(	GPIO1SEL[2:	0]	000
9	09	Jack detect control	0	0	JD_EN	JD_SI	EL[1:0]	0	0	0	0	000
10	0A	DAC Control	0	0	SOFT MUTE	0	0	DAC OSR128	AMUTE	DACR POL	DACL POL	000
11	0B	Left DAC digital Vol	DACVU		DACLVOL[7:0]						0FF	
12	0C	Right DAC dig'l Vol	DACVU				DACRV	/OL[7:0]				0FF
13	0D	Jack Detect Control	0		JD_EN	N1[3:0]			JD_EI	N0[3:0]		000
14	0E	ADC Control	HPFEN	HPFAPP	1	HPFCUT[2:0	]	ADC OSR128	0	ADCR POL	ADC LPOL	100
15	0F	Left ADC Digital Vol	ADCVU				ADCLV	OL[7:0]		•	1	0FF
16	10	Right ADC Digital Vol	ADCVU				ADCRV	/OL[7:0]				0FF
18	12	EQ1 – low shelf	EQ3D MODE	0	EQ10	C[1:0]			EQ1G[4:0]			12C
19	13	EQ2 – peak 1	EQ2BW	0	EQ20	C[1:0]			EQ2G[4:0]			02C
20	14	EQ3 – peak 2	EQ3BW	0	EQ30	C[1:0]			EQ3G[4:0]			02C
21	15	EQ4 – peak 3	EQ4BW	0	EQ40	C[1:0]			EQ4G[4:0]			02C
22	16	EQ5 – high shelf	0	0	EQ50	C[1:0]		1	EQ5G[4:0]			02C
24	18	DAC Limiter 1	LIMEN		LIMDO					ΓK[3:0]		032
25	19	DAC Limiter 2	0	0		LIMLVL[2:0]		<u> </u>	LIMBO	OST[3:0]		000
27	1B	Notch Filter 1	NFU	NFEN				NFA0[13:7]				000
28	1C	Notch Filter 2	NFU	0				NFA0[6:0]				000
29	1D	Notch Filter 3	NFU	0				NFA1[13:7]				000
30	1E	Notch Filter 4	NFU	0		1	AL CMANGO O	NFA1[6:0]		AL CAMPITO O	1	000
32	20	ALC control 1	ALC	SEL .	0		ALCMAX[2:0	'] 		ALCMIN[2:0]	l	038
33	21	ALC control 2  ALC control 3	0 ALC		ALCHL ALCDO					VL[3:0] TK[3:0]		00B 032
54		ALC COULDING	MODE		ALCDO	J 1 [J.U]			ALCA	1 K[J.U]		032



	DR 5:9]	REGISTER NAME	B8	В7	В6	B5	B4	B5 B4 B3		B1	В0	DEF'T VAL
D	Н											
E	E X											(HEX)
35	23	Noise Gate	0	0	0	0	0	NGEN		NGTH[2:0]		000
36	24	PLL N	0	0	0	0	PLLPRE	-	PLLI	N[3:0]		008
							SCALE					
37	25	PLL K 1	0	0	0			PLLK	[23:18]			00C
38	26	PLL K 2		PLLK[17:9]							093	
39	27	PLL K 3		PLLK[8:0]						0E9		
41	29	3D control		DEPTH3D[3:0]				1	000			
42	2A	OUT4 to ADC	OUT	1_2ADCVOL[	2:0]	OUT4_2 LNR	0	0	POB CTRL	DELEN	OUT1 DEL	
43	2B	Beep control	BYPL2 RMIX	BYPR2 LMIX	0	MUTER PGA2IN V	INVROUT2	E	BEEPVOL[2:	0]	BEEP EN	000
44	2C	Input ctrl	MBVSEL	0	R2_2	RIN2	RIP2	0	L2_2	LIN2	LIP2	033
					INPPGA	INPPGA	INPPGA		INPPGA	INPPGA	INPPGA	
45	2D	Left INP PGA gain ctrl	INPGAVU	INPPGA	INPPGA			INPPGA	VOLL[5:0]			010
	05	•	INDOM	ZCL	MUTEL			INDDOM	(OLD[E 0]			040
46	2E	Right INP PGA gain ctrl	INPGAVU	INPPGA ZCR	INPPGA MUTER			INPPGA	/OLR[5:0]			010
47	2F	Left ADC Boost	PGA	0		l 2BOOSTVOL	[2:0]	0	ΔΙΙΧ	L2BOOSTVO	ı [2·0]	100
"'		ctrl	BOOSTL	Ü		EDOOSTVOL	.[2.0]	Ů	7,07,1	LZDOOSTVO	-L[2.0]	100
48	30	Right ADC Boost	PGA	0	R2_:	2BOOSTVOL	[2:0]	0	AUXI	R2BOOSTVO	)L[2:0]	100
		ctrl	BOOSTR									
49	31	Output ctrl	0	0	DACL2	DACR2	OUT4	OUT3	SPK	TSDEN	VROI	002
					RMIX	LMIX	BOOST	BOOST	BOOST			
50	32	Left mixer ctrl	AUX	XLMIXVOL[2:	:0]	AUXL2	BY	PLMIXVOL[2	2:0]	BYPL2	DACL2	001
				/D. W. /	-1	LMIX	5)		1	LMIX	LMIX	
51	33	Right mixer ctrl	AUX	KRMIXVOL[2	:0]	AUXR2	BY	PRMIXVOL[	2:0]	BYPR2	DACR2	001
52	34	LOUT1 (HP)	OUT1VU	LOUT1	LOUT1	RMIX		LOUTI	VOL[5:0]	RMIX	RMIX	039
52	34	volume ctrl	OUTIVU	ZC	MUTE			LOUTT	VOL[3.0]			039
53	35	ROUT1 (HP)	OUT1VU	ROUT1	ROUT1			ROUT1	VOL[5:0]			039
		volume ctrl	001110	ZC	MUTE			110011	0.01			000
54	36	LOUT2 (SPK)	OUT2VU	LOUT2	LOUT2			LOUT2	VOL[5:0]			039
		volume ctrl		ZC	MUTE							
55	37	ROUT2 (SPK)	OUT2VU	ROUT2	ROUT2			ROUT2	VOL[5:0]			039
		volume ctrl		ZC	MUTE							
56	38	OUT3 mixer ctrl	0	0	OUT3	0	0	OUT4_	BYPL2	LMIX2	LDAC2	001
<u> </u>	<u> </u>				MUTE			2OUT3	OUT3	OUT3	OUT3	
57	39	OUT4 (MONO) mixer ctrl	0	OUT3_2 OUT4	OUT4	OUT4	LMIX2	LDAC2	BYPR2	RMIX2	RDAC2	001
	25			0014	MUTE	ATTN OUT4 OUT4 OUT4 OUT4 OUT4					000	
59	3B 3D	ALC Test Mode Bias Control	000 0000 ALCTST[1:0]					000				
61	งบ	DIG2 COULD	BIASCUT 0000 0000						000			

Table 70 WM8983 Register Map



# **REGISTER BITS BY ADDRESS**

# Notes:

1. Default values of N/A indicate non-latched data bits (e.g. software reset or volume update bits).

2. Register bits marked "s "Reser"ed" should not be changed from the default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO	
0 (00h)	[8:0]	RESET	N/A	Software reset	Resetting the Chip	
1 (01h)	8	BUFDCOPEN	0	Dedicated buffer for DC level shifting output stages when in 1.5x gain boost configuration.  0 = Buffer disabled  1 = Buffer enabled (required for 1.5x gain boost)	Analogue Outputs	
	7	OUT4MIXEN	0	OUT4 mixer enable 0=disabled 1=enabled	Power Management	
	6	OUT3MIXEN	0	OUT3 mixer enable 0=disabled 1=enabled	Power Management	
	5	PLLEN	0	PLL enable 0=PLL off 1=PLL on	Master Clock and Phase Locked Loop (PLL)	
	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON	Input Signal Path	
	3	BIASEN	0	Analogue amplifier bias control 0=disabled 1=enabled	Power Management	
	2	BUFIOEN	0	Unused input/output tie off buffer enable 0=disabled 1=enabled	Power Management	
	1:0	VMIDSEL	00	Reference string impedance to VMID pin (Determines startup time): $00 = \text{off } (250 \text{k}\Omega \text{ VMID to AGND1})$ $01 = 100 \text{k}\Omega$ $10 = 500 \text{k}\Omega$ $11 = 10 \text{k}\Omega \text{ total (for fast start-up)}$	Power Management	
2 (02h)	8	ROUT1EN	0	ROUT1 output enable 0=disabled 1=enabled	Power Management	
	7	LOUT1EN	0	LOUT1 output enable 0=disabled 1=enabled	Power Management	
	6	SLEEP	0	0 = normal device operation 1 = residual current reduced in device standby mode	Power Management	
	5	BOOSTENR	0	Right channel Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON	Power Management	
	4	BOOSTENL	0	Left channel Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON	Power Management	



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	INPPGAENR	0	Right channel input PGA enable 0 = disabled 1 = enabled	Power Management
	2 INPPGAENL 0		0	Left channel input PGA enable 0 = disabled 1 = enabled	Power Management
	1	ADCENR	0	Enable ADC right channel:  0 = ADC disabled  1 = ADC enabled	Analogue to Digital Converter (ADC)
	0	ADCENL	0	Enable ADC left channel:  0 = ADC disabled  1 = ADC enabled	Analogue to Digital Converter (ADC)
R3 (03h)	8	OUT4EN	0	OUT4 enable 0 = disabled 1 = enabled	Power Management
	7	OUT3EN	0	OUT3 enable 0 = disabled 1 = enabled	Power Management
	6	LOUT2EN	0	LOUT2 enable 0 = disabled 1 = enabled	Power Management
	5	ROUT2EN	0	ROUT2 enable 0 = disabled 1 = enabled	Power Management
	4		0	Reserved	Analogue Outputs
	3	RMIXEN	0	Right output channel mixer enable: 0 = disabled 1 = enabled	Analogue Outputs
	2	LMIXEN	0	Left output channel mixer enable: 0 = disabled 1 = enabled	Analogue Outputs
	1	DACENR	0	Right channel DAC enable 0 = DAC disabled 1 = DAC enabled	Analogue Outputs
	0	DACENL	0	Left channel DAC enable 0 = DAC disabled 1 = DAC enabled	Analogue Outputs
4 (04h)	8	BCP	0	BCLK polarity 0=normal 1=inverted	Digital Audio Interfaces
	7	LRP	0	LRC clock polarity 0=normal 1=inverted	Digital Audio Interfaces
	6:5	WL	10	Word length 00=16 bits 01=20 bits 10=24 bits 11=32 bits	Digital Audio Interfaces



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:3	FMT	10	Audio interface Data Format Select:  00=Right Justified  01=Left Justified  10=i <sup>2</sup> S format  11= DSP/PCM mode	Digital Audio Interfaces
	2	DLRSWAP	0	Controls whether DAC data appears in 'right' or 'left' phases of LRC clock: 0=DAC data appear in 'left' phase of LRC 1=DAC data appears in 'right' phase of LRC	Digital Audio Interfaces
	1	ALRSWAP	0	Controls whether ADC data appears in 'right' or 'left' phases of LRC clock:  0=ADC data appear in 'left' phase of LRC  1=ADC data appears in 'right' phase of LRC	Digital Audio Interfaces
	0	MONO	0	Selects between stereo and mono device operation: 0=Stereo device operation 1=Mono device operation. Data appears in 'left' phase of LRC	Digital Audio Interfaces
5 (05h)	8:6		000	Reserved	
	5	WL8	0	Companding Control 8-bit mode 0=off 1=device operates in 8-bit mode	Digital Audio Interfaces
	4:3	DAC_COMP	00	DAC companding 00=off (linear mode) 01=reserved 10=µ-law 11=A-law	Digital Audio Interfaces
	2:1	ADC_COMP	00	ADC companding 00=off (linear mode) 01=reserved 10=µ-law 11=A-law	Digital Audio Interfaces
	0	LOOPBACK	0	Digital loopback function 0=No loopback 1=Loopback enabled, ADC data output is fed directly into DAC data input.	Digital Audio Interfaces
6 (06h)	8	CLKSEL	1	Controls the source of the clock for all internal operation: 0=MCLK 1=PLL output	Digital Audio Interfaces
	7:5	MCLKDIV	010	Sets the scaling for either the MCLK or PLL clock output (under control of CLKSEL)  000=divide by 1  001=divide by 1.5  010=divide by 2  011=divide by 3  100=divide by 4  101=divide by 6  110=divide by 8  111=divide by 12	Digital Audio Interfaces



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:2	BCLKDIV	000	Configures the BCLK output frequency, for use when the chip is master over BCLK.  000=divide by 1 (BCLK=MCLK)  001=divide by 2 (BCLK=MCLK/2)  010=divide by 4  011=divide by 8  100=divide by 16  101=divide by 32  110=reserved  111=reserved	Digital Audio Interfaces
	1		0	Reserved	
	0	MS	0	Sets the chip to be master over LRC and BCLK 0=BCLK and LRC clock are inputs 1=BCLK and LRC clock are outputs generated by the WM8978 (MASTER)	Digital Audio Interfaces
7 (07h)	3:1	SR	000	Approximate sample rate (configures the coefficients for the internal digital filters):  000=48kHz 001=32kHz 010=24kHz 011=16kHz 100=12kHz 101=8kHz 110-111=reserved	Audio Sample Rates
	0	SLOWCLKEN	0	Slow clock enable. Used for both the jack insert detect debounce circuit and the zero cross timeout.  0 = slow clock disabled  1 = slow clock enabled	Analogue Outputs
8 (08h)	5:4	OPCLKDIV	00	PLL Output clock division ratio 00=divide by 1 01=divide by 2 10=divide by 3 11=divide by 4	General Purpose Input/Output (GPIO)
	3	GPIO1POL	0	GPIO1 Polarity invert 0=Non inverted 1=Inverted	General Purpose Input/Output (GPIO)
	2:0	GPIO1SEL [2:0]	000	CSB/GPIO1 pin function select:  000= input (CSB/jack detection: depending on MODE setting)  001= reserved  010=Temp ok  011=Amute active  100=PLL clk o/p  101=PLL lock  110=logic 0  111=logic 1	General Purpose Input/Output (GPIO)



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
9 (09h)	8:7		00	Reserved	
	6	JD_EN	0	Jack Detection Enable 0=disabled 1=enabled	Output Switching (Jack Detect)
	5:4	JD_SEL	00	Pin selected as jack detection input  00 = GPIO1  01 = GPIO2  10 = GPIO3  11 = Reserved	Output Switching (Jack Detect)
	3:0		0	Reserved	Output Switching (Jack Detect)
10 (0Ah)	8:7		00	Reserved	
	6 SOFTMUTE 0 Softmute enable: 0=Disabled			Output Signal Path	
	5:4		00	Reserved	
	3	DACOSR128	0	DAC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)	Power Management
	2	AMUTE	0	Automute enable 0 = Amute disabled 1 = Amute enabled	Output Signal Path
	1	DACPOLR	0	Right DAC output polarity: 0 = non-inverted 1 = inverted (180 degrees phase shift)	Output Signal Path
	0	DACPOLL	0	Left DAC output polarity: 0 = non-inverted 1 = inverted (180 degrees phase shift)	Output Signal Path
11 (0Bh)	8	DACVU	N/A	DAC left and DAC right volume do not update until a 1 is written to DACVU (in reg 11 or 12)	Digital to Analogue Converter (DAC)
	7:0	DACVOLL	11111111	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB 0.5dB steps up to 1111 1111 = 0dB	Digital to Analogue Converter (DAC)
12 (0Ch)	8	DACVU	N/A	DAC left and DAC right volume do not update until a 1 is written to DACVU (in reg 11 or 12)	Output Signal Path
	7:0	DACVOLR	11111111	Right DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
13 (0Dh)	8		0	Reserved	
	7:4	JD_EN1	0000	Output enabled when selected jack detection input is logic 1  [4]= OUT1_EN_1  [5]= OUT2_EN_1  [6]= OUT3_EN_1  [7]= OUT4_EN_1	Output Switching (Jack Detect)
	3:0	JD_EN0	0000	Output enabled when selected jack detection input is logic 0.  [0]= OUT1_EN_0  [1]= OUT2_EN_0  [2]= OUT3_EN_0  [3]= OUT4_EN_0	Output Switching (Jack Detect)
14 (0Eh)	8	HPFEN	1	High Pass Filter Enable 0=disabled 1=enabled	Analogue to Digital Converter (ADC)
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1 <sup>st</sup> order, fc = ~3.7Hz) 1=Application mode (2 <sup>nd</sup> order, fc = HPFCUT)	Analogue to Digital Converter (ADC)
	6:4	HPFCUT	000	Application mode cut-off frequency See table 14 for details	Analogue to Digital Converter (ADC)
	3	ADCOSR 128	0	ADC oversample rate select 0 = 64x (lowest power) 1 = 128x (best SNR)	Power Management
	2		0	Reserved	
	1	ADCRPOL	0	ADC right channel polarity adjust: 0=normal 1=inverted	Analogue to Digital Converter (ADC)
	0	ADCLPOL	0	ADC left channel polarity adjust: 0=normal 1=inverted	Analogue to Digital Converter (ADC)
15 (0Fh)	8	ADCVU	N/A	ADC left and ADC right volume do not update until a 1 is written to ADCVU (in reg 16 or 17)	Analogue to Digital Converter (ADC)
	7:0	ADCVOLL	11111111	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB 0.5dB steps up to 1111 1111 = 0dB	Analogue to Digital Converter (ADC)
16 (10h)	8	ADCVU	N/A	ADC left and ADC right volume do not update until a 1 is written to ADCVU (in reg 16 or 17)	Analogue to Digital Converter (ADC)
	7:0	ADCVOLR	11111111	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB 0.5dB steps up to 1111 1111 = 0dB	Analogue to Digital Converter (ADC)



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
18 (12h)	8	EQ3DMODE	1	0 = Equaliser and 3D Enhancement applied to ADC path 1 = Equaliser and 3D Enhancement applied to DAC path	Output Signal Path
	7		0	Reserved	
	6:5	EQ1C		EQ Band 1 Cut-off Frequency: 00=80Hz 01=105Hz 10=135Hz 11=175Hz	Output Signal Path
	4:0	EQ1G	01100	EQ Band 1 Gain Control. See Table 38 for details.	Output Signal Path
19 (13h)	8	EQ2BW	0	EQ Band 2 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth	Output Signal Path
	7		0	Reserved	Output Signal Path
	6:5	EQ2C	01	EQ Band 2 Centre Frequency: 00=230Hz 01=300Hz 10=385Hz 11=500Hz	Output Signal Path
	4:0	EQ2G	01100	EQ Band 2 Gain Control. See Table 38 for details.	Output Signal Path
20 (14h)	8	EQ3BW	0	EQ Band 3 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth	Output Signal Path
	7		0	Reserved	Output Signal Path
	6:5	EQ3C	01	EQ Band 3 Centre Frequency: 00=650Hz 01=850Hz 10=1.1kHz 11=1.4kHz	Output Signal Path
	4:0	EQ3G	01100	EQ Band 3 Gain Control. See Table 38 for details.	Output Signal Path
21 (15h)	8	EQ4BW	0	EQ Band 4 Bandwidth Control 0=narrow bandwidth 1=wide bandwidth	Output Signal Path
	7		0	Reserved	Output Signal Path
	6:5	EQ4C	01	EQ Band 4 Centre Frequency: 00=1.8kHz 01=2.4kHz 10=3.2kHz 11=4.1kHz	Output Signal Path
	4:0	EQ4G	01100	EQ Band 4 Gain Control. See Table 38 for details.	Output Signal Path
22 (16h)	8:7		0	Reserved	Output Signal Path
	6:5	EQ5C	01	EQ Band 5 Cut-off Frequency: 00=5.3kHz 01=6.9kHz 10=9kHz 11=11.7kHz	Output Signal Path
	4:0	EQ5G	01100	EQ Band 5 Gain Control. See Table 38 for details.	Output Signal Path



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
24 (18h)	8	LIMEN	0	Enable the DAC digital limiter: 0=disabled 1=enabled	Output Signal Path
	7:4	LIMDCY	0011	DAC Limiter Decay time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate: 0000=750us 0001=1.5ms 0010=3ms 0011=6ms 0100=12ms 0101=24ms 0110=48ms 0111=96ms 1000=192ms 1001=384ms 1010=768ms	Output Signal Path
	3:0	LIMATK	0010	DAC Limiter Attack time (per 6dB gain change) for 44.1kHz sampling. Note that these will scale with sample rate.  0000=94us 0001=188s 0010=375us 0011=750us 0110=750us 0100=1.5ms 0101=3ms 0110=6ms 0111=12ms 1000=24ms 1001=48ms 1010=96ms 1011 to 1111=192ms	Output Signal Path
25 (19h)	8:7 6:4	LIMLVL	00	Reserved Programmable signal threshold level	Output Signal
				(determines level at which the DAC limiter starts to operate) 000=-1dB 001=-2dB 010=-3dB 011=-4dB 100=-5dB 101 to 111=-6dB	Path
	3:0	LIMBOOST	0000	DAC Limiter volume boost (can be used as a stand alone volume boost when LIMEN=0): 0000=0dB 0001=+1dB 0010=+2dB (1dB steps) 1011=+11dB 1100=+12dB 1101 to 1111=reserved	Output Signal Path
27 (1Bh)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7	NFEN	0	Notch filter enable: 0=Disabled 1=Enabled	Analogue to Digital Converter (ADC)
	6:0	NFA0[13:7]	0000000	Notch Filter $a_0$ coefficient, bits [13:7]	Analogue to Digital Converter (ADC)



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
28 (1Ch)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7		0	Reserved	
	6:0	NFA0[6:0]	0000000	Notch Filter a <sub>0</sub> coefficient, bits [6:0]	Analogue to Digital Converter (ADC)
29 (1Dh)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7		0	Reserved	
	6:0	NFA1[13:7]	0000000	Notch Filter a <sub>1</sub> coefficient, bits [13:7]	Analogue to Digital Converter (ADC)
30 (1Eh)	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.	Analogue to Digital Converter (ADC)
	7		0	Reserved	
	6:0	NFA1[6:0]	0000000	Notch Filter a <sub>1</sub> coefficient, bits [6:0]	Analogue to Digital Converter (ADC)
32 (20h)	8:7	ALCSEL	00	ALC function select:  00=ALC off  01=ALC right only  10=ALC left only  11=ALC both on	Input Limiter/ Automatic Level Control (ALC)
	6		0	Reserved	
	5:3	ALCMAXGAIN	111	Set Maximum Gain of PGA  111=+35.25dB  110=+29.25dB  101=+23.25dB  100=+17.25dB  011=+11.25dB  010=+5.25dB  001=-0.75dB  000=-6.75dB	Input Limiter/ Automatic Level Control (ALC)
	2:0	ALCMINGAIN	000	Set minimum gain of PGA 000=-12dB 001=-6dB 010=0dB 011=+6dB 100=+12dB 101=+18dB 110=+24dB 111=+30dB	Input Limiter/ Automatic Level Control (ALC)
33 (21h)	7:4	ALCHLD	0000	ALC hold time before gain is increased.  0000 = 0ms  0001 = 2.67ms  0010 = 5.33ms  (time doubles with every step)  1111 = 43.691s	Input Limiter/ Automatic Level Control (ALC)



REGISTER ADDRESS	BIT	LABEL	DEFAULT		DE	SCRIPTION		REFER TO
	3:0	ALCLVL	1011	ALC target – sets signal level at ADC input 1111: -1.5dBFS 1110: -1.5dBFS 1101: -3dBFS 1100: -4.5dBFS (-1.5dB steps) 0001: -21dBFS 0000: -22.5dBFS				Input Limiter/ Automatic Level Control (ALC)
34 (22h)	8	ALCMODE	0	Determii 0=ALC r 1=Limite		Input Limiter/ Automatic Level Control (ALC)		
	7:4	ALCDCY [3:0]	0011		gain ramp-u <sub>l</sub> DE ==0)	p) time		Input Limiter/ Automatic
					Per step	Per 6dB	90% of range	Level Control
				0000	410us	3.3ms	24ms	(ALC)
				0001	820us	6.6ms	48ms	]
				0010	1.64ms	13.1ms	192ms	]
				(time	doubles with	h every step)		
				1010 or higher	420ms	3.36s	24.576s	
			0011		l nain ramn₌u	n) time		-
			0011		Decay (gain ramp-up) time (ALCMODE ==1)		1	
					Per step	Per 6dB	90% of range	
				0000	90.8us	726.4us	5.26ms	
				0001	181.6us	1.453ms	10.53ms	
				0010	363.2us	2.905ms	21.06ms	
						h every step)		
				1010	93ms	744ms	5.39s	
	3:0	ALCATK	0010			np-down) tim	ie	Input Limiter/ Automatic
				(ALCMC	DE == 0)	D 0 ID	000/ 6	Level Control
					Per step	Per 6dB	90% of range	(ALC)
				0000	104us	832us	6ms	-
				0001	208us	1.664ms	12ms	-
				0010	416us	3.328ms	24.1ms	
				(time	l	h every step) 852ms		-
				or	106ms	0021118	6.18s	
			0010	higher	ack (gain ron	⊥ np-down) tim		
			0010		DE == 1)		T	
					Per step	Per 6dB	90% of range	
			1	0000	22.7us	182.4us	1.31ms	]
			1	0001	45.4us	363.2us	2.62ms	
				0010	90.8us	726.4us	5.26ms	]
			1			h every step)		
			1	1010	23.2ms	186ms	1.348s	
35 (23h)	8:4		00000	Reserve				
	3	NGEN	0		-	ction enable		Input Limiter/
				1 = enat				Automatic Level Control
				0 = disal	ble			(ALC)



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	NGTH	000	ALC Noise gate threshold: 000=-39dB 001=-45dB 010=-51db (6dB steps) 111=-81dB	Input Limiter/ Automatic Level Control (ALC)
36 (24h)	8:5		0000	Reserved	
	4	PLL PRESCALE	0	0 = MCLK input not divided (default) 1 = Divide MCLK by 2 before input to PLL	Master Clock and Phase Locked Loop (PLL)
	3:0	PLLN[3:0]	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.	Master Clock and Phase Locked Loop (PLL)
37 (25h)	8:6		000	Reserved	
	5:0	PLLK[23:18]	01100	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
38 (26h)	8:0	PLLK[17:9]	010010011	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
39 (27h)	8:0	PLLK[8:0]	011101001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Master Clock and Phase Locked Loop (PLL)
41 (29h)	8:4		00000	Reserved	
	3:0	DEPTH3D	0000	Stereo depth 0000: 0% (minimum 3D effect) 0001: 6.67% 1110: 93.3% 1111: 100% (maximum 3D effect)	3D Stereo Enhancement
42 (2Ah)	8:6	OUT4_2ADCVOL	000	Controls the OUT4 to ADC input boost stage:  000 = Path disabled (disconnected)  001 = -12dB gain  010 = -9dB gain  011 = -6dB gain  100 = -3dB gain  101 = +0dB gain  111 = +6dB gain	Analogue Outputs
	5	OUT4_2LNR	0	OUT4 to L or R ADC input 0 = Right ADC input 1 = Left ADC input	Analogue Outputs
43 (2Bh)	8	BYPL2RMIX	0	Left bypass path (from the Left channel input PGA stage) to right output mixer 0 = not selected 1 = selected	Analogue Outputs
	7	BYPR2LMIX	0	Right bypass path (from the right channel input PGA stage) to Left output mixer 0 = not selected 1 = selected	Analogue Outputs
	6		0	Reserved	Analogue Outputs



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	MUTERPGA2INV	0	Mute input to INVROUT2 mixer	Analogue Outputs
	4	INVROUT2	0	Mute input to INVROUT2 mixer	Analogue Outputs
	3:1	BEEPVOL	000	AUXR input to ROUT2 inverter gain 000 = -15dB	Analogue Outputs
	0	BEEPEN	0	111 = +6dB  0 = mute AUXR beep input  1 = enable AUXR beep input	Analogue Outputs
44 (2Ch)	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD	Input Signal Path
	7		0	Reserved	
	6	R2_2INPPGA	0	Connect R2 pin to right channel input PGA positive terminal.	Input Signal Path
				0=R2 not connected to input PGA 1=R2 connected to input PGA amplifier positive terminal (constant input impedance).	
	5	RIN2INPPGA	1	Connect RIN pin to right channel input PGA negative terminal.	Input Signal Path
				0=RIN not connected to input PGA 1=RIN connected to right channel input PGA amplifier negative terminal.	
	4 RIP2INPPGA 1 Connect RIP pin amplifier positive 0 = RIP not connect 1 = right channel		Connect RIP pin to right channel input PGA amplifier positive terminal.  0 = RIP not connected to input PGA  1 = right channel input PGA amplifier positive terminal connected to RIP (constant input	Input Signal Path	
				impedance)	
	3		0	Reserved	
	2 L2_2INPPGA 0 Connect L2 pin to left channel input PGA positive terminal. 0=L2 not connected to input PGA		positive terminal.	Input Signal Path	
				terminal (constant input impedance).	
	1	LIN2INPPGA	1	Connect LIN pin to left channel input PGA negative terminal.  0=LIN not connected to input PGA  1=LIN connected to input PGA amplifier negative	Input Signal Path
				terminal.	
	0	LIP2INPPGA	1	Connect LIP pin to left channel input PGA amplifier positive terminal.	Input Signal Path
				0 = LIP not connected to input PGA 1 = input PGA amplifier positive terminal connected to LIP (constant input impedance)	
45 (2Dh)	8	INPPGAU	N/A	INPPGAVOLL and INPPGAVOLR volume do not update until a 1 is written to INPPGAUPDATE (in reg 45 or 46)	Input Signal Path
	7	INPPGAZCL	0	Left channel input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1 <sup>st</sup> zero cross after gain register write.	Input Signal Path
	6	INPPGAMUTEL	0	Mute control for left channel input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).	Input Signal Path



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5:0	INPPGAVOLL	010000	Left channel input PGA volume 000000 = -12dB 000001 = -11.25db	Input Signal Path
				010000 = 0dB 111111 = 35.25dB	
46 (2Eh)	8	INPPGAU	N/A	INPPGAVOLL and INPPGAVOLR volume do not update until a 1 is written to INPPGAUPDATE (in reg 45 or 46)	Input Signal Path
	7	INPPGAZCR	0	Right channel input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1 <sup>st</sup> zero cross after gain register write.	Input Signal Path
	6	INPPGAMUTER	0	Mute control for right channel input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).	Input Signal Path
	5:0	INPPGAVOLR	010000	Right channel input PGA volume 000000 = -12dB 000001 = -11.25db	Input Signal Path
				010000 = 0dB 111111 = +35.25dB	
47 (2Fh)	8	PGABOOSTL	1	Boost enable for left channel input PGA:  0 = PGA output has +0dB gain through input BOOST stage.  1 = PGA output has +20dB gain through input BOOST stage.	Input Signal Path
-	7		0	Reserved	
	6:4	L2_2BOOSTVOL	000	Controls the L2 pin to the left channel input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage	Input Signal Path
_				111=+6dB gain through boost stage	
	3		0	Reserved	
	2:0	AUXL2BOOSTVOL	000	Controls the auxilliary amplifer to the left channel input boost stage:  000=Path disabled (disconnected)  001=-12dB gain through boost stage  010=-9dB gain through boost stage   111=+6dB gain through boost stage	Input Signal Path
48 (30h)	8	PGABOOSTR	1	Boost enable for right channel input PGA:  0 = PGA output has +0dB gain through input BOOST stage.  1 = PGA output has +20dB gain through input BOOST stage.	Input Signal Path
	7		0	Reserved	



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	R2_2BOOSTVOL	000	Controls the R2 pin to the right channel input boost stage:  000=Path disabled (disconnected)	Input Signal Path
				001=-12dB gain through boost stage 010=-9dB gain through boost stage	
	3		0	111=+6dB gain through boost stage  Reserved	
	2:0	AUXR2BOOSTVOL	000	Controls the auxilliary amplifer to the right	Input Signal
				channel input boost stage: 000=Path disabled (disconnected)	Path
				001=-12dB gain through boost stage 010=-9dB gain through boost stage	
				 111=+6dB gain through boost stage	
49 (31h)	8:7		00	Reserved	
	6	DACL2RMIX	0	Left DAC output to right output mixer  0 = not selected  1 = selected	Analogue Outputs
	5	DACR2LMIX	0	Right DAC output to left output mixer 0 = not selected	Analogue Outputs
	3	OUT3BOOST	1 = selected  Output 3 Gain 0 = OUT3 output gain = -1; DC = AVDD1 / 2 1 = OUT3 output gain = +1.5		Analogue Outputs
	DC = 1.5 x AVDD1 / 2  4 OUT4BOOST 0 Output 4 Gain 0 = OUT4 output gain = -1; DC = AVDD1 / 2 1 = OUT4 output gain = +1.5		Output 4 Gain 0 = OUT4 output gain = -1; DC = AVDD1 / 2	Analogue Outputs	
	2	SPKBOOST	0	Speaker Gain 0 = speaker gain = -1; DC = AVDD1 / 2 1 = speaker gain = +1.5; DC = 1.5 x AVDD1 / 2	Analogue Outputs
	1	TSDEN	1	Thermal Shutdown Enable 0 : thermal shutdown disabled 1 : thermal shutdown enabled	Analogue Outputs
	0	VROI	0	VREF (AVDD/2 or 1.5xAVDD/2) to analogue output resistance 0: approx 1kΩ 1: approx 30 kΩ	Analogue Outputs
50 (32h)	8:6	AUXLMIXVOL	000	Aux left channel input to left mixer volume control:  000 = -15dB  001 = -12dB   101 = 0dB  110 = +3dB	Analogue Outputs
	5	AUXL2LMIX	0	111 = +6dB  Left Auxilliary input to left channel output mixer: 0 = not selected 1 = selected	Analogue Outputs



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4:2	BYPLMIXVOL	000	Left bypass volume control to output channel mixer:  000 = -15dB  001 = -12dB   101 = 0dB  110 = +3dB  111 = +6dB	Analogue Outputs
	1	BYPL2L MIX	0	Left bypass path (from the left channel input boost output) to left output mixer 0 = not selected 1 = selected	Analogue Outputs
	0	DACL2L MIX	1	Left DAC output to left output mixer 0 = not selected 1 = selected	Analogue Outputs
51 (33h)	8:6	AUXRMIXVOL	000	Aux right channel input to right mixer volume control:  000 = -15dB  001 = -12dB   101 = 0dB  110 = +3dB  111 = +6dB	Analogue Outputs
	5	AUXR2RMIX	0	Right Auxilliary input to right channel output mixer:  0 = not selected  1 = selected	Analogue Outputs
	4:2	BYPRMIXVOL	000	Right bypass volume contol to output channel mixer:  000 = -15dB  001 = -12dB   101 = 0dB  110 = +3dB  111 = +6dB	Analogue Outputs
	1	BYPR2RMIX	0	Right bypass path (from the right channel input boost output) to right output mixer  0 = not selected  1 = selected	Analogue Outputs
	0	DACR2RMIX	1	Right DAC output to right output mixer 0 = not selected 1 = selected	Analogue Outputs
52 (34h)	8	OUT1VU	N/A	LOUT1 and ROUT1 volumes do not update until a 1 is written to OUT1VU (in reg 52 or 53)	Analogue Outputs
7 LOUT1ZC 0 Headphon 1 = Chang		Headphone volume zero cross enable:  1 = Change gain on zero cross only  0 = Change gain immediately	Analogue Outputs		
	6	LOUT1MUTE	0	Left headphone output mute: 0 = Normal operation 1 = Mute	Analogue Outputs



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5:0	LOUT1VOL	111001	Left headphone output volume: 000000 = -57dB  111001 = 0dB 	Analogue Outputs
				111111 = +6dB	
53 (35h)	8	OUT1VU	N/A	LOUT1 and ROUT1 volumes do not update until a 1 is written to OUT1VU (in reg 52 or 53)	Analogue Outputs
	7	ROUT1ZC	0	Headphone volume zero cross enable:  1 = Change gain on zero cross only  0 = Change gain immediately	Analogue Outputs
	6	ROUT1MUTE	0	Right headphone output mute:  0 = Normal operation  1 = Mute	Analogue Outputs
	5:0	ROUT1VOL	111001	Right headphone output volume: 000000 = -57dB  111001 = 0dB  111111 = +6dB	Analogue Outputs
54 (36h)	8	OUT2VU	N/A	LOUT2 and ROUT2 volumes do not update until a 1 is written to OUT2VU (in reg 54 or 55)	Analogue Outputs
	7	LOUT2ZC	0	Speaker volume zero cross enable: 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6	LOUT2MUTE	0	Left speaker output mute: 0 = Normal operation 1 = Mute	Analogue Outputs
	5:0	LOUT2VOL	111001	Left speaker output volume: 000000 = -57dB  111001 = 0dB  111111 = +6dB	Analogue Outputs
55 (37h)	8	OUT2VU	N/A	LOUT2 and ROUT2 volumes do not update until a 1 is written to OUT2VU (in reg 54 or 55)	Analogue Outputs
	7	ROUT2ZC	0	Speaker volume zero cross enable:  1 = Change gain on zero cross only  0 = Change gain immediately	Analogue Outputs
	6	ROUT2MUTE	0	Right speaker output mute: 0 = Normal operation 1 = Mute	Analogue Outputs
	5:0	ROUT2VOL	111001	Right speaker output volume: 000000 = -57dB  111001 = 0dB  111111 = +6dB	Analogue Outputs
56 (38h)	8:7		00	Reserved	1
	6	OUT3MUTE	0	0 = Output stage outputs OUT3 mixer 1 = Output stage muted – drives out VMID. Can be used as VMID buffer in this mode.	Analogue Outputs
	5:4		00	Reserved	



REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3	OUT4_2OUT3	0	OUT4 mixer output to OUT3	Analogue
				0 = disabled	Outputs
				1= enabled	
	2	BYPL2OUT3	0	Left ADC input to OUT3	Analogue
				0 = disabled	Outputs
				1= enabled	
	1	LMIX2OUT3	0	Left DAC mixer to OUT3	Analogue
				0 = disabled	Outputs
				1= enabled	
	0	LDAC2OUT3	1	Left DAC output to OUT3	Analogue
				0 = disabled	Outputs
				1= enabled	
57 (39h)	8		0	Reserved	
	7	OUT3_2OUT4	0	OUT3 mixer output to OUT4	Analogue
				0 = disabled	Outputs
				1 = enabled	
	6	OUT4MUTE	0	0 = Output stage outputs OUT4 mixer	Analogue
				1 = Output stage muted – drives out VMID. Can	Outputs
				be used as VMID buffer in this mode.	
	5	OUT4ATTN	0	0 = OUT4 normal output	Analogue
				1 = OUT4 attenuated by 6dB	Outputs
	4	LMIX2OUT4	0	Left DAC mixer to OUT4	Analogue
				0 = disabled	Outputs
				1= enabled	
	3	LDAC2OUT4	0	Left DAC to OUT4	Analogue
				0 = disabled	Outputs
				1= enabled	
	2	BYPR2OUT4	0	Right ADC input to OUT4	Analogue
				0 = disabled	Outputs
				1= enabled	
	1	RMIX2OUT4	0	Right DAC mixer to OUT4	Analogue
				0 = disabled	Outputs
				1= enabled	
	0	RDAC2OUT4	1	Right DAC output to OUT4	Analogue
				0 = disabled	Outputs
				1= enabled	
59 (3Bh)	8:2		0000000	Reserved	
	1:0	ALCTST	00	ALC Test Mode	ALC Test
				00 = disabled	Mode
				11 = enabled	
61 (3Dh)	8	BIASCUT	0	Global bias control	Bias Control
				0 = normal	
				1 = 0.5x	
	7:0		00000000	Reserved	



# **DIGITAL FILTER CHARACTERISTICS**

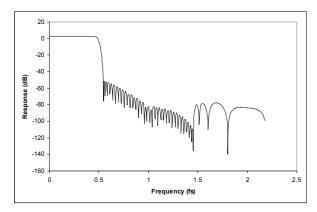
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
ADC Filter						
Passband	+/- 0.025dB	0		0.454fs		
	-6dB		0.5fs			
Passband Ripple				+/- 0.025	dB	
Stopband		0.546fs				
Stopband Attenuation	f > 0.546fs	-60			dB	
Group Delay			21/fs			
ADC High Pass Filter						
High Pass Filter Corner	-3dB		3.7		Hz	
Frequency	-0.5dB		10.4			
	-0.1dB		21.6			
DAC Filter						
Passband	+/- 0.035dB	0		0.454fs		
	-6dB		0.5fs			
Passband Ripple				+/-0.035	dB	
Stopband		0.546fs				
Stopband Attenuation	f > 0.546fs	-55			dB	
Group Delay			29/fs			

**Table 71 Digital Filter Characteristics** 

## **TERMINOLOGY**

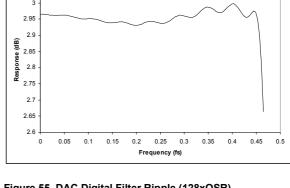
- 1. Stop Band Attenuation (dB) the degree to which the frequency spectrum is attenuated (outside audio band)
- 2. Pass-band Ripple any variation of the frequency response in the pass-band region

## **DAC FILTER RESPONSES**



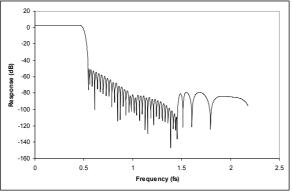
3.05 2.95 2.9 2.85 2.8 27 0.05 0.1 0.15 0.2 0.25 0.3 0.35

Figure 54 DAC Digital Filter Frequency Response (128xOSR)



-20 -60

Figure 55 DAC Digital Filter Ripple (128xOSR)



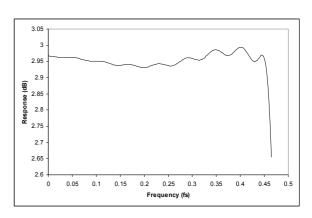
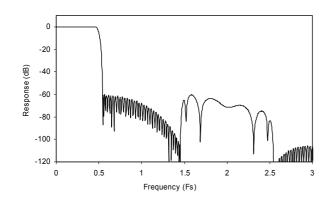


Figure 56 DAC Digital Filter Frequency Response (64xOSR)

Figure 57 DAC Digital Filter Ripple (64xOSR)

# **ADC FILTER RESPONSES**



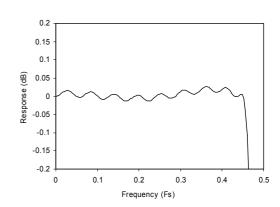


Figure 58 ADC Digital Filter Frequency Response

Figure 59 ADC Digital Filter Ripple



## **HIGHPASS FILTER**

The WM8983 has a selectable digital highpass filter in the ADC filter path. This filter has two modes, audio and applications. In audio mode the filter is a 1<sup>st</sup> order IIR with a cut-off of around 3.7Hz. In applications mode the filter is a 2<sup>nd</sup> order high pass filter with a selectable cut-off frequency.

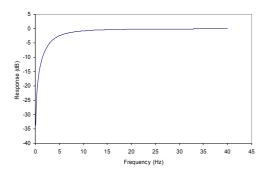
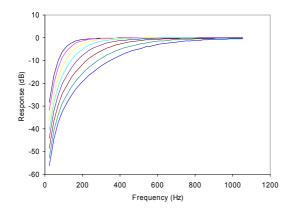


Figure 60 ADC Highpass Filter Response, HPFAPP=0



10 0 -10 -20 Response (dB) -30 -40 -50 -60 -70 0 200 400 600 800 1000 1200 Frequency (Hz)

Figure 61 ADC Highpass Filter Responses (48kHz), HPFAPP=1, all cut-off settings shown.

Figure 62 ADC Highpass Filter Responses (24kHz), HPFAPP=1, all cut-off settings shown.

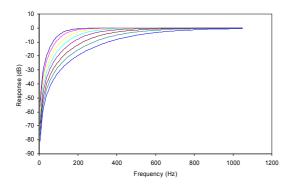
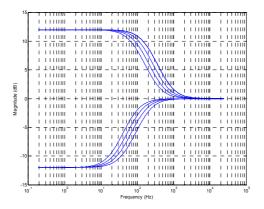


Figure 63 ADC Highpass Filter Responses (12kHz), HPFAPP=1, all cut-off settings shown.

#### **5-BAND EQUALISER**

The WM8983 has a 5-band equaliser which can be applied to either the ADC path or the DAC path. The plots from Figure 64 to Figure 77 show the frequency responses of each filter with a sampling frequency of 48kHz, firstly showing the different cut-off/centre frequencies with a gain of  $\pm 12$ dB, and secondly a sweep of the gain from -12dB to +12dB for the lowest cut-off/centre frequency of each filter.



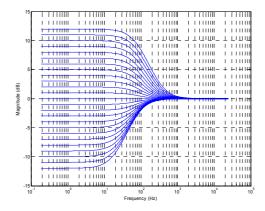
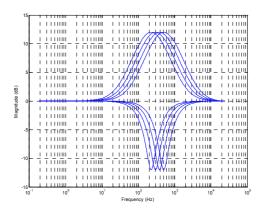


Figure 64 EQ Band 1 Low Frequency Shelf Filter Cut-offs

Figure 65 EQ Band 1 Gains for Lowest Cut-off Frequency



1.111101 LUUU 1.1111111 1.111100 1.1111111 1.111100 1.1111111 4 + 1411411-+ 11 11111 4 + 141411 1.111110 1 11111111 1.11111111 1.1111111 1.1111111 1.1.111111

Figure 66 EQ Band 2 – Peak Filter Centre Frequencies, EQ2BW=0

Figure 67 EQ Band 2 – Peak Filter Gains for Lowest Cut-off Frequency, EQ2BW=0

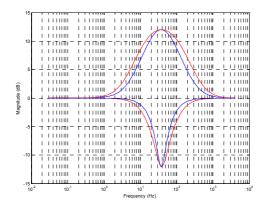
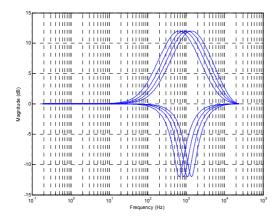


Figure 68 EQ Band 2 - EQ2BW=0, EQ2BW=1





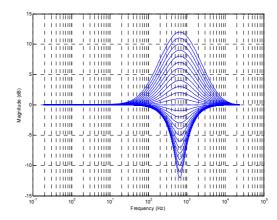


Figure 69 EQ Band 3 – Peak Filter Centre Frequencies, EQ3BW=0

Figure 70 EQ Band 3 – Peak Filter Gains for Lowest Cut-off Frequency, EQ3BW=0

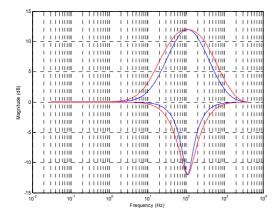
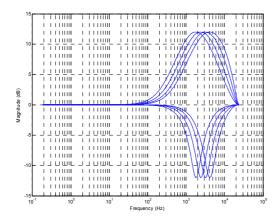


Figure 71 EQ Band 3 - EQ3BW=0, EQ3BW=1



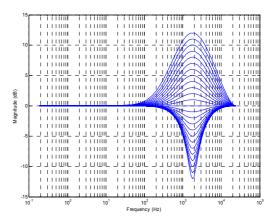


Figure 72 EQ Band 4 – Peak Filter Centre Frequencies, EQ3BW=0

Figure 73 EQ Band 4 – Peak Filter Gains for Lowest Cut-off Frequency, EQ4BW=0

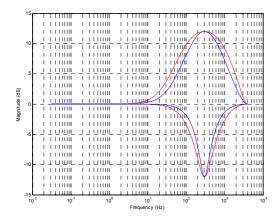
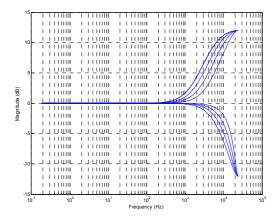


Figure 74 EQ Band 4 - EQ3BW=0, EQ3BW=1



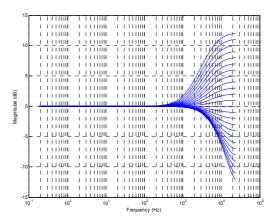


Figure 75 EQ Band 5 High Frequency Shelf Filter Cut-offs Figure 76 EQ Band 5 Gains for Lowest Cut-off Frequency

Figure 77 shows the result of having the gain set on more than one channel simultaneously. The blue traces show each band (lowest cut-off/centre frequency) with  $\pm 12$ dB gain. The red traces show the cumulative effect of all bands with  $\pm 12$ dB gain and all bands  $\pm 12$ dB gain, with EqxBW=0 for the peak filters.

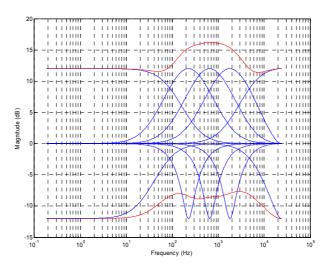


Figure 77 Cumulative Frequency Boost/Cut

# **APPLICATIONS INFORMATION**

## **RECOMMENDED EXTERNAL COMPONENTS**

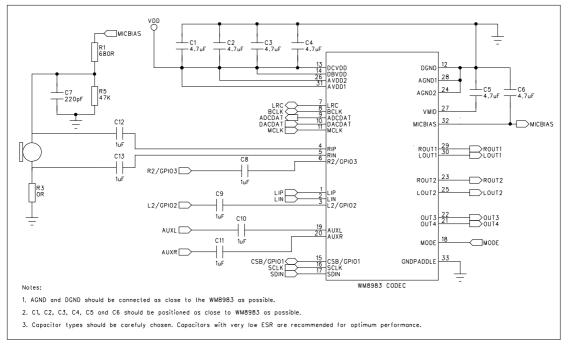
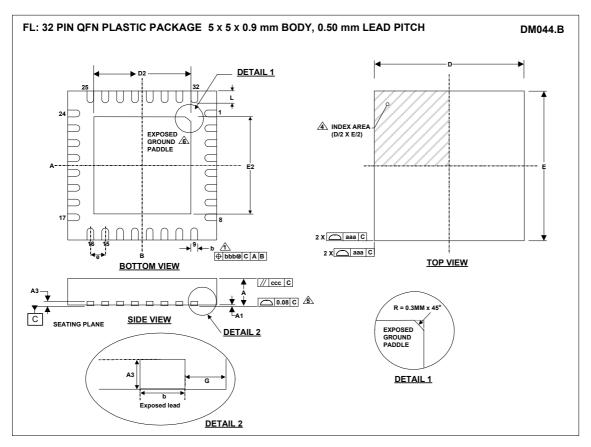


Figure 78 External Component Diagram

# **PACKAGE DIAGRAM**



Symbols		Dimensions (mm)				
	MIN	NOM	MAX	NOTE		
Α	0.80	0.85	0.90			
A1	0	0.02	0.05			
A3		0.203 REF				
b	0.20	0.25	0.30	1		
D		5.00 BSC				
D2	3.05	3.10	3.15	2		
E		5.00 BSC				
E2	3.05	3.10	3.15	2		
е		0.50 BSC				
G		0.625				
L	0.35	0.40	0.45			
	Tolerances	s of Form an	d Position			
aaa	0.15					
bbb	0.10					
ccc	0.10					
REF:	JEDEC	C, MO-220, V	ARIATION V	HHD-5.		

- NOTES:

  1. DIMENSION 5 APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
  2. FALLS WITHIN 15DEC, MO-220, VARIATION VHHD-5.
  3. ALL DIMENSIONS ARE IN MILLIMETRES.
  4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
  5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
  6. REFER TO APPLICATION NOTE WAN\_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
  7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.



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