IES5502

Fast Dual Bi-Directional Bus Buffer with Hot Insertion Logic

1 FEATURES

- Dual, bi-directional unity gain isolating buffer
- Hot insertion logic prevents data and clock bus corruption for live backplane applications
- Pre-charge minimises data corruption on live insertion
- Supports I²C(1) bus (standard and fast modes), SMBus (standard and high power modes) and PMbus
- Open-collector Ready output.
- Fast switching times allow operation in excess of 1MHz
- Enable allows bus segments to be disconnected
- Low current stand-by mode when not enabled
- High impedance ports when IC unpowered
- 4 mA (static) pull-down capability
- Low noise susceptibility
- Supports the connection of several buffers in series.
- Level shift bus voltages from 1.8 V to 15 V

2 APPLICATIONS

- Backplane Management / Interconnect
- Telecommunications Systems including ATCA
- Desktop and Portable Computers including RAID

(1) I²C is a trademark of NXP B.V.

3 GENERAL DESCRIPTION

The IES5502 is a monolithic bipolar integrated circuit for bus buffering in applications including I²C, SMBus, PMbus, and other systems based on similar principles.It extends the functionality of the IES5501 to include hot-insertion logic for detecting stop and idle conditions, making it ideal for live insertion into backplanes. The buffer extends the bus load limit by buffering both the SCL and SDA lines.

Hot insertion logic allows the IC to be plugged into live backplanes without causing data corruption on the bus. The open-collector READY signal indicates when the connection has been made. Precharging of the backplane ports minimises disruptions to the bus during hot insertion.

The enable function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line sucessively. Bus level translation between a very wide range of bus voltages, from 1.8 V to 15 V, is supported. These features provide enormous flexibility in interfacing systems of different technologies, operating speeds and loads.

The unique operation of the IES5502 provides one of the fastest response times of such bi-directional buffers. It does this without the need for “rise-time accelerators” which, combined with low noise margins, may cause glitches outside of the I²C specification.

4 BLOCK DIAGRAM

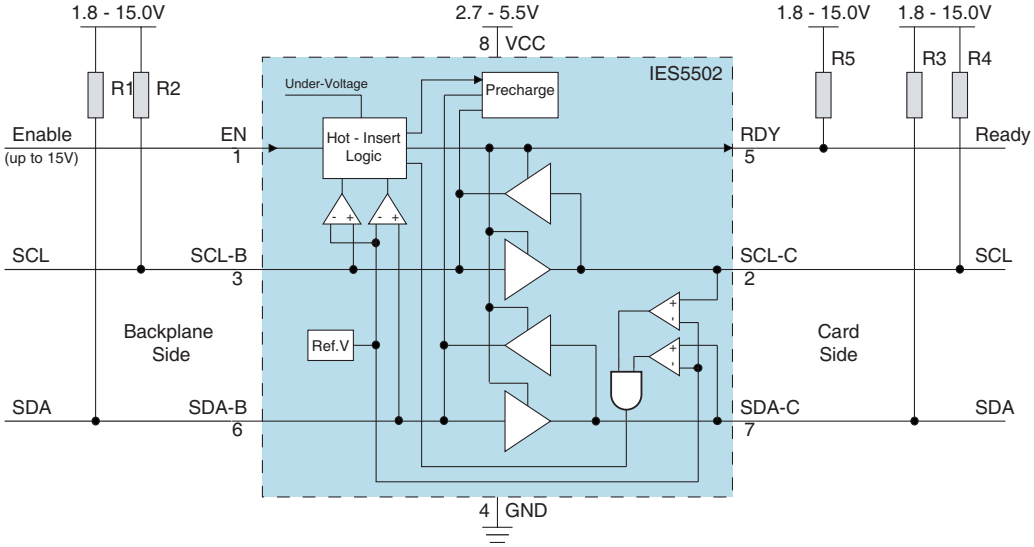

Fig.1 Block diagram

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Contents are subject to the Disclaimer

5 PINNING INFORMATION

5.1 Pinning layout

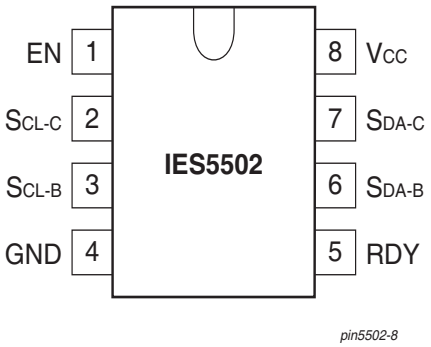

Fig.2 Pinning diagram (SO8)

5.2 Pin description

SYMBOL	PIN	DESCRIPTION
EN	1	Enable
S_{CL-C}	2	SCL Buffer, Card* Side
S_{CL-B}	3	SCL Buffer, Backplane* Side
GND	4	Supply Ground
RDY	5	Ready
S_{DA-B}	6	SDA Buffer, Backplane* Side
S_{DA-C}	7	SDA Buffer, Card* Side
V_{CC}	8	Positive supply

*For device family compatability, please note:
Backplane Side is equivalent to SCL_{IN} / SDA_{IN}
Card Side is equivalent to SCL_{OUT} / SDA_{OUT}

6 FUNCTIONAL DESCRIPTION

6.1 V_{CC}, GND - DC supply pins

The IES5502 can be driven from voltage supplies ranging from 2.7 V to 5.5 V. The threshold level below which the output will begin to match the input is 33% of V_{CC}. Hence, the operating voltage should be chosen with the required bus voltage, switching threshold, and noise margins, in mind.

6.2 S_{CL-B}, S_{CL-C}, S_{DA-B}, S_{DA-C} - Buffer inputs/outputs

The two buffers (S_{CL} and S_{DA}) are identical and symmetrical. The buffers can be driven from either direction, with the same buffering response. However, the hot insertion logic is determined from the “backplane” (S_{xx-B}) sides of the buffers. When the one side of (e.g. S_{xx-B}) of the buffer is being driven low (<0.3V_{CC}) by another device on the bus, the other side (e.g. S_{xx-C}) will be driven low by the IC to provide the buffered output.

The “control” or “input” side is determined by the lowest externally driven signal. Therefore if the “input” is externally pulled to V_{Sxx-B} = 250 mV, and the “output” is externally pulled to V_{Sxx-C} = 500 mV, the buffer will pull the “output” down further such that it becomes $V_{Sxx-C} = V_{Sxx-B} + V_{OFFSET}$. Should the “output” subsequently become lower than the “input” by means of an external device pulling it low ($V_{Sxx-C} < V_{Sxx-B}$), control of the buffering operation will switch sides. The voltage at the “input” will then become $V_{Sxx-B} = V_{Sxx-C} + V_{OFFSET}$. Many bus buffers are prone to causing glitches during control transition, but the IES5502 shows negligible glitching even under the worst operating conditions.

6.3 Enable (EN) - Activate Buffer Operations

The enable input (EN) is used to disable the buffer, for the purpose of isolating sections of the bus. The IC should only be disabled when the bus is idle, to prevent truncation of commands which may confuse other devices on the bus.

Upon receiving a valid Enable signal, the IC will wait to detect either a bus STOP condition, or an IDLE condition as described in the I^2C(1) and SMBus(2) specifications. This ensures that truncated transmissions are not communicated along the newly enabled bus segment.

Enable may be used to progressively activate sections of the bus during system start-up. Bus sections slow to respond on power-up can be kept isolated from the main system to avoid interference and collisions.

The Enable pin may be pulled up higher than the Vcc of the buffer, further enhancing the capability of the IES5502 in a level shifting role. For example, a microprocessor could drive Enable, S_{CL-B} and S_{DA-B} at 5V, while the buffer V_{CC}, S_{CL-C} and S_{DA-C} ports are at 3.3V.

Similarly, the threshold level of the Enable pin allows a 1.8V device to enable an IES5502 with a V_{CC} of 3.3V.

(1) “UM10204: I2C-bus Specification and User Manual”, Rev 03, 19 June 2007, NXP B.V.
(2) “System Management Bus (SMBus) Specification”, Version 2.0, August 3, 2000, SBS Implementers Forum.

6.4 Ready (RDY) - Buffer Connected Indicator

The ready output (RDY) indicates that the buffer has met it's enable conditions, and that communication will now occur. This is an open-collector transistor which is switched off when ready, allowing the voltage at the pin to be pulled high by a pull-up resistor.

6.5 Start-up

During power-up or live insertion into backplanes, the IES5502 will start-up in an under voltage lock-out state (UVLO) where any activity on the input-output ports will be ignored. This is to ensure that the IES5502 does not try to operate when there is not enough voltage on the supply.

During this time, the pre-charge circuit will charge all S_{CL-B}/S_{DA-B} backplane ports to a typically 0.73V. This will minimise any voltage difference between the ports and hence minimises disruptions to the bus during hot insertion into backplanes.

When the supply increases above the UVLO state, the IES5502 will then monitor the bus for either stop bit or bus idle condition. When a stop bit condition is detected and S_{CL-C}/S_{DA-C} are both idle or when all S_{CL}/S_{DA} ports idle for a time period of typically 95µS, then the IES5502 will activate the input-output connection circuitry. The pre-charge circuitry is switched off. The voltage at the READY pin is pulled high by an external pull-up resistor to indicate the input-output connection has been made.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are specified with respect to pin 4 (GND)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage range (V_{CC})		–0.3	+7	V
V_{Sxx-x}	Voltage range (S_{CL-B}, S_{CL-C}, S_{DA-B}, S_{DA-C})		–0.3	+16	V
V_{EN}	Voltage range (EN)		–0.3	+16	V
I	DC current (any pin)		–	20	mA
P_{tot}	total power dissipation		–	300	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	operating ambient temperature		–40	+85	°C

8 CHARACTERISTICS

All specifications apply over the full operating temperature range of T_{amb} = -40°C to +85°C;
Voltages are specified with respect to pin 4 (GND)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply						
V_{CC}	supply voltage (operating)		2.7	–	5.5	V
I_{CC}	supply current (operating)	V_{CC}= V_{EN}= 5.5V	–	6.1	–	mA
	supply current (stand-by)	V_{CC}= 5.5V, V_{EN} = 0V	–	580	–	µA
Startup circuitry						
UVLO	under voltage lock-out level	V_{CC}= V_{EN}	–	2.2	–	V
V_{PRE}	precharge voltage level	V_{xxx-B} floating, V_{CC} = 3.3V, V_{EN} >1.2V	–	0.73	–	V
I_{PRE}	precharge current level	V_{xxx-B} > V_{PRE}, V_{CC} = 3.3V, V_{EN} > 1.2V	–	20	–	µA
V_{THR}	logic input threshold voltage		–	$0.5V_{CC}$	–	V
	logic output threshold voltage		–	$0.5V_{CC}$	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Buffer Ports						
V_{Sxx-x}	Bus voltage		1.8	–	15	V
V_{TL}	Input low threshold voltage		$0.30V_{CC}$	$0.33V_{CC}$	$0.41V_{CC}$	V
I_{IL}	Input low current	$V_{Sxx-x} < V_{CC}$	–	–	-10	µA
I_{OL}	Output low sink current	$V_{Sx-xx(in)} = 0V$	4	–	–	mA
V_{OFFSET}	Input-output offset voltage (V_{CC} = 3.3V)	I_{OL} = 4 mA, $V_{Sxx-x(in)}$ = 50mV	–	200	250	mV
		I_{OL} = 500µA, $V_{Sxx-x(in)}$ = 50mV	–	80	100	mV
		I_{OL} = 1.2mA, $V_{Sxx-x(in)}$ = 200mV	–	85	125	mV
I_{LEAK}	Leakage current	$V_{Sxx-x} = V_{CC}$	–	–	±5	µA
Enable						
V_{EN}	Enable active voltage		1.2	–	–	V
$V_{DISABLE}$	Disable (stand-by) voltage		–	–	0.8	V
I_{EN}	Enable Pin Current	V_{EN} > 1.2V	1	–	5	µA
Ready						
V_{RL}	Ready low voltage	I_{RDY} = 3mA	–	–	400	mV
I_{leak}	leakage current	$V_{RDY} = V_{CC}$	–	–	±5	µA
Timing Characteristics (note 1)						
td	Response Delay	$0.3V_{CC}$ to $0.7V_{Sxx-x(out)}$	–	45	–	ns
tf	Fall Time	$0.7V_{Sxx-x(out)}$ to $0.3V_{Sxx-x(out)}$	–	40	–	ns
f_{Sxx}	Operating Frequency		0	400	–	kHz
t_{idle}	Bus Idle Time	$V_{Sxxx-x} = V_{EN} = V_{CC}$ = 3.3V	50	95	150	µs
		$V_{Sxxx-x} = V_{EN} = V_{CC}$ = 5.5V	50	75	120	µs
t_{ENLH}	ENABLE High to READY off		–	95	–	µs
t_{ENHL}	ENABLE Low to READY on		–	1		µs
t_{RDYLH}	READY High to V_{Sxxx-x} on		–	1		µs
t_{RDYHL}	READY Low to V_{Sxxx-x} off		–	1.1		µs

Note

1. Guaranteed by design (not subject to test), except for t_{idle}

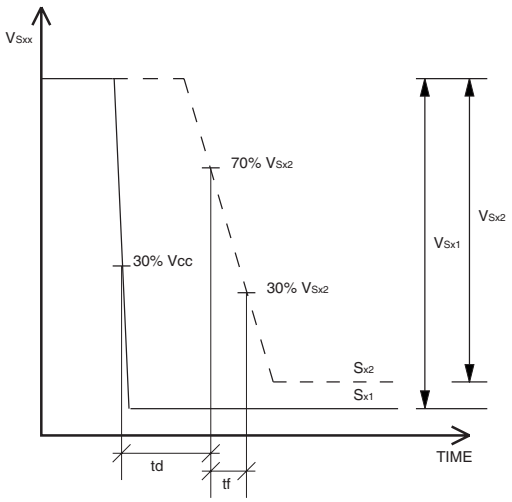

Fig.3 Timing Parameters

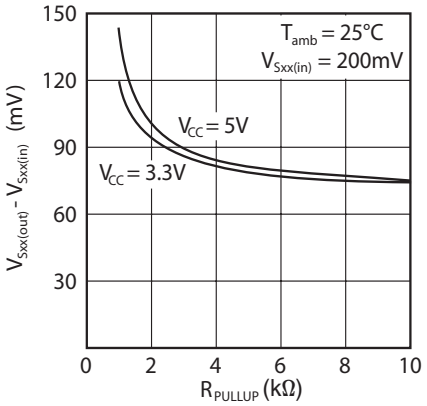

Fig.4 Offset Voltage, Vout - Vin

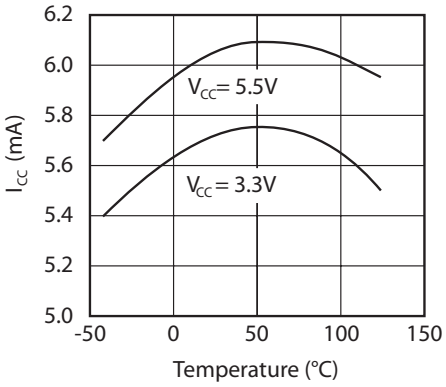

Fig.5 Supply Current vs Temperature

9 APPLICATION INFORMATION

9.1 Design Considerations

Figure 6 shows a typical application for the IES5502. The IC can level shift between various bus voltages, without the need for additional external components. Higher bus voltages and currents outside the range of the standard I^2C bus specification can be catered for, providing a longer range capability and higher noise immunity.

The enable pin can be used to interface buses of different operating frequencies. When enabled, the bus frequency is limited to the maximum 100 kHz of the slave device. When disabled, the slave is isolated, and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow it to run well in excess of the 400 kHz maximum limit of the I^2C fast mode.

Figure 7 shows the IES5502 used in a backplane application. Peripheral cards and backplanes operating at a range of voltages can be interfaced together using a minimum of components. In this example, cards are running at 1.8 V and 3V, while the backplane is at 5V. Cards operating buses between 1.8 V and 15 V can be catered for in the same system.

Each card can be safely isolated from the system by disabling the IES5502 at the interface to the backplane. The Hot-Insertion logic on the IES5502 protects against corrupted or truncated data transmissions on start-up of buffer operations.

An ideal backplane application for the IES5502 is the Advanced Telecom Computing Architecture (AdvancedTCA) as shown in Figure 8. The IES5502 is well suited to placement on “Field Replaceable Units” (FRUs) used in either a conventional fully-bused arrangement (not shown) or in the low cost high noise margin radial architecture example as shown in Figure 9. It is fully interoperable with existing systems and components. If required, Figure 9 shows a simple low-cost circuit for use at the Shelf Manager for accelerating the rise in bused systems.

In each of these examples, the buffers are intended to extend total system capacitance above 400pF, so anticipate high capacitance on each side. When loading on one side is small, adding 47pF is suggested to avoid any waveform ripple, should it occur.

9.2 Input to Output Offset Voltage Calculation

The offset voltage between the side acting as the output ($S_{xx(out)}$) and the side acting as the input ($S_{xx(in)}$) of the IES5502 can be calculated using the relationship:

$$V_{Sxx(out)} = V_{Sxx(in)} + 69mV + (V_{BUS}/R) \bullet 15[\Omega]$$

This calculation is valid for $V_{Sxx(in)} \geq 200mV$, as below this point the saturation voltage of the open collector output drive transistor will begin to affect the characteristic. Input and output voltages are shown in millivolts, V_{BUS} (the supply voltage to the bus) is in volts, and R is in ohms.

An example calculation for VBUS = 3.3V, V_{SA1} = 200mV, the resistance R pulling up S_{A2} is 2k, then the voltage on S_{A2} is typically:

$$V_{SA2} = 200mV + 69mV + (3.3/2000) \bullet 15$$
$$= 294mV$$

This can be compared with the offset characteristic shown in Figure 4.

Application circuits

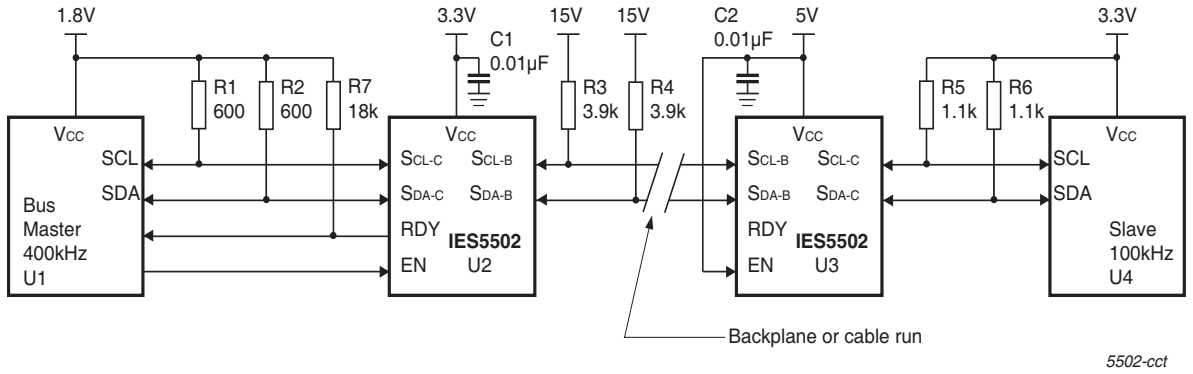

Fig.6 IES5502 typical buffer application

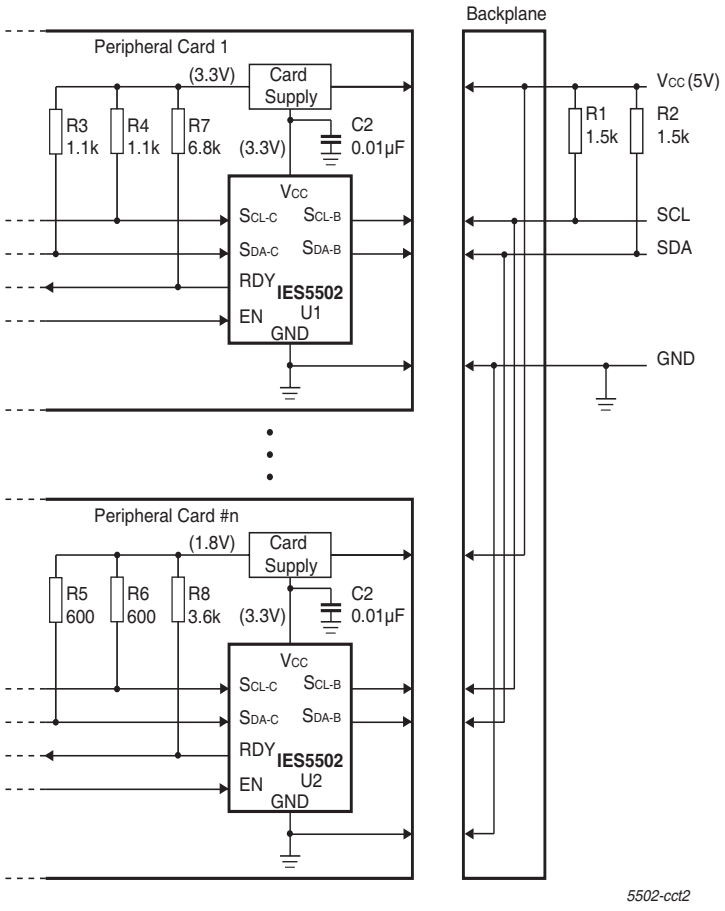

Fig.7 IES5502 backplane application

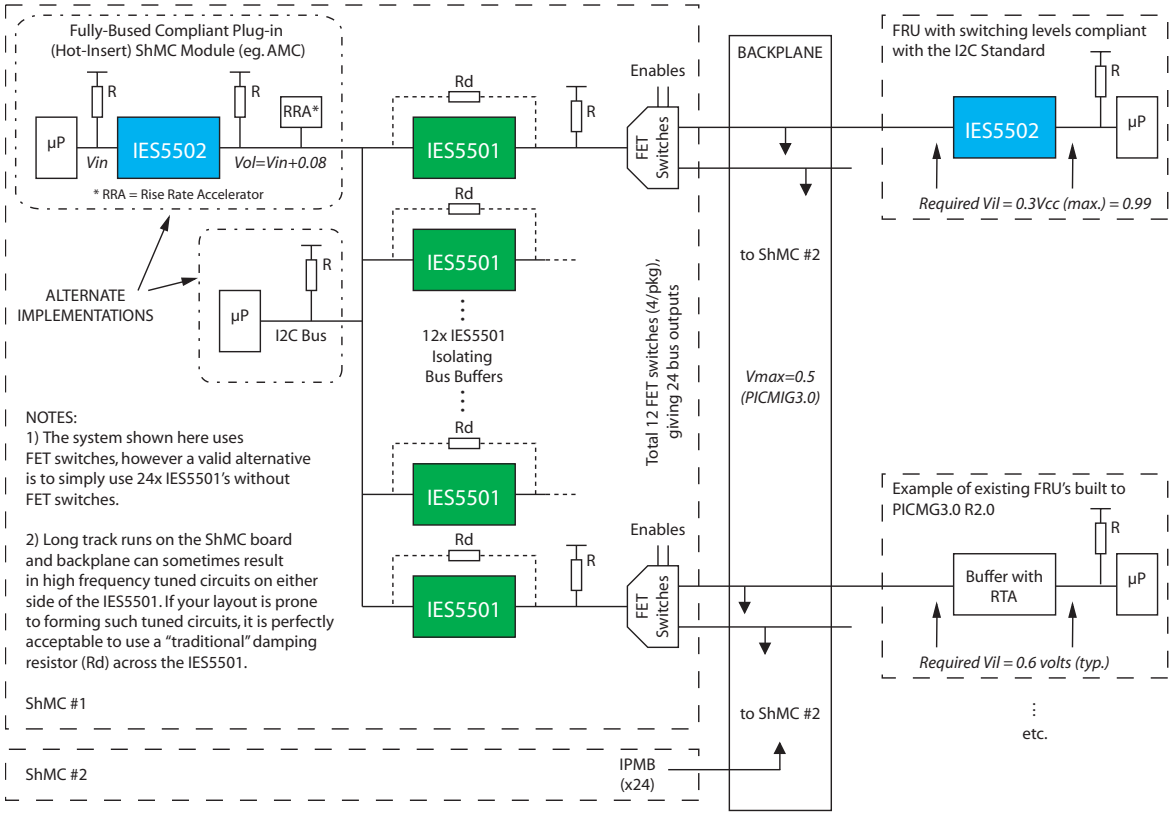

Fig.8 IES5502 used in an AdvancedTCA application
in conjunction with the IES5501

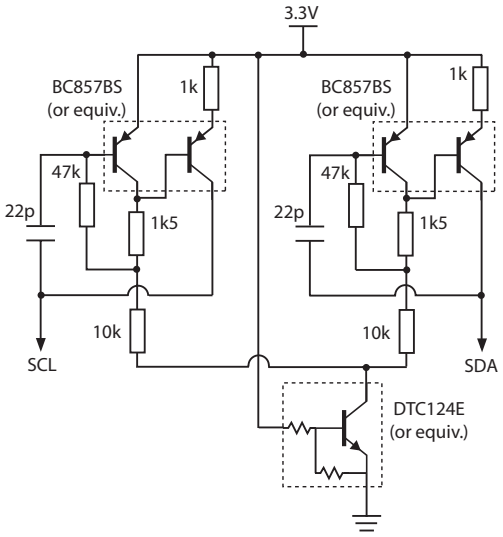

Fig.9 An example discrete Rise Rate Accelerator circuit

10 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5502T	SO8	plastic small outline package; 8 leads; body width 3.9 mm supplied in tube	SOT96-1	Yes
IES5502TR	SO8	plastic small outline package; 8 leads; body width 3.9 mm supplied in tape and reel	SOT96-1	Yes
IES5502D	MSOP-8L	micro small outline package; 8 leads; body width 3.0 mm supplied in tube	SOT505-1	Yes
IES5502DR	MSOP-8L	micro small outline package; 8 leads; body width 3.0 mm supplied in tape and reel	SOT505-1	Yes

Other package options are available - contact Hendon Semiconductors for details. For more information on packages, please refer to the document “Integrated Circuit Packaging and Soldering Information” on the Hendon Semiconductors web site.

11 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.

12 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
1.0	20080320	Product Specification
1.1	20080421	Pre-charge condition update
1.2	20080513	Fix pre-charge condition typo
1.3	20080526	Note to table in Section 5.2
1.4	20080724	Change from commercial to industrial temperature; update section 8 characteristics
1.5	20110114	Update Section 10 to include tape and reel parts

13 DEFINITIONS

Data sheet status	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility.Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

14 COMPANY INFORMATION

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