

### 1 FEATURES

- Drop-in pin compatible with other manufacturer's parts
- Each I/O is impedance isolated from all others allowing maximum capacitance on all branches.
- 30mA static sink capability on all ports.
- Works with I<sup>2</sup>C-bus<sup>(1)</sup> (Standard, Fast Mode, and FM+), SMBus (standard and high power mode), and PMbus
- Fast switching times allow operation in excess of 1MHz
- Allows driving of large loads (eg. 5x 4nF)
- Hysteresis on I/O increases noise immunity
- Operating voltages from 2.7 V to 5.5 V
- Uncomplicated characteristics suitable for quick implementation in most common 2-wire bus applications

### 2 APPLICATIONS

- Large arrays of I<sup>2</sup>C components - eg LED displays;
- Power Management Systems;
- Game Consoles; Computers; RAID systems;

(1) I<sup>2</sup>C-bus is a trademark of NXP B.V.

### 4 BLOCK DIAGRAM

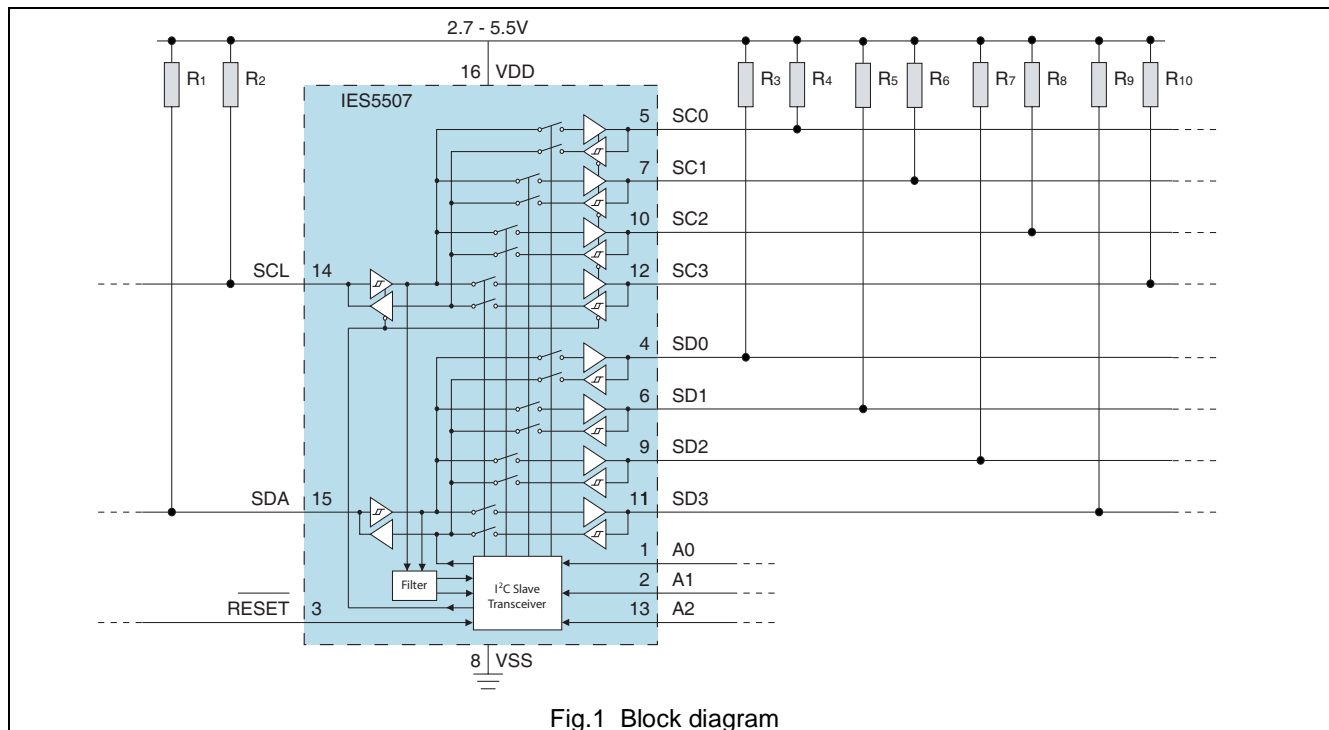


Fig.1 Block diagram

### 3 GENERAL DESCRIPTION

The IES5507 is a monolithic CMOS integrated circuit for 2-wire bus buffering and switching in applications including I<sup>2</sup>C, SMBus, PMbus, and other systems based on similar principles.

Each of the four outputs may be independently enabled in any combination as determined by the contents of the programmable control register. Each I/O is impedance isolated from all others, thus allowing a total of five branches of 2-wire bus with the maximum specified load (e.g. 5x 400pF for I<sup>2</sup>C FM+ at 1MHz, or 5x 4nF at lower frequencies). More than one IES5507 may be used in series, providing a substantial fan-out capability.

As per the IES5505/15 simple bus buffers, the IES5507 includes a uni-directional buffer for the clock signal, and a bi-directional buffer for the data signal. The direction of the clock signal may also be set by the contents of the programmable control register. Clock stretching and timing must always be under control of the Master device.

The IES5507 has excellent application to 2-wire bus address expansion and increasing of maximum load capacitance. Very large LED displays are a perfect example.

### 5 PINNING INFORMATION

#### 5.1 Pin description

SYMBOL	PIN	DESCRIPTION
A0	1	Address Input 0
A1	2	Address Input 1
$\overline{\text{RESET}}$	3	Active Low Reset Input
SD0	4	Serial Data 0
SC0	5	Serial Clock 0
SD1	6	Serial Data 1
SC1	7	Serial Clock 1
V <sub>SS</sub>	8	Negative supply (ground)
SD2	9	Serial Data 2
SC2	10	Serial Clock 2
SD3	11	Serial Data 3
SC3	12	Serial Clock 3
A2	13	Address Input 2
SCL	14	Serial Clock Line (normally in)
SDA	15	Serial Data Line
V <sub>DD</sub>	16	Positive supply

#### 5.2 Pinning layout

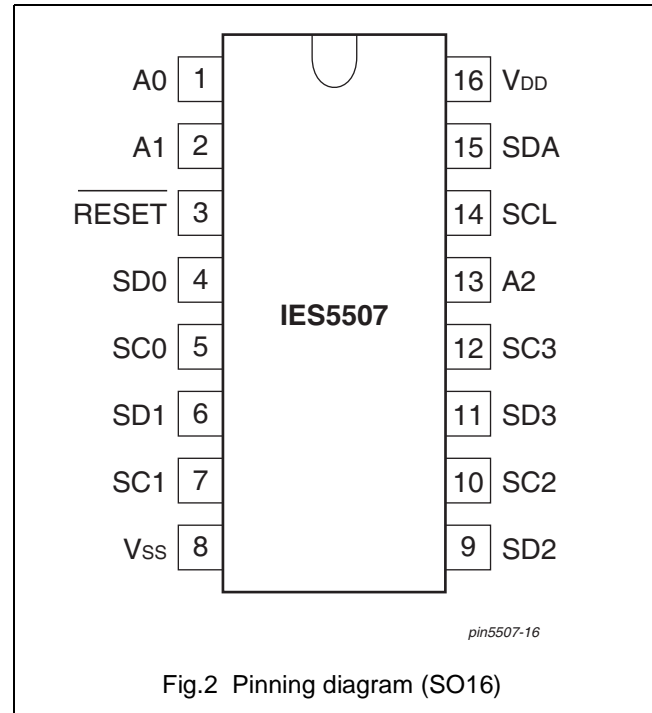


Fig.2 Pinning diagram (SO16)

### 6 FUNCTIONAL DESCRIPTION

#### 6.1 V<sub>DD</sub>, V<sub>SS</sub> - DC supply pins

The power supply voltage for the IES5507 may be any voltage in the range 2.7 V to 5.5 V. The IC supply must be common with the supply for the bus. Hysteresis on the ports are a percentage of the IC's power supply, hence noise margin considerations should be taken into account when selecting an operating voltage.

#### 6.2 SCL - Clock Signal Input

The clock signal buffer is uni-directional, with this pin acting as the default input. However, the clock signal direction may be reversed by setting the MSB of the control register HIGH. In normal bus operations, for example the I<sup>2</sup>C bus, the Master device generates a uni-directional clock signal to the slave. For lowest cost the IES5507 combines uni-directional buffering of the clock signal with a bi-directional buffer for the data signal. Clock stretching is therefore not supported and Slave devices that may require clock stretching must be accommodated by the Master adopting an appropriate clocking when communicating with them.

The buffer includes hysteresis to ensure clean switching signals are output, especially with slow rise times on high capacitively loaded buses.

#### 6.3 SC0, SC1, SC2, SC3 - Clock Signal Outputs

The clock signal from SCL is buffered through four independent buffers, and the signal is presented at the four SC0..3 ports. Ports are open-drain type and require external pullup resistors.

When the MSB of the control register is set HIGH, the port direction is reversed. The 'AND-ed' result of the four SC0..3 lines is then used to drive the open drain output of the SCL pin.

#### 6.4 SDA, SD0..3 - Data Signal Inputs/Outputs

The data signal buffers are bi-directional. The port (SDA, or any one of SD0..3) which first falls low, will decide the direction of this buffer and "lock out" signals coming from the opposite side. As the "input" signal continues to fall, it will then drive the open-drain of the "output" side low. Again, hysteresis is applied to the buffer to minimise the effects of noise. Ports are open-drain type and require external pullup resistors.

At some points during the communication, the data direction will reverse - for example, when the Slave transmits an acknowledge (ACK) or responds with its register contents. During these times, the controlling "input" side will have to rise to  $V_{LK}$  before it releases the "lock", which then allows the "output" side to gain control, and pull (what was) the "input" side low again. This will cause a "pulse" on the "input" side, which can be quite large in high capacitance buses. However, this pulse will not interfere with the actual data transmission, as it should not occur during times of clock line transition (during normal I<sup>2</sup>C and SMBus protocols), and thus data signal set-up time requirements are still met.

### 6.5 $\overline{RESET}$ - Reset IC to Default State

The active low  $\overline{RESET}$  input is used to disable the buffer, and reset it to its default state. The IC should only be disabled when the bus is idle to avoid truncation of commands which may confuse other devices on the bus.

The  $\overline{RESET}$  signal will clear the contents of the control register, which has the effect of disabling all output lines SC0..3 and SD0..3. It is the nature of the I<sup>2</sup>C protocol that devices may become 'stuck'. To help in the clearing of this condition, the IES5507 can be reset, and each port brought on-line successively to find the component holding the bus low.

### 6.6 Power On Reset (POR)

During power-on, the IES5507 is internally held in the reset condition for a maximum of  $t_{RST} = 500ns$ . The default condition after reset is for the Control Register to be Erased (all zeros), resulting in all output channels being disabled.

### 6.7 A0, A1, A2 - Address lines

The slave address of the IES5507 is shown in the Figure 3. The address pins (A2..0) must be driven to a HIGH or LOW level - they are not internally pulled to a default state.

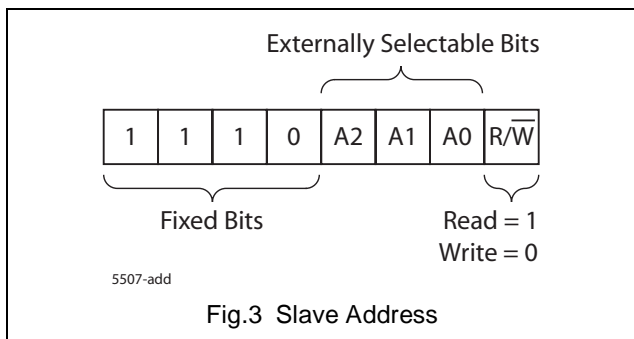


Fig.3 Slave Address

The read/write bit must be set LOW to enable a write to the control register, or HIGH to read from the control register.

### 6.8 Control Register

The control register of the IES5507 is shown in the Figure 4. Each of the four output channels (SCx/SDx pairs) can be enabled independently, and the direction of the clock signal can be reversed.

A LOW or zero bit (B3..0) indicates that the respective channel (SC3..0 / SD3..0) is disabled. The default reset condition of the register is all zeros, all channels disabled, forward direction. A HIGH or one bit indicates the respective channel is enabled.

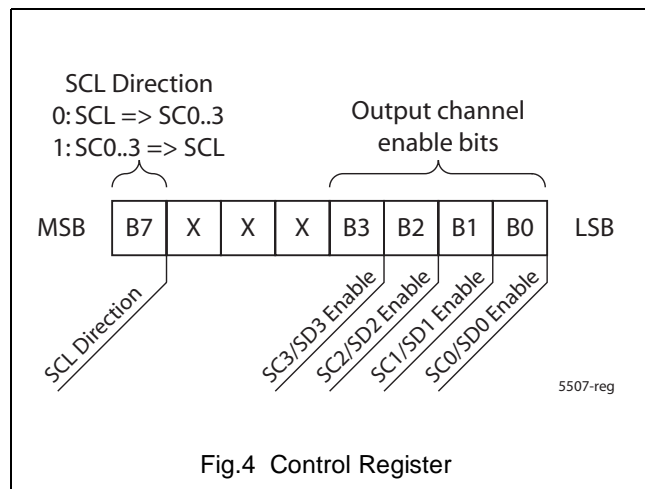


Fig.4 Control Register

Example: B3 = 1, B2 = 0, B1 = 1, B0 = 0 means channels 3 (SC3/SD3) and 1 (SC1/SD1) are enabled, and channels 2 (SC2/SD2) and 0 (SC0/SD0) are disabled.

As each channel is individually buffered, the loads on each are isolated, and therefore there is no special requirement to keep the sum of the collective capacitances below the maximum bus capacitance. Instead, each line may have up to the maximum bus capacitance and be enabled or disabled without affecting the performance of the other channels.

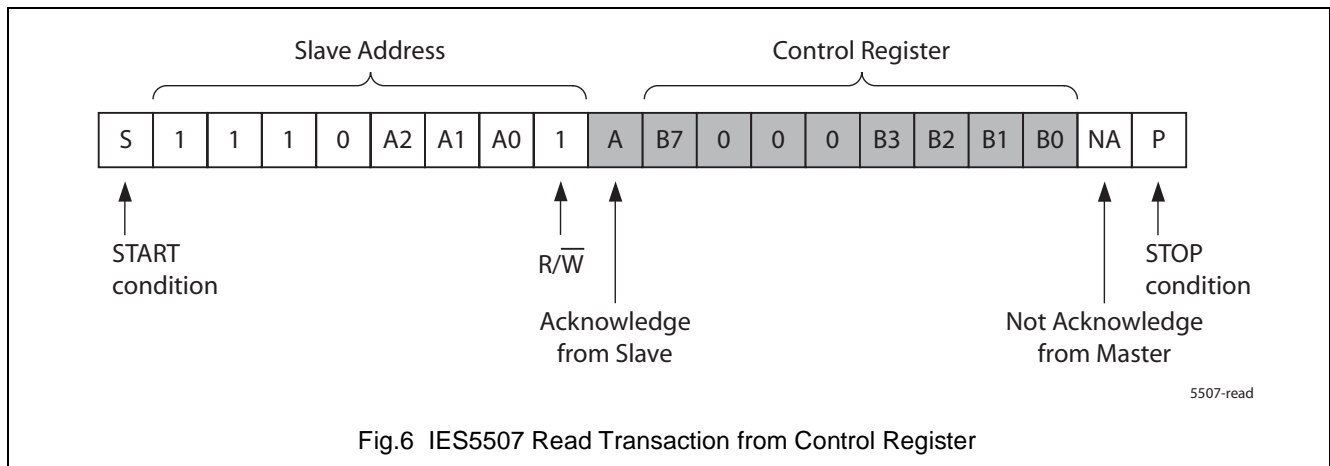
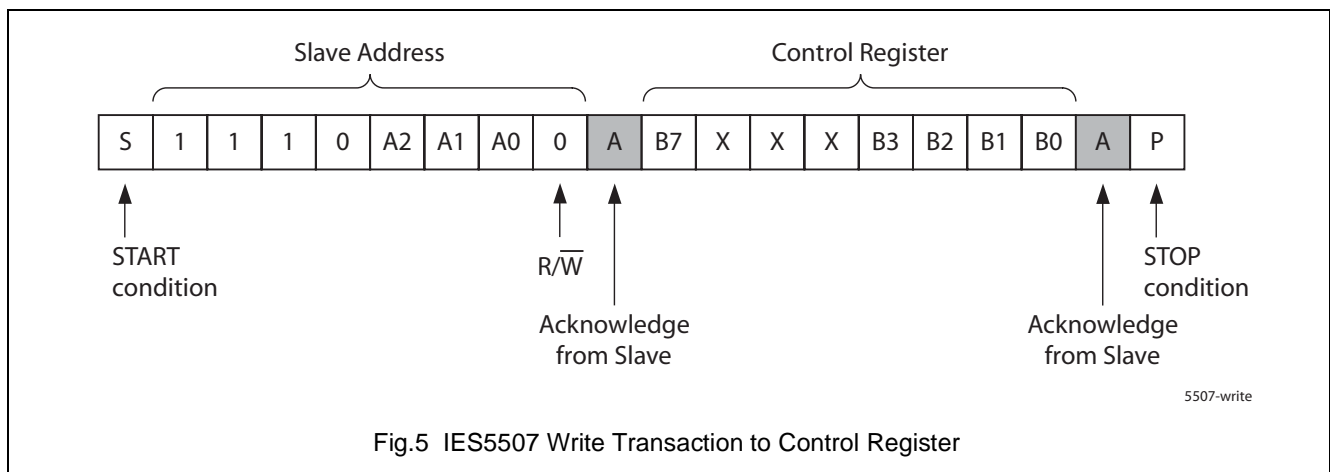
The Most Significant Bit (MSB) B7 is used to set the direction of the SCL (clock) signal. The default state is LOW (zero). In this state, the SCL port will act as the input, and the IC will supply a buffered signal to any of the four output channels (SC0..3) which are enabled. When B7 is set HIGH (one), the clock signal direction is reversed. The ports SC0..3 act as inputs, the AND-ed combination of their signals is buffered and output on the SCL pin.

The IES5507 is always addressable from the SCL/SDA side, regardless of the state of B7. Any device which can communicate data to the SCL/SDA pins, either by being directly attached to those pins or by transmitting through

the IES5507 (when B7=1), may address the device and change the control register's contents. The control register is only updated upon receipt of the STOP condition.

### 7 BUS TRANSACTION

A typical I<sup>2</sup>C write transaction to the IES5507 is shown in Figure 5. A typical read transaction is shown in figure 6.



### 8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are specified with respect to pin 8 ( $V_{SS}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	Supply voltage range ( $V_{DD}$ )		-0.3	+7	V
$V_{Sxx}$	Voltage range ( $SDA_x, SCL_x$ )		$V_{SS}-0.5$	$V_{DD}+0.5$	V
$V_{RST}$	Voltage range ( $\overline{RESET}$ )		$V_{SS}-0.5$	$V_{DD}+0.5$	V
$V_{A2..0}$	Voltage range (ADDRESS pins)		$V_{SS}-0.5$	$V_{DD}+0.5$	V
I	DC current (pins other than SCx/SDx)		-	20	mA
	DC current (all SCx and SDx)		-	40	mA
	DC current ( $V_{SS}$ pin)		-	280	mA
$P_{tot}$	total power dissipation		-	300	mW
$T_{stg}$	storage temperature		-55	+125	°C
$T_{amb}$	operating ambient temperature		-40	+85	°C

### 9 CHARACTERISTICS

All specifications apply over the full operating temperature range of  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;

Voltages are specified with respect to pin 8 ( $V_{SS}$ );  $V_{DD} = 5.5\text{V}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	$V_{DD}(\text{V})$				
<b>Power supply</b>							
$V_{DD}$	supply voltage (operating)			2.7	-	5.5	V
$I_{DD}$	supply current (quiescent)	$V_{RST} = 0\text{V}$	5.5	-	-	0.1	$\mu\text{A}$
<b>I2C Ports (SCL / SDA / SC3..0 / SD3..0)</b>							
$V_{Sxx}$	Bus voltage (SDX, SCX)			-	-	$V_{DD}+0.3$	V
$V_{LK}$	Lock-out input voltage - locked	[2]	2.7	-	-	1.3	V
			5.5	-	-	3.0	V
	Lock-out input voltage - unlocked	[2]	2.7	2.0	-	-	V
			5.5	4.8	-	-	V
$V_{IL}$	LOW-level input voltage	[2]	2.7	-	-	0.4	V
			5.5	-	-	0.5	V
$V_{IH}$	HIGH-level input voltage	[2]	2.7	1.2	-	-	V
			5.5	2.0	-	-	V
$V_{Sxx(\text{hys})}$	Input Hysteresis	[2]	2.7	80	-	-	mV
			5.5	200	-	-	mV
$I_{IL}$	Input low leakage current	$V_{Sxx} = V_{DD}$		-	-	$\pm 0.1$	$\mu\text{A}$
$I_{OL}$	Output low sink current	$V_{Sxxin} < V_{IL}$		30	-	-	mA
$V_{OL}$	Output low voltage	$I_{OL} = 30\text{mA}$	2.7	-	110	300	mV
			5.5	-	80	250	mV

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>DD</sub> (V)				
<b>RESET</b>							
V <sub>RST(hi)</sub>	HIGH-level input voltage		2.7	2.0	–	–	V
			5.5	4.8	–	–	V
V <sub>RST(lo)</sub>	LOW-level input voltage		2.7	–	–	650	mV
			5.5	–	–	900	mV
V <sub>RST(hys)</sub>	RESET Hysteresis		2.7	100	–	–	mV
			5.5	200	–	–	mV
I <sub>RST</sub>	Input leakage current	V <sub>RST</sub> = V <sub>DD</sub>	–	–	–	±0.1	μA
t <sub>w-RST(lo)</sub>	LOW-level reset time	V <sub>RST</sub> < V <sub>IL(RST)</sub> [1]	–	25	–	–	ns
t <sub>RST</sub>	Reset (and POR) time	from V <sub>RST</sub> > V <sub>IH(RST)</sub>	–	250	500	–	ns
<b>Address A0, A1, A2</b>							
V <sub>A2..0(hi)</sub>	HIGH-level input voltage		2.7	1.7	–	–	V
			5.5	3.5	–	–	V
V <sub>A2..0(lo)</sub>	LOW-level input voltage		2.7	–	–	0.7	V
			5.5	–	–	1.5	V
I <sub>A2..0</sub>	Input leakage current	V <sub>A2..0</sub> = V <sub>DD</sub>	–	–	–	±0.1	μA
<b>Timing Characteristics (refer Figure 7)</b>							
td	Response Delay	R <sub>Sxx(PULLUP)</sub> = 200ohm	2.7	–	100	–	ns
			5.5	–	70	–	ns
tf	Fall Time	R <sub>Sxx(PULLUP)</sub> = 200ohm	–	16	–	–	ns

### Notes

- [1] Guaranteed by design, not subject to test.  
 [2] Supply voltage dependant. Refer graphs for typical trend.

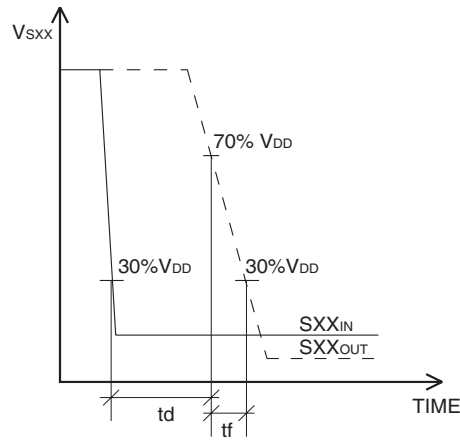


Fig.7 Timing Conditions

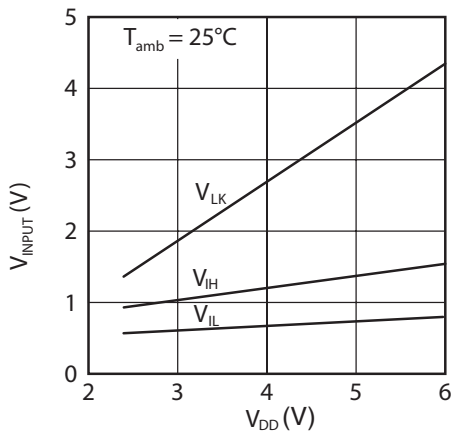
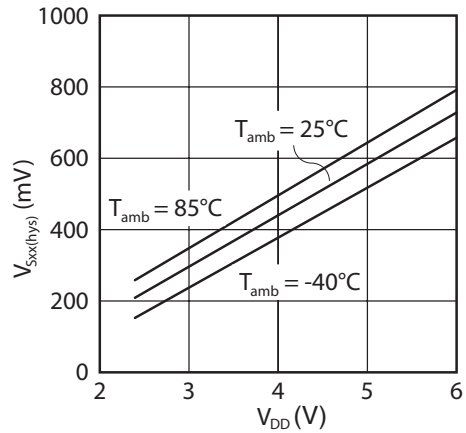
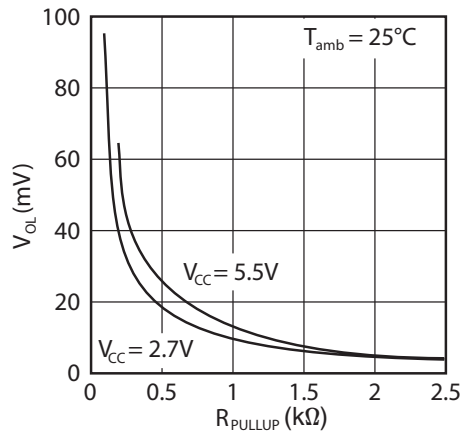
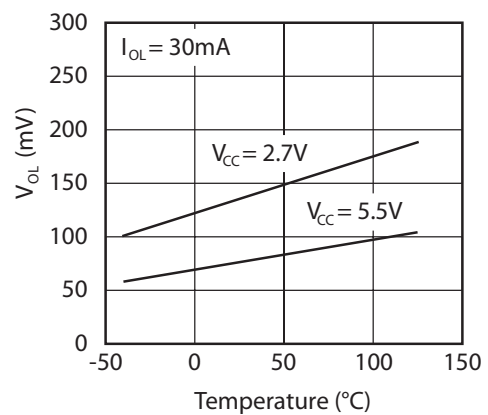


Fig.8 Typ.Input Levels vs. Supply Voltage


 Fig.9 Typical  $V_{IH} - V_{IL}$  Hysteresis vs. Supply Voltage

 Fig.10 Typical  $V_{OL}$  vs. pull-up resistance

 Fig.11 Typical  $V_{OL}$  vs. Temperature

### 10 APPLICATION INFORMATION

#### 10.1 Design Considerations

Figure 12 shows a typical data transfer through the IES5507. The IES5507 has excellent application to extending loads and expanding the address space of slave devices. Rise times are determined simply by the side of the buffer with the slowest RC time constant.

Figure 13 shows a typical application for the IES5507. Each channel can support up to the maximum permissible capacitance load, thus the maximum loading of the system can be 5x that which could be achieved with out buffering.

The channel enable function can be used to interface buses of different operating frequencies. When certain bus sections are enabled the system frequency may be limited by a bus section having a slave device specified only to 100 kHz. When that bus section is disabled, the slow slave is isolated and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow the IES5507 to run in excess of the 1MHz maximum limit of the I<sup>2</sup>C fast mode plus, or to run a huge 4nF of load at 100kHz.

Figure 14 shows the IES5507 used as a line driver. Four such lines (only one shown) can be run from the same device. The receiving end may then again be used as a 4 way bus switch, radiating out into another four lines.

Using the address pins, this entire structure may be repeated. Thus a total of eight IES5507 “line drivers” may be connected to a single bus master (U1), allowing for 32 (8x4) long distance bus pairs to be driven from the one I<sup>2</sup>C port.

Figure 15 shows an alternative solution. In this case, the IES5507 is used to isolate a P82B715 I<sup>2</sup>C bus extender. The P82B715 provides a “10x impedance transformation”<sup>(1)</sup> but does not isolate either side of the buffer. Using the IES5507 to isolate this device greatly simplifies calculation of the pull-ups and increases the total system loading capability in extender applications. Of course, it is possible to connect a P82B715 to each of the four channels, thus allowing a significant drive capability.

The IES5507 may also be driven in series. Figure 16 shows this configuration. In this scenario, each of the four outputs of the first device (U2) has six more IES5507’s connected to it. Each of those six devices has four outputs, thus giving  $4 \times 7 \times 4 = 112$  outputs. If the RESET pin on U2 was also driven from the master, it would be possible to reproduce this entire structure multiple times, giving a truly massive address space capability. Such a configuration may be applied to situations such as display drivers.

(1) P82B715 I2C bus extender datasheet, 2 December 2003, Philips Electronics N.V.

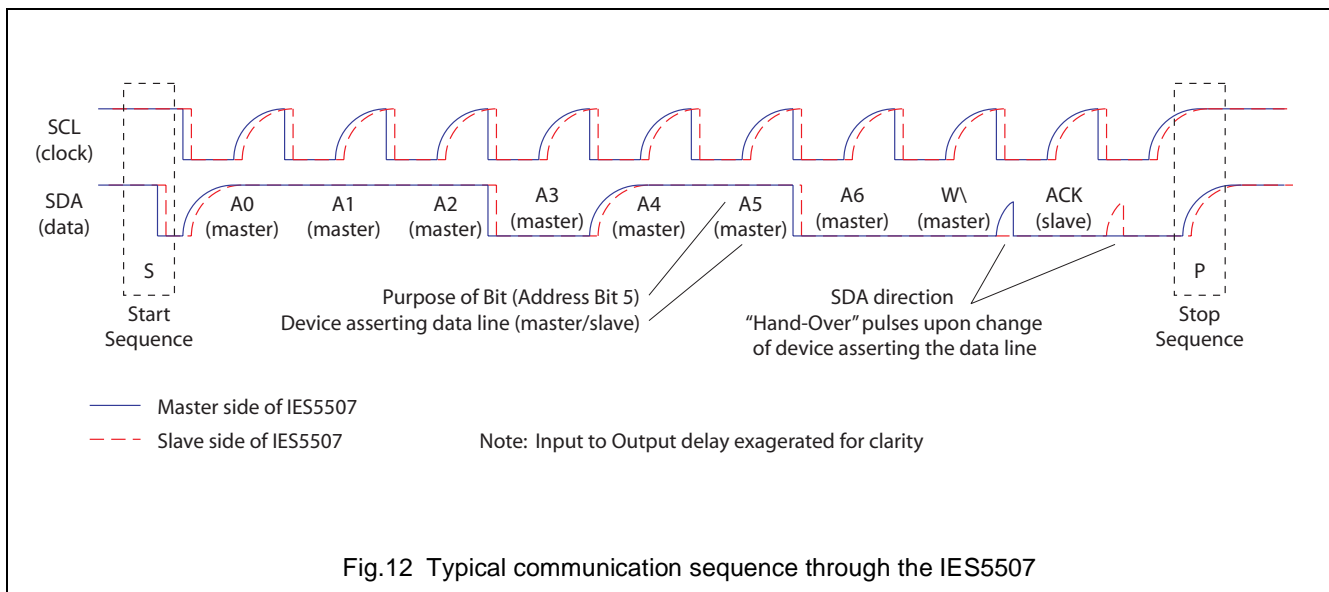
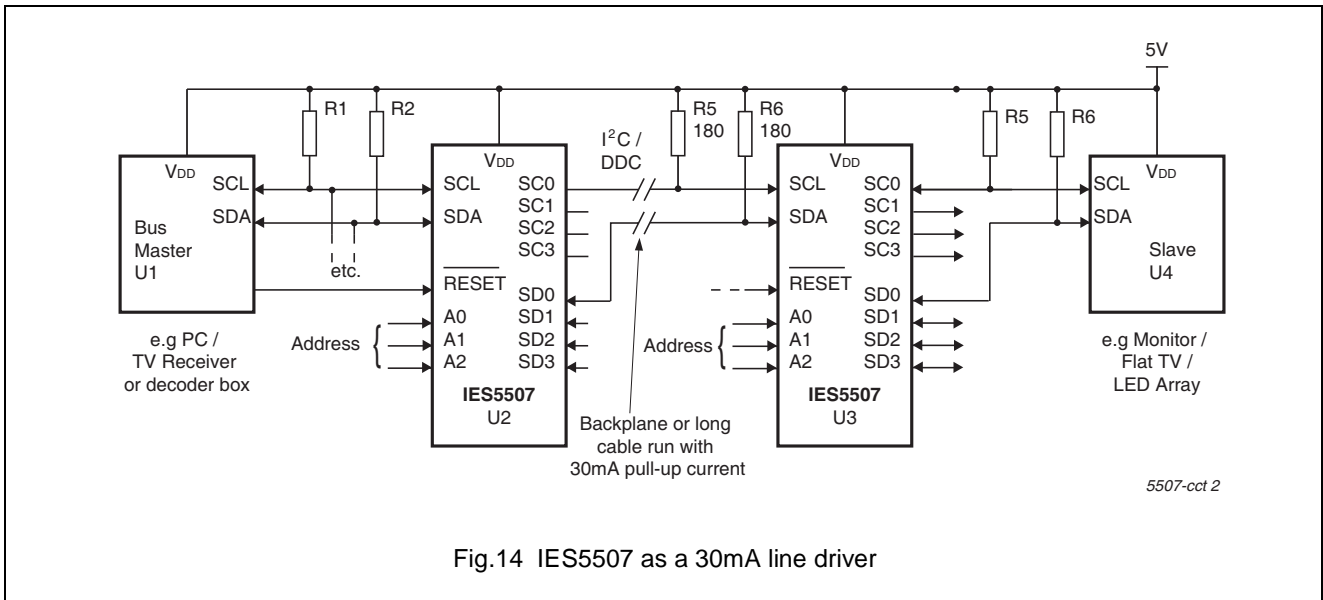
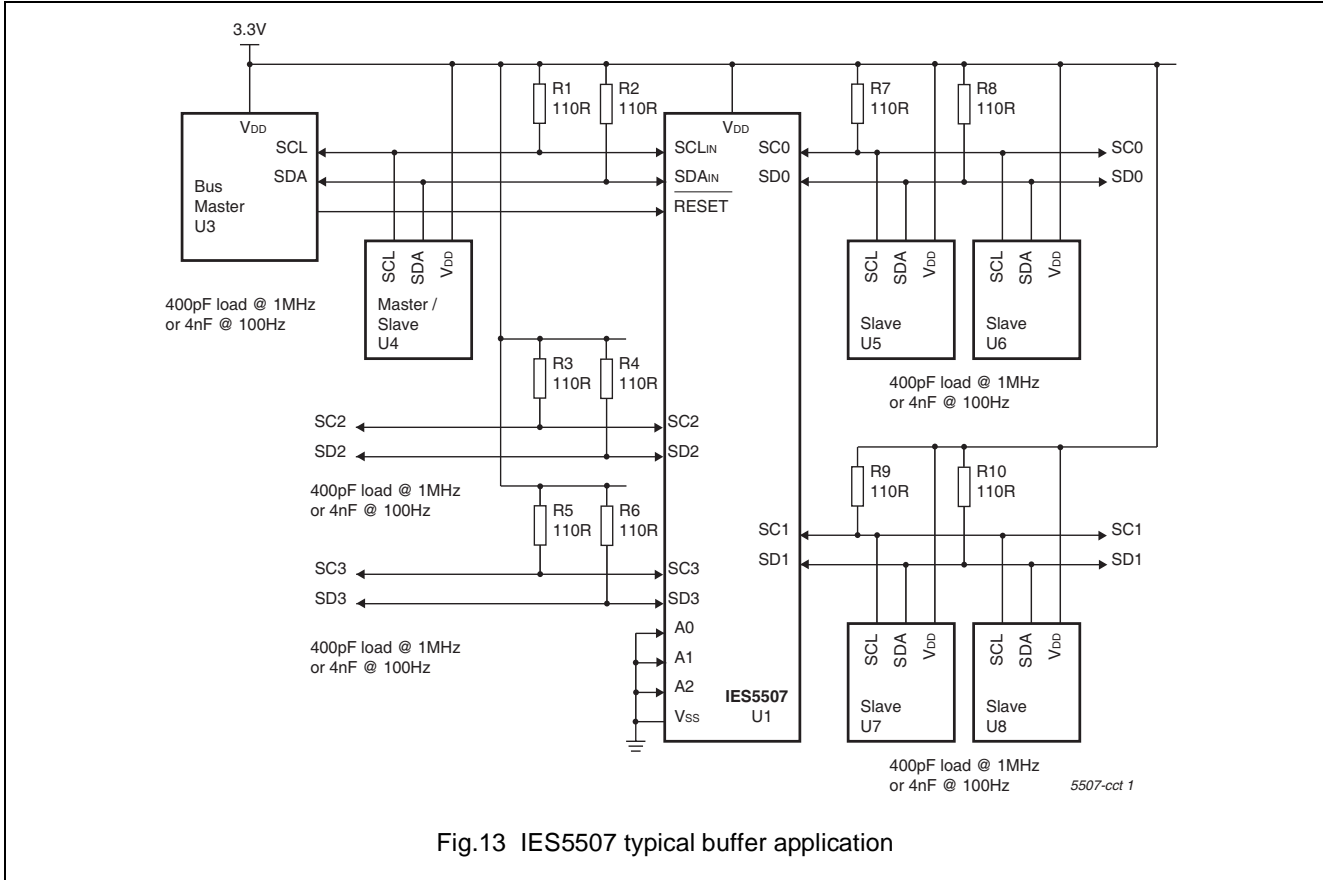
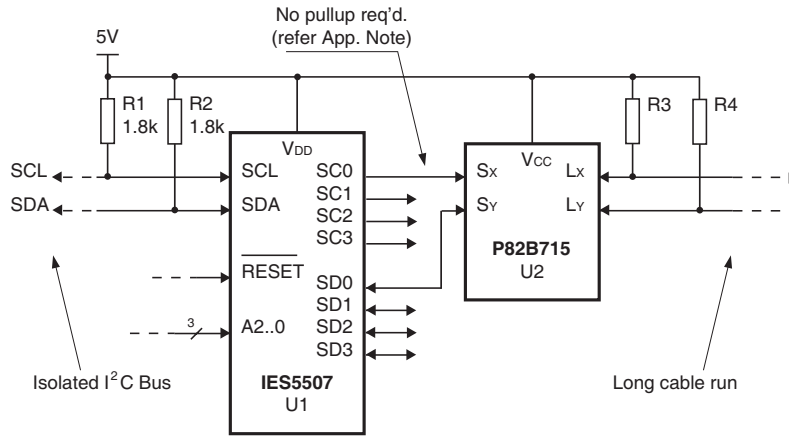


Fig.12 Typical communication sequence through the IES5507



**10.2 Application circuits**

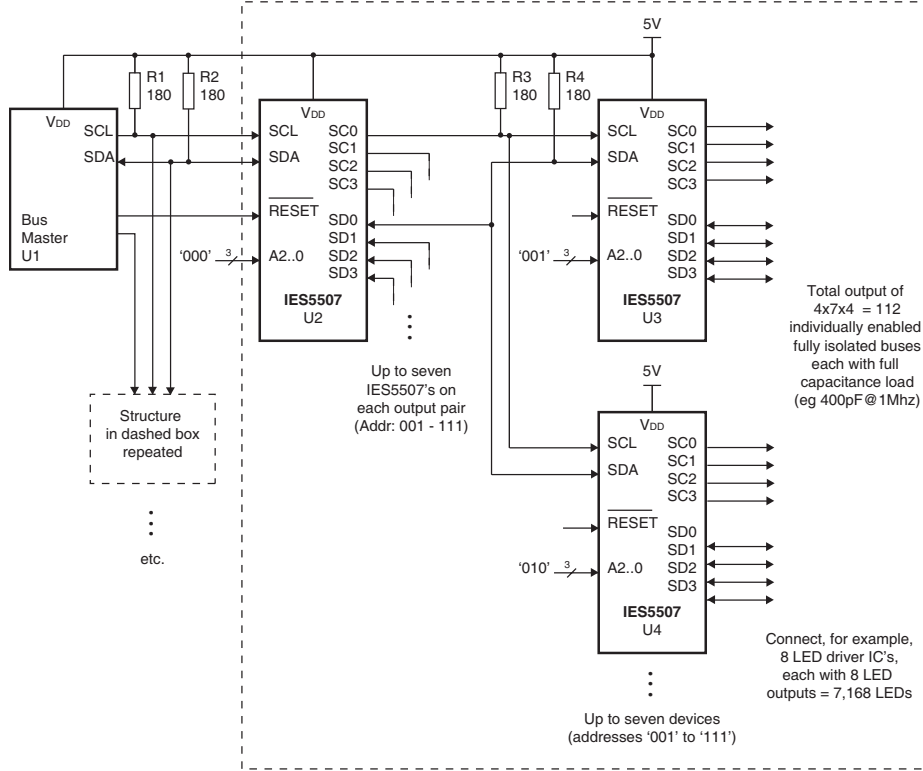




IES5507 provides bus isolation and simplifies calculation of bus RC components

5507-cct 4


Fig.15 IES5507 isolating the standard I<sup>2</sup>C bus from a P82B715 used as a line driver



5507-cct 3

Fig.16 IES5507 series implementation for large I/O fanout

### 11 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5507 T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT162-1	Yes 

Other package options are available - contact Hendon Semiconductors for details. For more information on packages, please refer to the document "Integrated Circuit Packaging and Soldering Information" on the Hendon Semiconductors web site.

### 12 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.



### 13 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
1.0	20090304	Product Release

### 14 DEFINITIONS

<b>Data sheet status</b>	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility. Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

### 15 COMPANY INFORMATION

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