



N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from secondary breakdown
- ► Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- ► High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

| Device | Package Option | BV _{DSS} /BV _{DGS} | R _{DS(ON)} | l _{D(ON)} | |
|--------|----------------|--------------------------------------|---------------------|--------------------|--|
| Device | TO-92 | (V) | (max) (Ω) | (min) (A) | |
| VN0104 | VN0104N3-G | 40 | 3.0 | 2.0 | |

⁻G indicates package is RoHS compliant ('Green')





Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|-------------------|
| Drain-to-source voltage | BV _{DSS} |
| Drain-to-gate voltage | BV _{DGS} |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking



YY = Year Sealed WW = Week Sealed ____ = "Green" Packaging

Package may or may not include the following marks: Si or 🌗

TO-92 (N3)

Distance of 1.6mm from case for 10 seconds.

Thermal Characteristics

| Package | I _D (continuous) [†] (mA) | I _D (pulsed) (A) | Power Dissipation @T _c = 25°C (W) | θ _{jc} (°C/W) | θ _{ja} (°C/W) | l _{DR} † (mA) | l _{DRM} (A) |
|---------|---|-----------------------------------|--|----------------------------------|----------------------------------|---------------------------|-------------------------|
| TO-92 | 350 | 2.0 | 1.0 | 125 | 170 | 350 | 2.0 |

Notes:

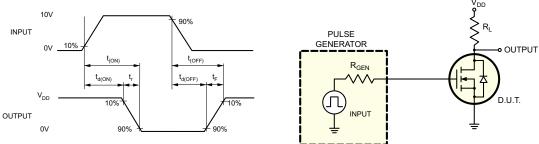
Electrical Characteristics (T_A = 25°C unless otherwise specified)

| Sym | Parameter | Min | Тур | Max | Units | Conditions | |
|----------------------------|--|-----|------|------|-------|--|--|
| BV _{DSS} | Drain-to-source breakdown voltage | 40 | - | - | V | $V_{GS} = 0V, I_{D} = 1.0 \text{mA}$ | |
| $V_{\rm GS(th)}$ | Gate threshold voltage | 0.8 | ı | 2.4 | V | $V_{GS} = V_{DS}$, $I_D = 1.0 \text{mA}$ | |
| $\Delta V_{\text{GS(th)}}$ | Change in V _{GS(th)} with temperature | - | -3.8 | -5.5 | mV/°C | $V_{GS} = V_{DS}$, $I_{D} = 1.0$ mA | |
| I _{GSS} | Gate body leakage | - | - | 100 | nA | $V_{GS} = \pm 20V, V_{DS} = 0V$ | |
| | | - | - | 1.0 | | $V_{GS} = 0V, V_{DS} = Max Rating$ | |
| l _{DSS} | Zero gate voltage drain current | - | - | 100 | μA | $V_{DS} = 0.8$ Max Rating, $V_{GS} = 0V$, $T_{A} = 125$ °C | |
| | On state drain current | 0.5 | 1.0 | - | Α | $V_{GS} = 5.0V, V_{DS} = 25V$ | |
| D(ON) | On-state drain current | | 2.5 | - | | $V_{GS} = 10V, V_{DS} = 25V$ | |
| D | Static drain-to-source on-state resistance | - | 3.0 | 5.0 | Ω | $V_{GS} = 5.0V, I_{D} = 250mA$ | |
| R _{DS(ON)} | Static drain-to-source on-state resistance | | 2.5 | 3.0 | 22 | $V_{GS} = 10V, I_{D} = 1.0A$ | |
| $\Delta R_{DS(ON)}$ | Change in R _{DS(ON)} with temperature | - | 0.70 | 1.0 | %/°C | $V_{GS} = 10V, I_{D} = 1.0A$ | |
| G _{FS} | Forward transductance | 300 | 450 | - | mmho | $V_{DS} = 25V, I_{D} = 500mA$ | |
| C _{ISS} | Input capacitance | - | 55 | 65 | | V _{GS} = 0V, | |
| C _{oss} | Common source output capacitance | - | 20 | 25 | pF | $V_{DS} = 25V$, | |
| C _{RSS} | Reverse transfer capacitance | - | 5.0 | 8.0 | | f = 1.0MHz | |
| t _{d(ON)} | Turn-on delay time | - | 3.0 | 5.0 | | | |
| t _r | Rise time Turn-off delay time | | 5.0 | 8.0 | ns | $V_{DD} = 25V,$ $I_{D} = 1.0A,$ $R_{GEN} = 25\Omega$ | |
| t _{d(OFF)} | | | 6.0 | 9.0 | | | |
| t _f | Fall time | - | 5.0 | 8.0 | | OLIY | |
| V _{SD} | Diode forward voltage drop | - | 1.2 | 1.8 | V | $V_{GS} = 0V, I_{SD} = 1.0A$ | |
| t _{rr} | Reverse recovery time | - | 400 | - | ns | $V_{GS} = 0V, I_{SD} = 1.0A$ | |

Notes:

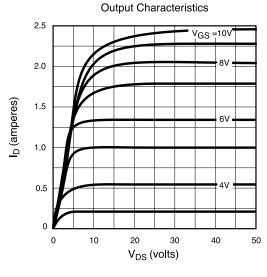
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

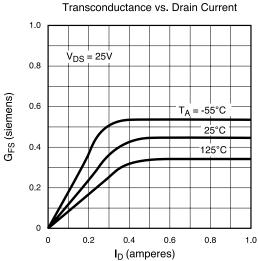
Switching Waveforms and Test Circuit

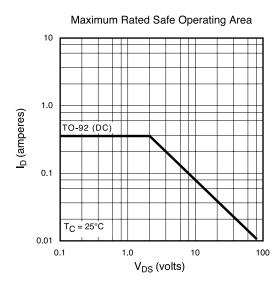


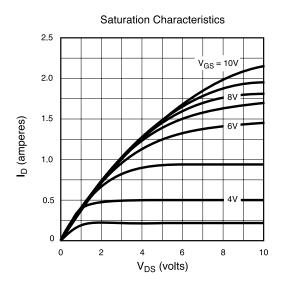
[†] I_D (continuous) is limited by max rated T_i .

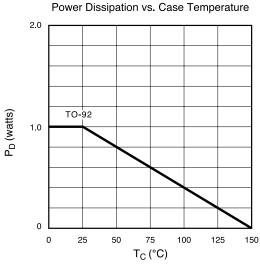
Typical Performance Curves

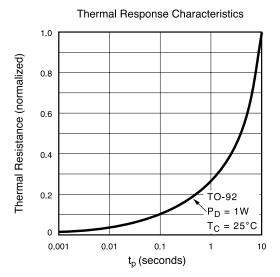




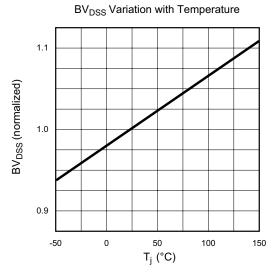


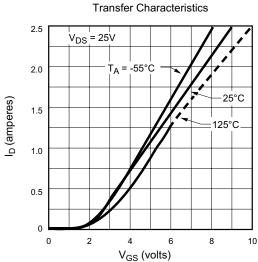


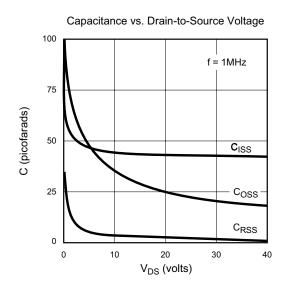


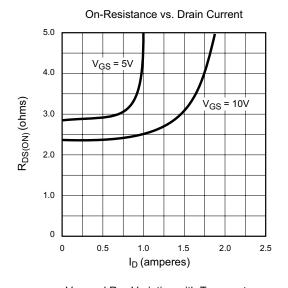


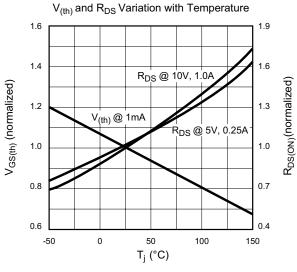
Typical Performance Curves (cont.)

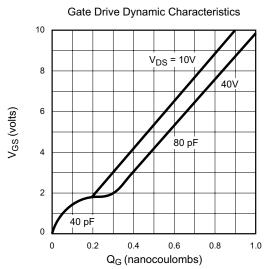




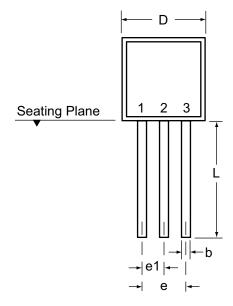


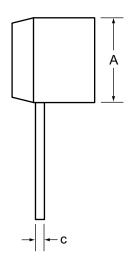






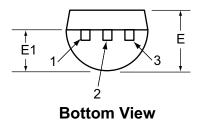
3-Lead TO-92 Package Outline (N3)





Front View

Side View



| Symbol | | Α | b | С | D | E | E1 | е | e1 | L |
|---------------------|-----|------|-------------------|-------------------|------|------|------|------|------|-------|
| Dimensions (inches) | MIN | .170 | .014 [†] | .014 [†] | .175 | .125 | .080 | .095 | .045 | .500 |
| | NOM | - | - | - | - | - | - | - | - | - |
| | MAX | .210 | .022 [†] | .022 [†] | .205 | .165 | .105 | .105 | .055 | .610* |

JEDEC Registration TO-92.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. website: http://www.supertex.com.

©2009 **Supertex inc.** All rights reserved. Unauthorized use or reproduction is prohibited.

Supertex inc.

^{*} This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

[†] This dimension is a non-JEDEC dimension.