Complementary 20 V (D-S) Low-Threshold MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.280 at V_{GS} = 4.5 V	1.28
		0.360 at V_{GS} = 2.5 V	1.13
		0.450 at V_{GS} = 1.8 V	1.0
P-Channel	- 20	0.490 at V_{GS} = - 4.5 V	- 1.0
		0.750 at V_{GS} = - 2.5 V	- 0.81
		1.10 at V_{GS} = - 1.8 V	- 0.67

FEATURES

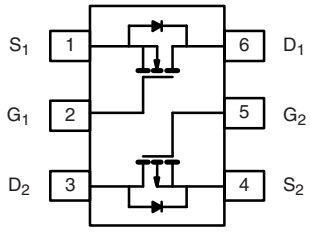
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETS: 1.8 V Rated
- ESD Protected: 2000 V
- Thermally Enhanced SC-70 Package
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

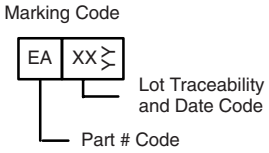
APPLICATIONS

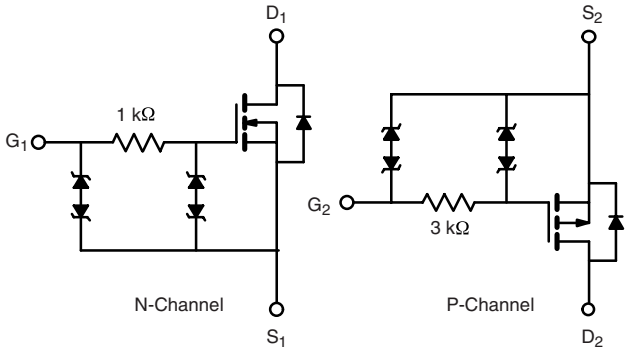
- Load Switching
- PA Switch
- Level Switch

SOT-363
SC-70 (6-LEADS)



Top View





Ordering Information: Si1563EDH-T1-E3 (Lead (Pb)-free)
Si1563EDH-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted							
			N-Channel		P-Channel		
Parameter		Symbol	5 s	Steady State	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		- 20		V
Gate-Source Voltage		V_{GS}	± 12		± 12		
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	1.28	1.13	- 1.0	- 0.88	A
	T_A = 85 °C		0.92	0.81	- 0.72	- 0.63	
Pulsed Drain Current		I_{DM}	4.0		- 3.0		
Continuous Source Current (Diode Conduction)[a]		I_S	0.61	0.48	- 0.61	- 0.48	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	0.74	0.57	0.30	0.57	W
	T_A = 85 °C		0.38	0.30	0.16	0.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	130	170	°C/W
	Steady State		170	220	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	80	100	

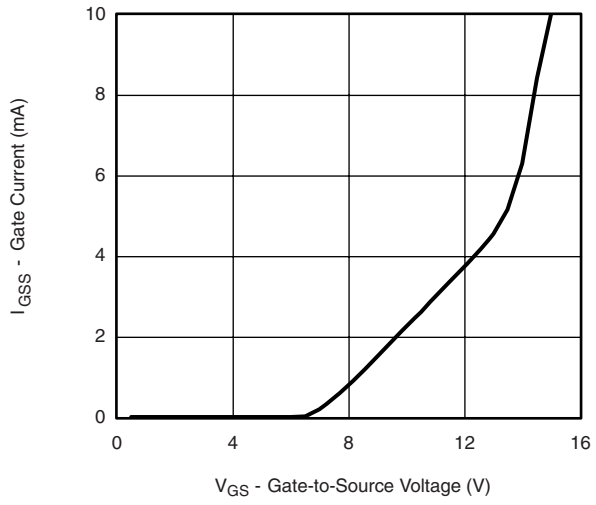
Notes:
a. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 100 µA	N-Ch	0.45			V
		V_{DS} = V_{GS}, I_D = - 100 µA	P-Ch	- 0.45			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	N-Ch			± 1	µA
			P-Ch			± 1	
		V_{DS} = 0 V, V_{GS} = ± 12 V	N-Ch			± 10	mA
			P-Ch			± 10	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 16 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 16 V, V_{GS} = 0 V, T_J = 85 °C	N-Ch			5	
		V_{DS} = - 16 V, V_{GS} = 0 V, T_J = 85 °C	P-Ch			- 5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	2			A
		V_{DS} ≤ - 5 V, V_{GS} = - 4.5 V	P-Ch	- 2			
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 1.13 A	N-Ch		0.220	0.280	Ω
		V_{GS} = - 4.5 V, I_D = - 0.88 A	P-Ch		0.400	0.490	
		V_{GS} = 2.5 V, I_D = 0.99 A	N-Ch		0.281	0.360	
		V_{GS} = - 2.5 V, I_D = - 0.71 A	P-Ch		0.610	0.750	
		V_{GS} = 1.8 V, I_D = 0.20 A	N-Ch		0.344	0.450	
		V_{GS} = - 1.8 V, I_D = - 0.20 A	P-Ch		0.850	1.10	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 1.13 A	N-Ch		2.6		S
		V_{DS} = - 10 V, I_D = - 0.88 A	P-Ch		1.5		
Diode Forward Voltage[a]	V_{SD}	I_S = 0.48 V, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = - 0.48 V, V_{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 1.13 A P-Channel V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 0.88 A	N-Ch		0.65	1.0	nC
			P-Ch		1.2	1.8	
Gate-Source Charge	Q_{gs}		N-Ch		0.2		
			P-Ch		0.3		
Gate-Drain Charge	Q_{gd}		N-Ch		0.23		
			P-Ch		0.3		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 20 Ω I_D ≅ 0.5 A, V_{GEN} = 4.5 V, R_g = 6 Ω P-Channel V_{DD} = - 10 V, R_L = 20 Ω I_D ≅ - 0.5 A, V_{GEN} = - 4.5 V, R_g = 6 Ω	N-Ch		45	70	ns
			P-Ch		150	230	
Rise Time	t_r		N-Ch		85	130	
			P-Ch		480	720	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		350	530	
			P-Ch		840	1200	
Fall Time	t_f		N-Ch		210	320	
			P-Ch		850	1200	

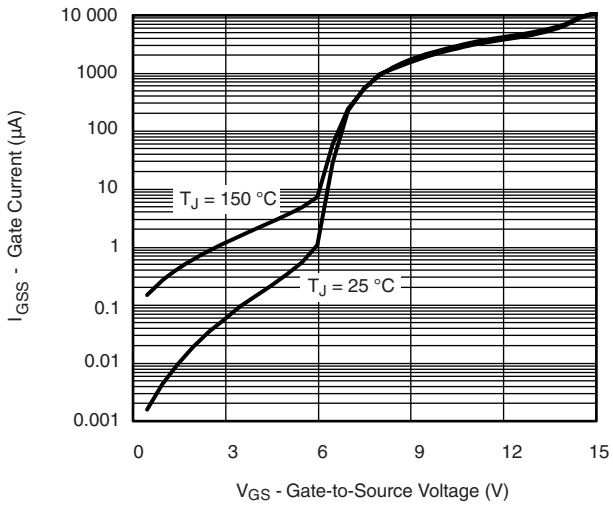
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

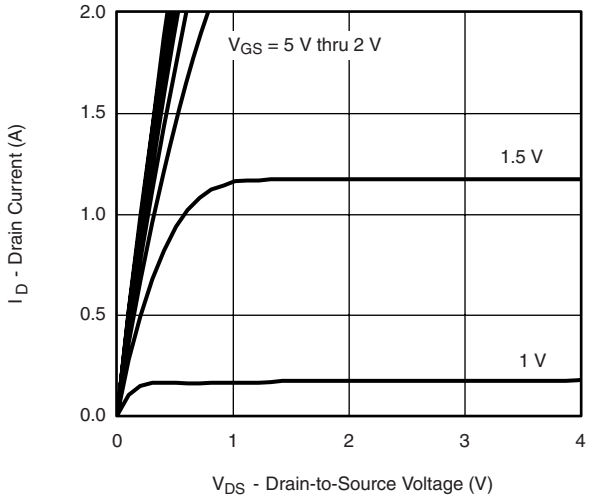
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



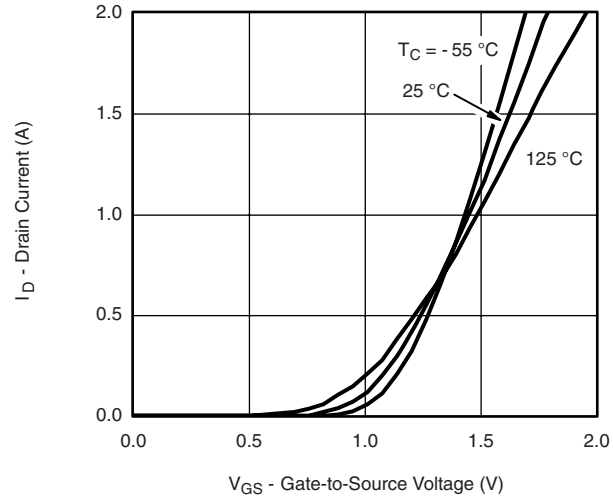
Gate-Current vs. Gate-Source Voltage



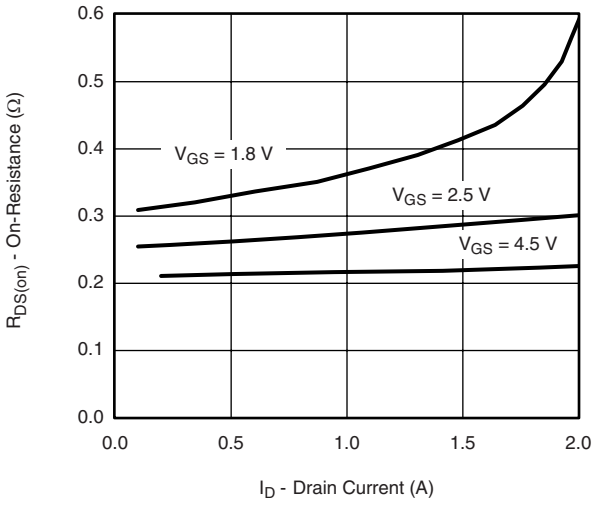
Gate-Current vs. Gate-Source Voltage



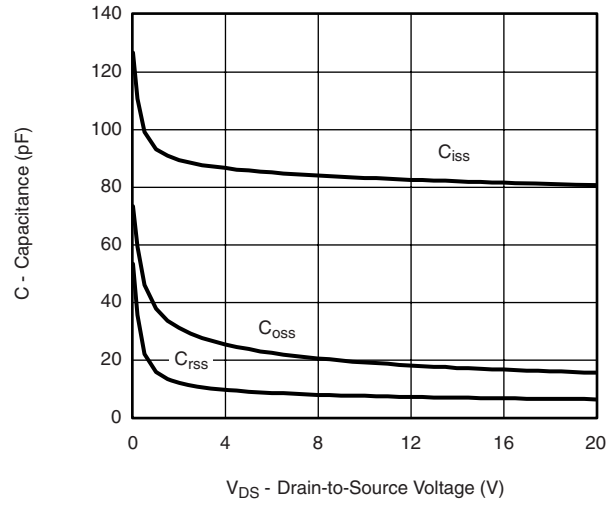
Output Characteristics



Transfer Characteristics

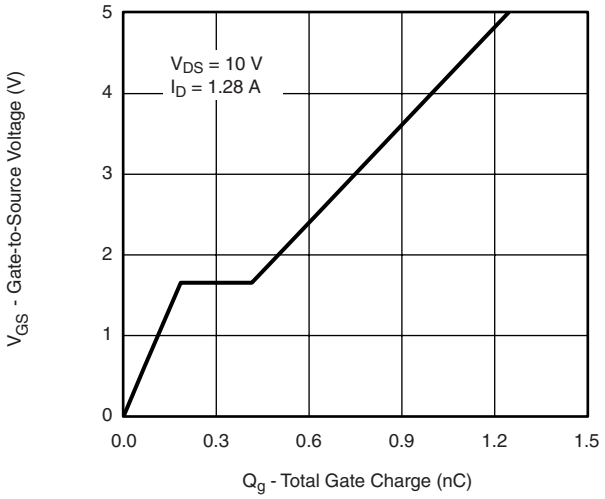


On-Resistance vs. Drain Current

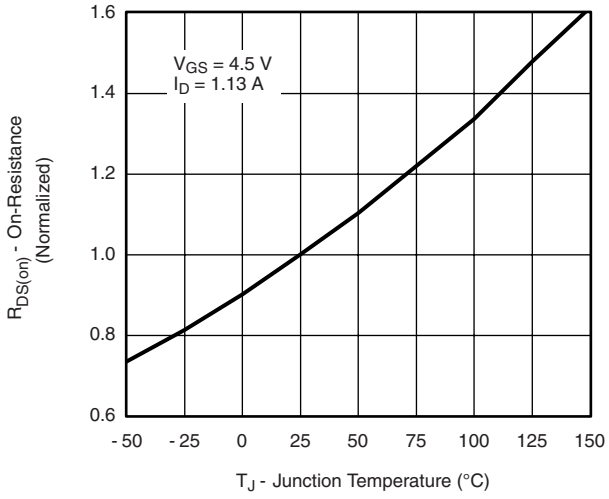


Capacitance

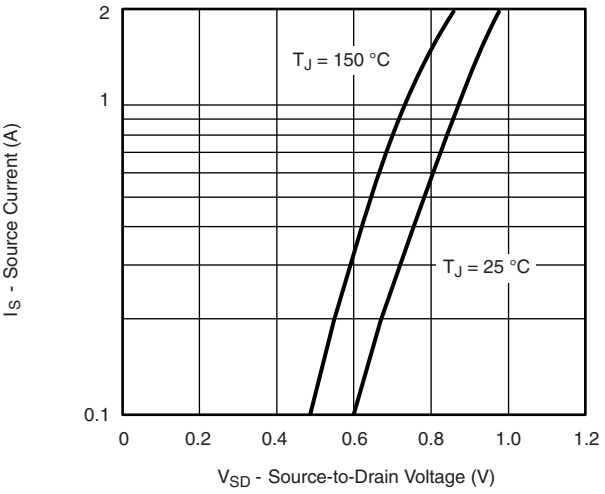
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



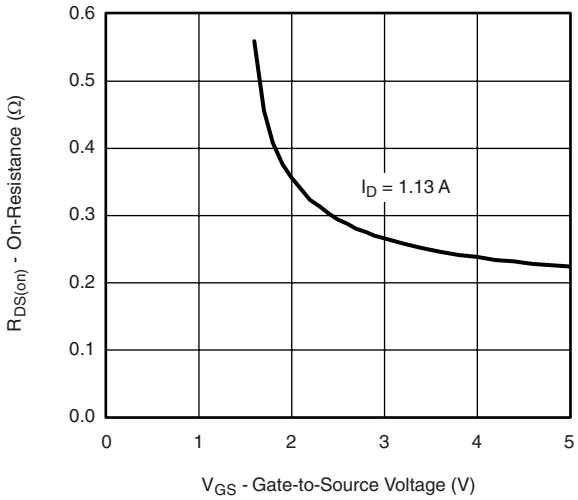
Gate Charge



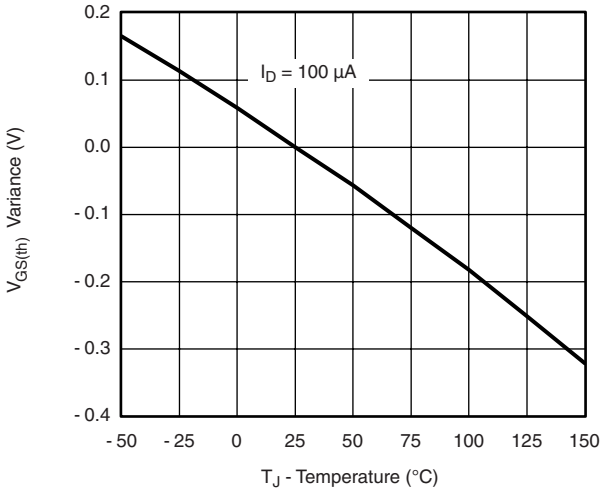
On-Resistance vs. Junction Temperature



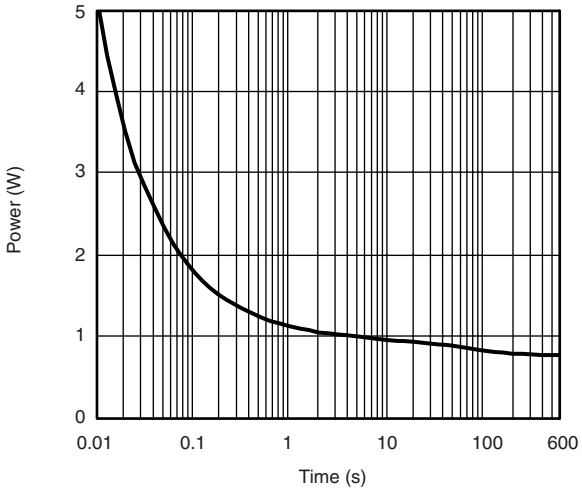
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

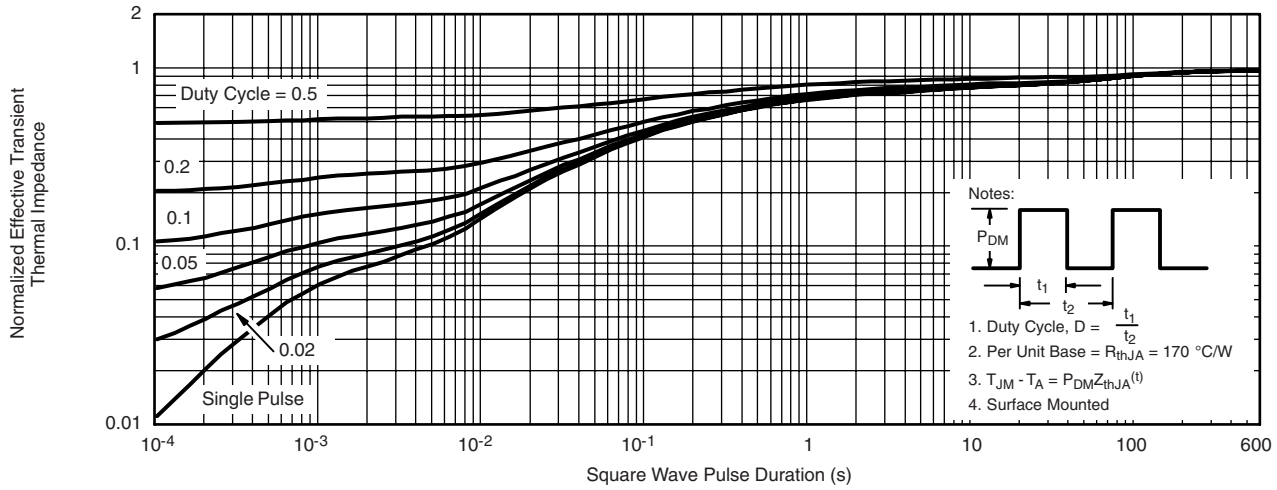


Threshold Voltage

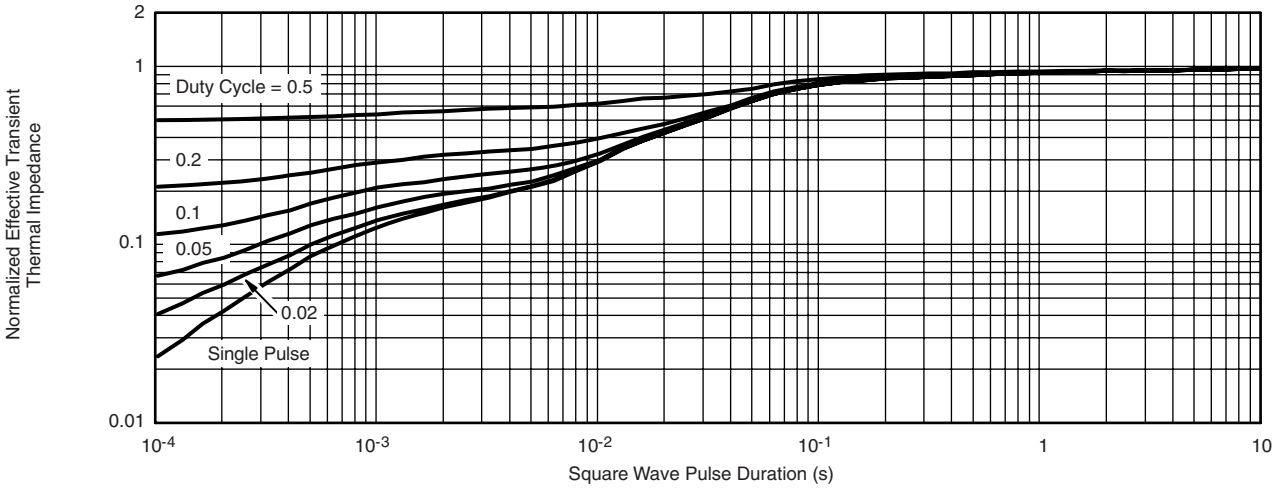


Single Pulse Power, Junction-to-Ambient

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

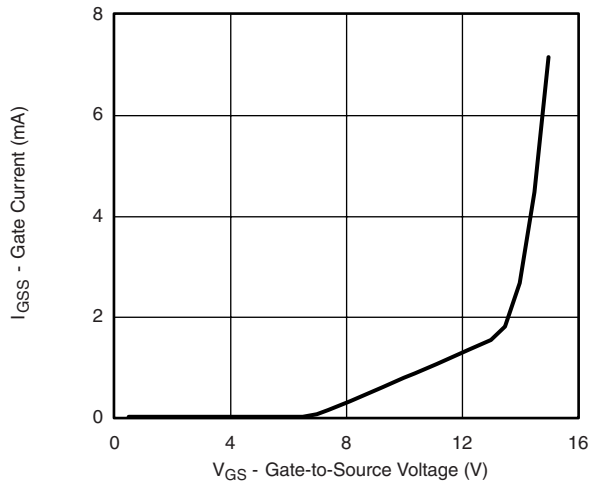


Normalized Thermal Transient Impedance, Junction-to-Ambient

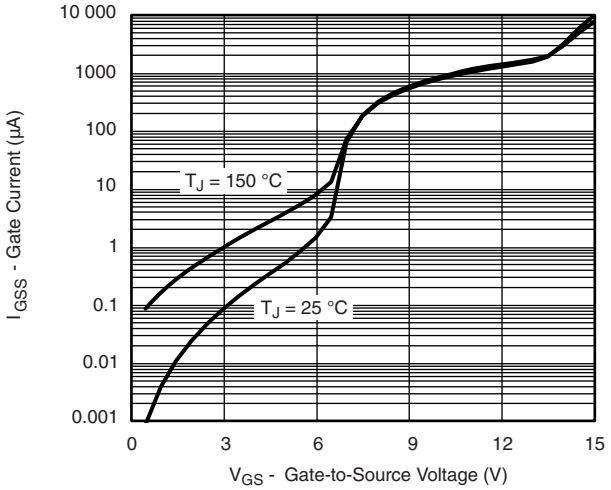


Normalized Thermal Transient Impedance, Junction-to-Foot

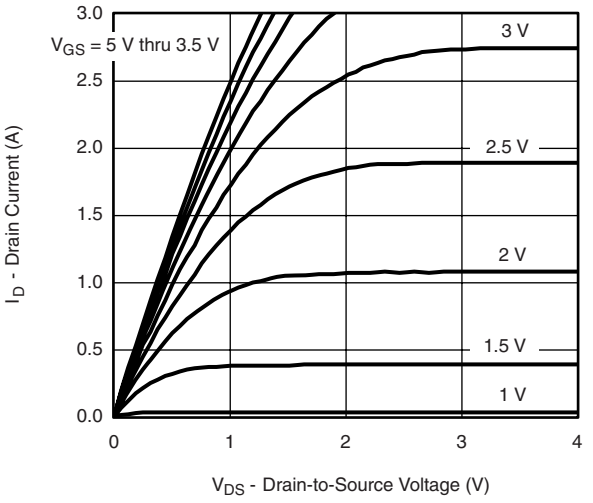
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



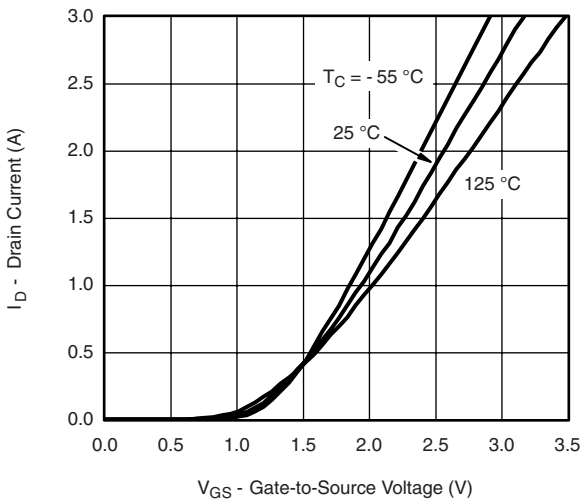
Gate-Current vs. Gate-Source Voltage



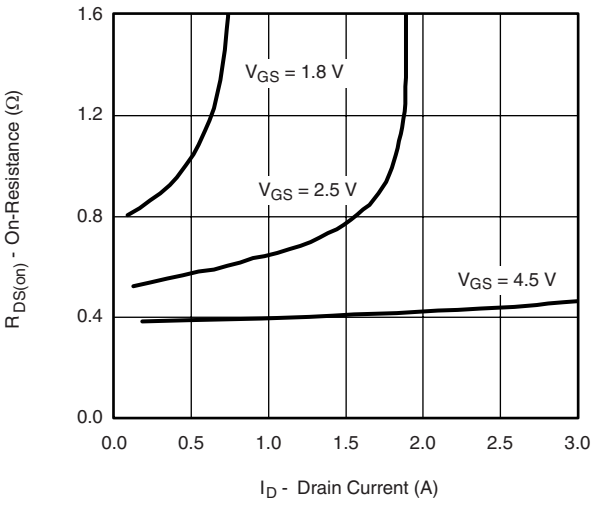
Gate-Current vs. Gate-Source Voltage



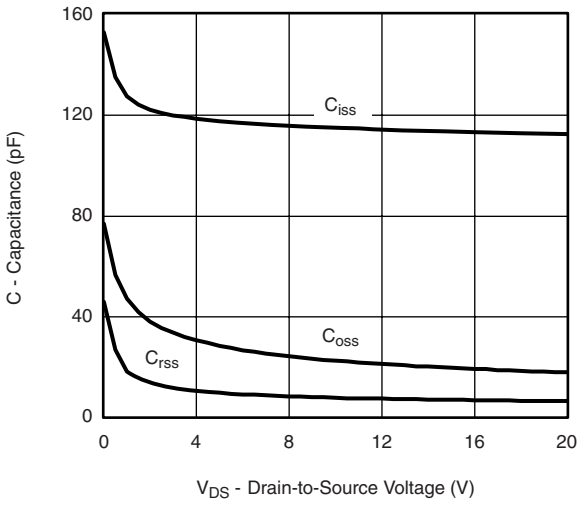
Output Characteristics



Transfer Characteristics

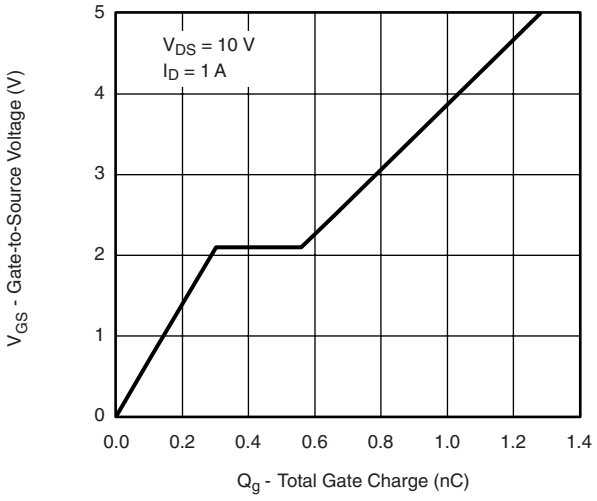


On-Resistance vs. Drain Current

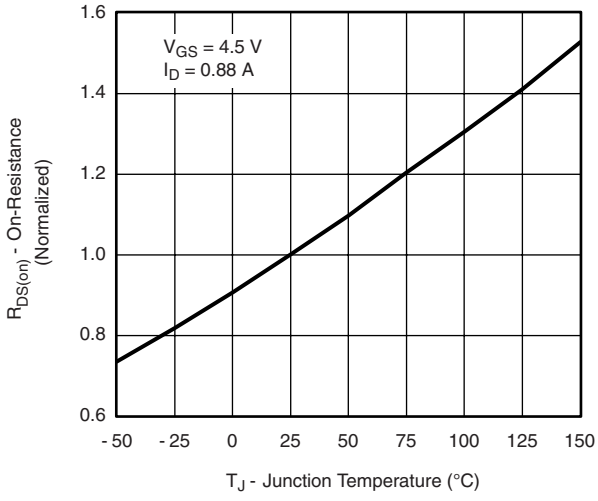


Capacitance

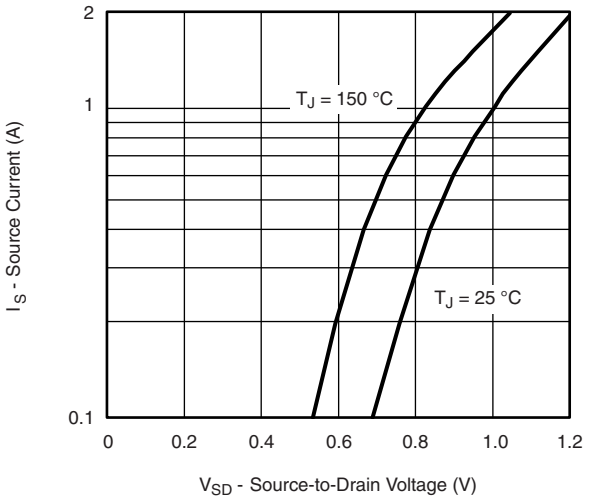
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



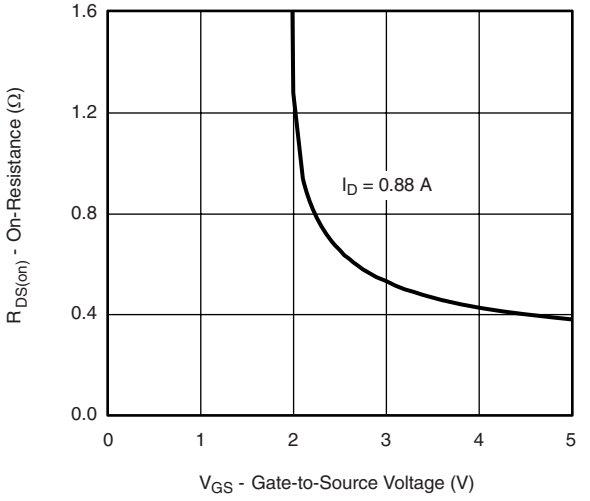
Gate Charge



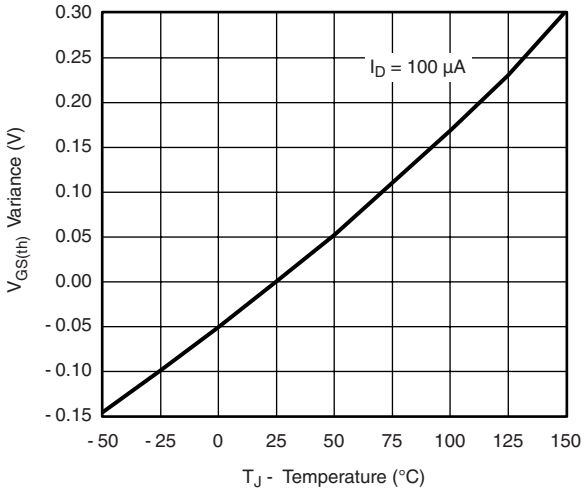
On-Resistance vs. Junction Temperature



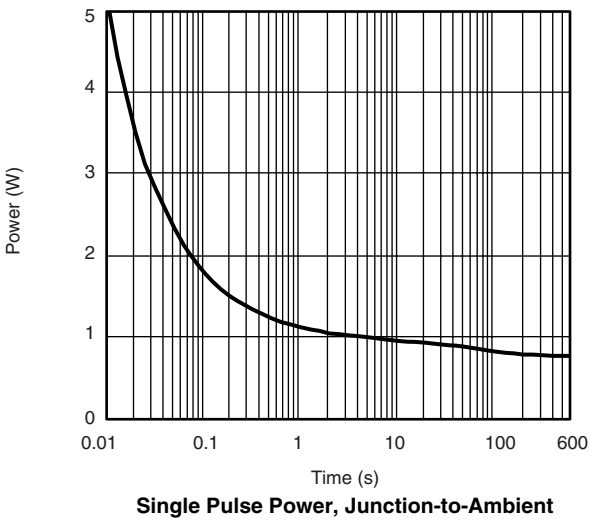
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

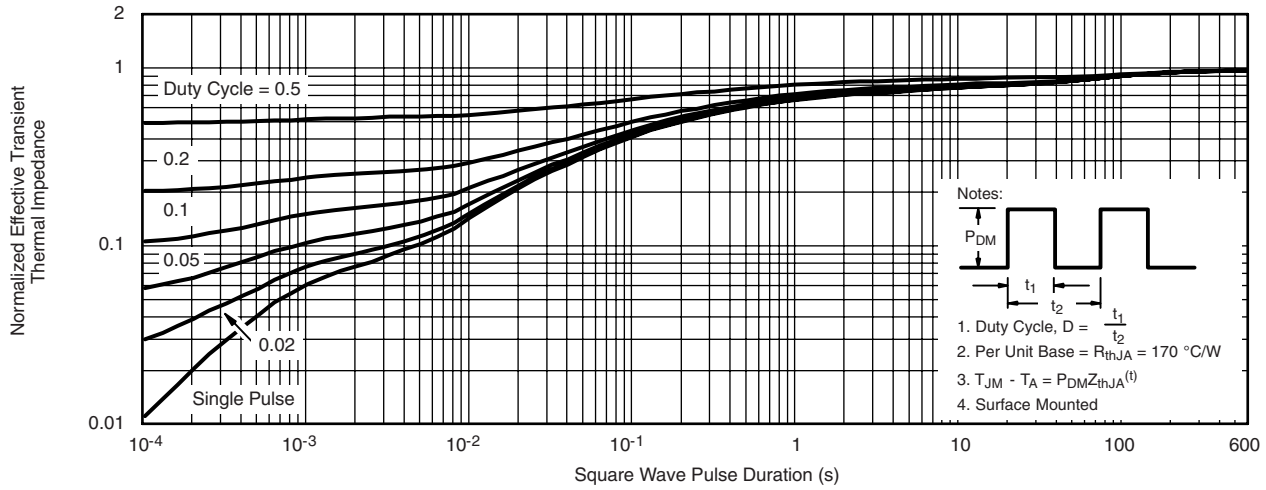


Threshold Voltage

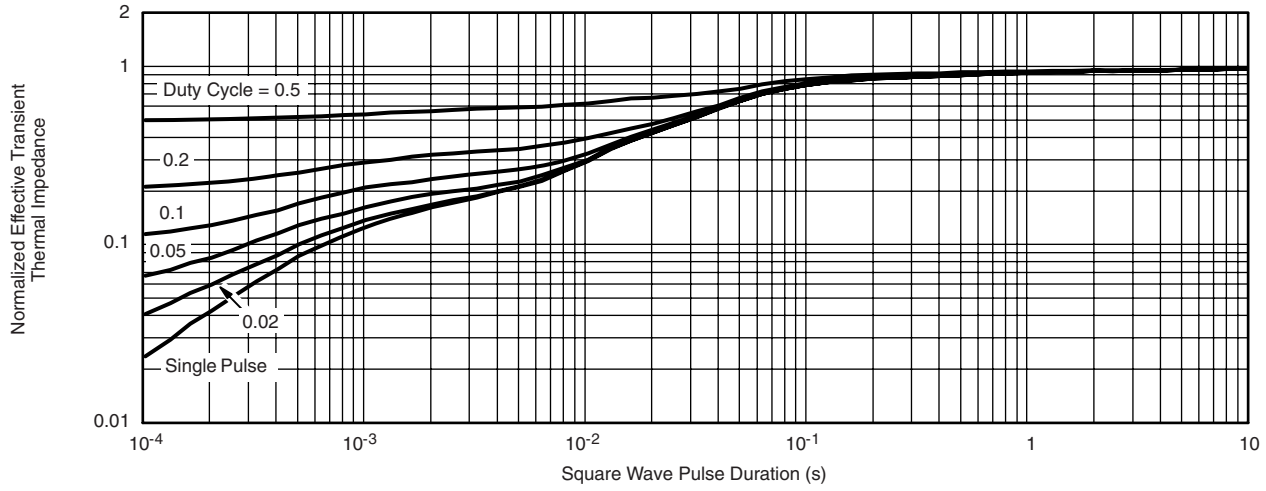


Single Pulse Power, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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