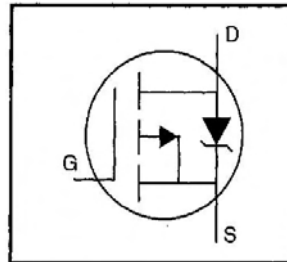


# IRFD9210PbF

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling
- Lead-Free

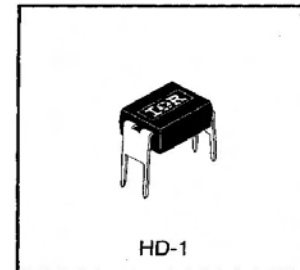


$V_{DSS} = -200V$
$R_{DS(on)} = 3.0\Omega$
$I_D = -0.40A$

## Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-0.40	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-0.25	
$I_{DM}$	Pulsed Drain Current ①	-3.2	
$P_D @ T_C = 25^\circ C$	Power Dissipation	1.0	W
	Linear Derating Factor	0.0083	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	210	mJ
$I_{AR}$	Avalanche Current ①	-0.40	A
$E_{AR}$	Repetitive Avalanche Energy ①	0.10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

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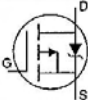
# IRFD9210PbF

International  
 Rectifier

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

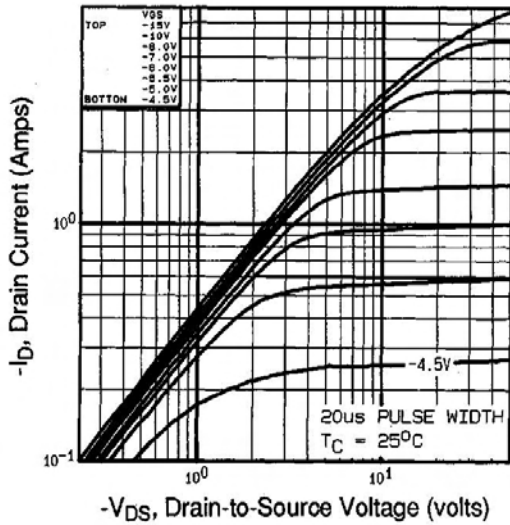
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-200	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.23	—	V/°C	Reference to 25°C, I <sub>D</sub> =-1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V <sub>GS</sub> =-10V, I <sub>D</sub> =-0.24A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
g <sub>fs</sub>	Forward Transconductance	0.27	—	—	S	V <sub>DS</sub> =-50V, I <sub>D</sub> =-0.24A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-100	μA	V <sub>DS</sub> =-200V, V <sub>GS</sub> =0V
		—	—	-500		V <sub>DS</sub> =-160V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> =-20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> =20V
Q <sub>g</sub>	Total Gate Charge	—	—	8.9	nC	I <sub>D</sub> =-1.3A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	2.1		V <sub>DS</sub> =-160V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	3.9		V <sub>GS</sub> =-10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.0	—	ns	V <sub>DD</sub> =-100V
t <sub>r</sub>	Rise Time	—	12	—		I <sub>D</sub> =-2.3A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	11	—		R <sub>G</sub> =24Ω
t <sub>f</sub>	Fall Time	—	13	—		R <sub>D</sub> =41Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	6.0	—		
C <sub>iss</sub>	Input Capacitance	—	170	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	54	—		V <sub>DS</sub> =-25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	16	—		f=1.0MHz See Figure 5

## Source-Drain Ratings and Characteristics

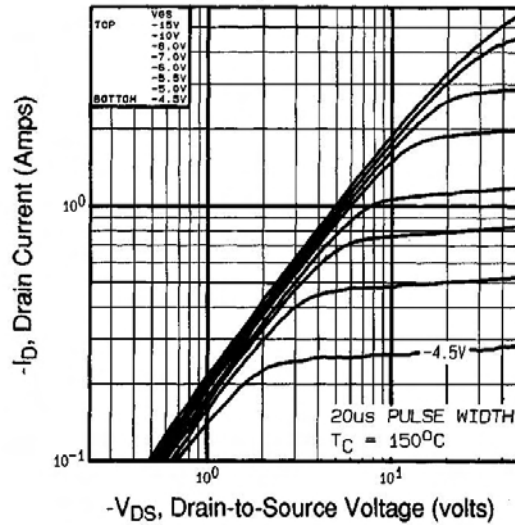
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-0.40	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-3.2		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-5.8	V	T <sub>J</sub> =25°C, I <sub>S</sub> =-0.40A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	110	220	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =-2.3A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.56	1.1	μC	di/dt=100A/μs ④

### Notes:

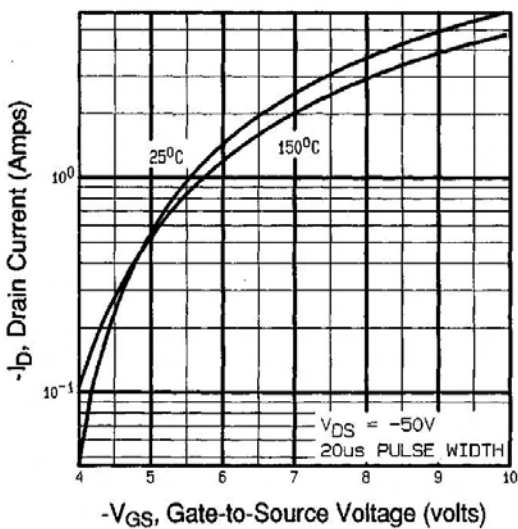
- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=-50V, starting T<sub>J</sub>=25°C, L=123mH R<sub>G</sub>=25Ω, I<sub>AS</sub>=-1.6A (See Figure 12)
- ③ I<sub>SD</sub>≤-2.3A, di/dt≤70A/μs, V<sub>DD</sub>≤V<sub>(BR)DSS</sub>, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.



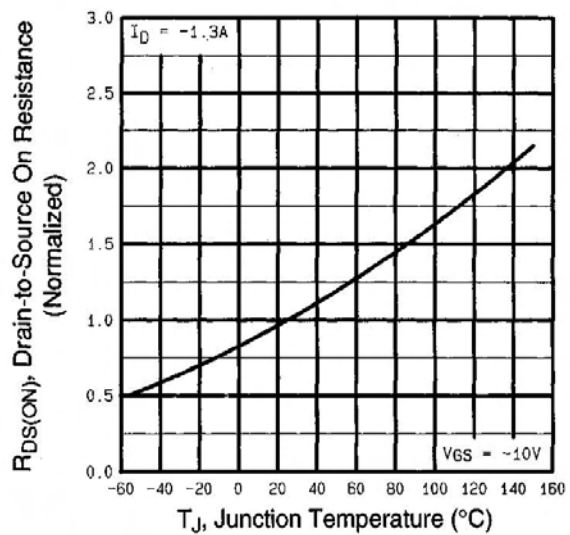
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=150^\circ\text{C}$

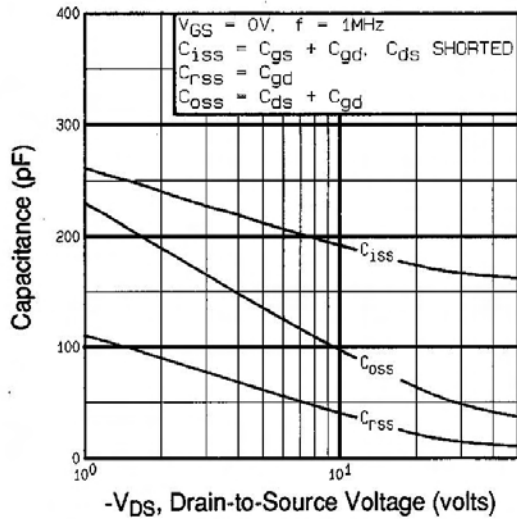


**Fig 3.** Typical Transfer Characteristics

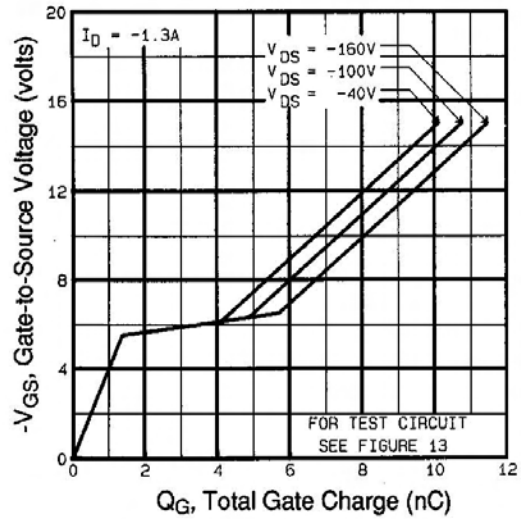


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

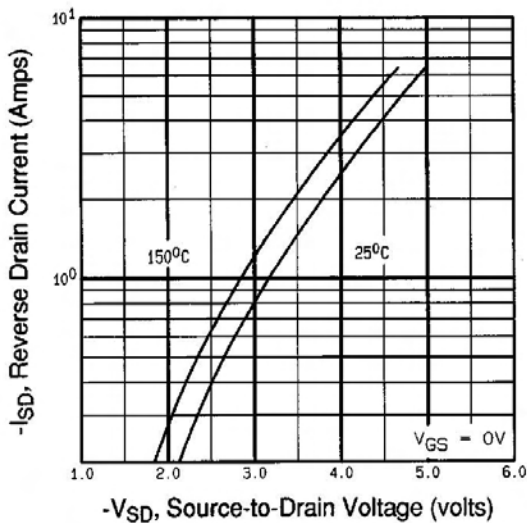
# IRFD9210PbF



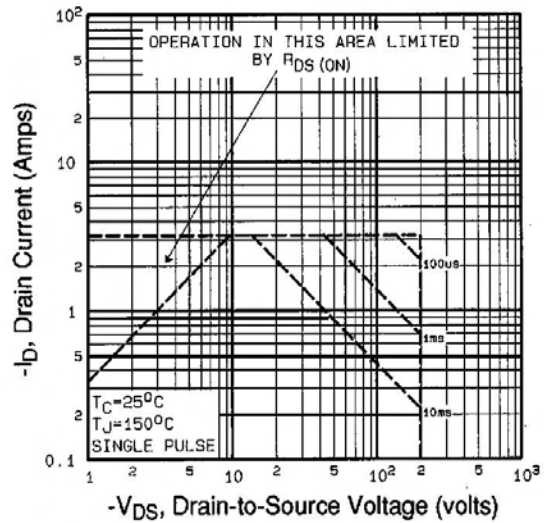
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



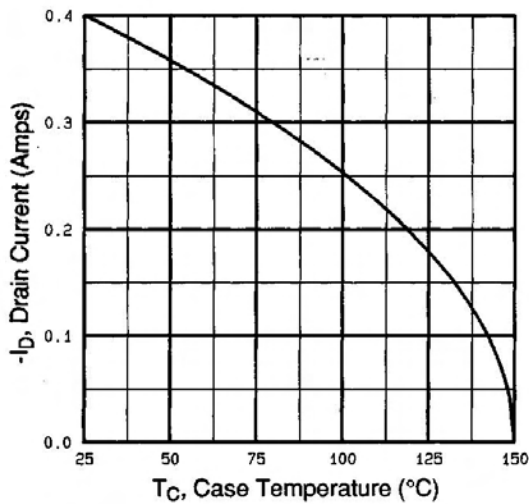
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



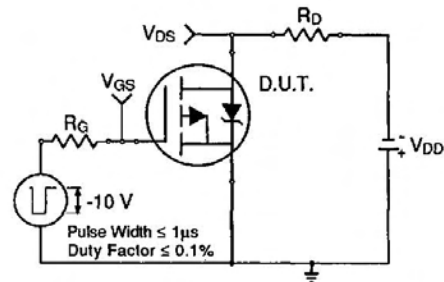
**Fig 7.** Typical Source-Drain Diode Forward Voltage



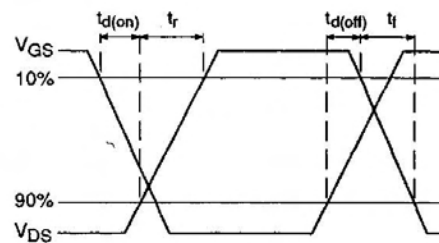
**Fig 8.** Maximum Safe Operating Area



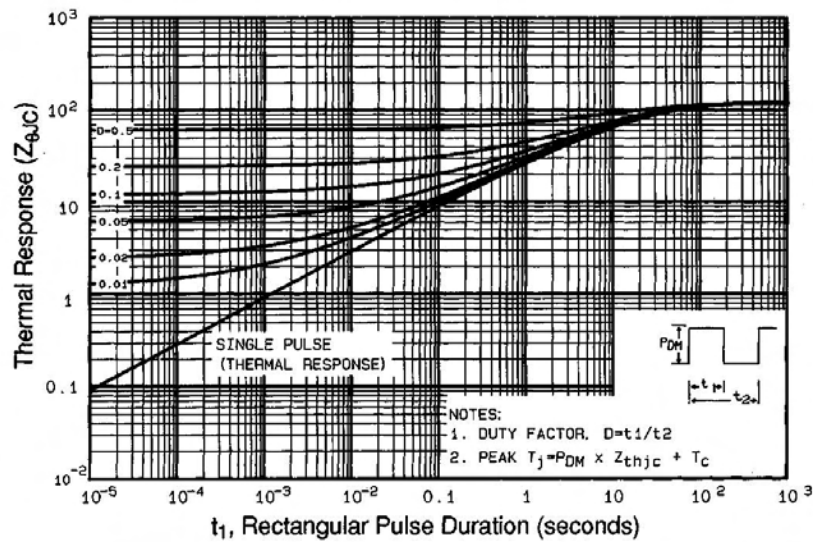
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

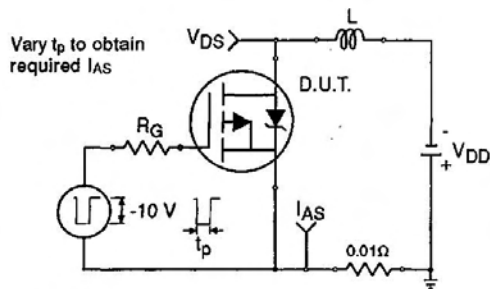


**Fig 10b.** Switching Time Waveforms

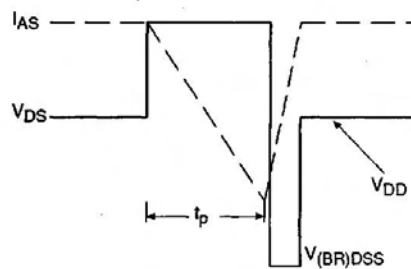


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

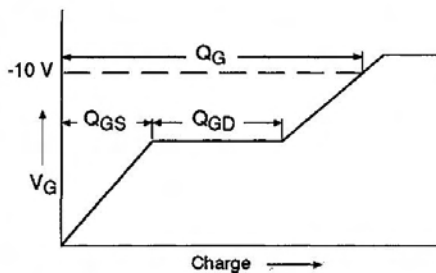
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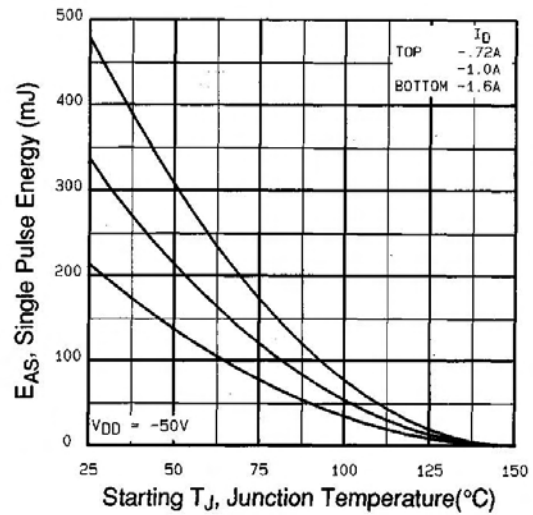
**Fig 12a.** Unclamped Inductive Test Circuit



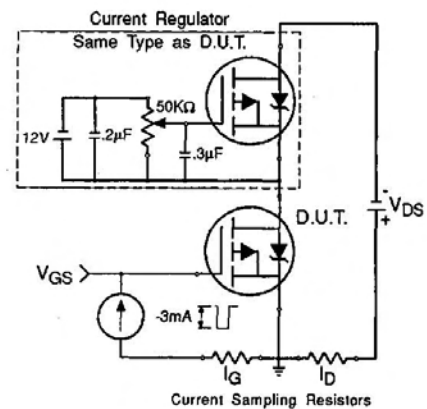
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

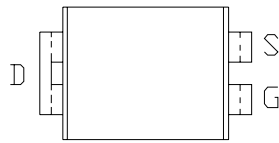


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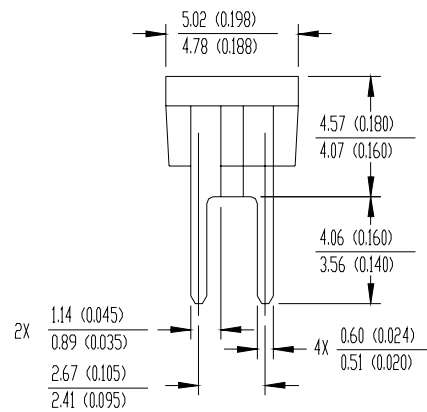
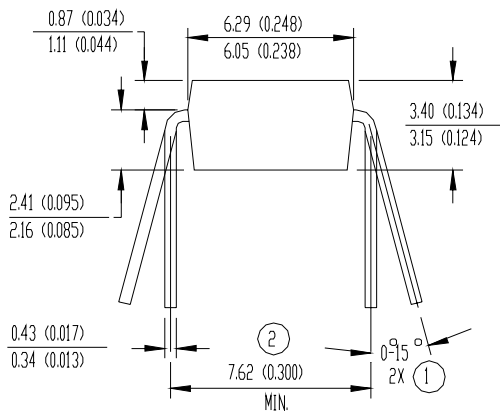
## Hexdip Package Outline

Dimensions are shown in millimeters (inches)



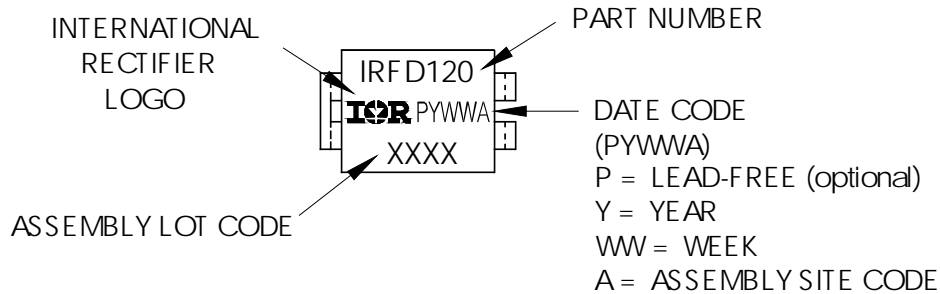
NOTES:

- ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
- ② APPLIES TO INSTALLED LEAD CENTERS
- 3 CONTROLLING DIMENSION: INCH.
- 4 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
- 5 CASE STYLE HD-1 (SIMILAR TO JEDEC OUTLINE MO-001AN)
- 6 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP  
SOLDER DIP MAX. + 0.16 (0.006)



## Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120



Data and specifications subject to change without notice.



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10/04

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