

Complementary MOSFET Half-Bridge (N- and P-Channel)

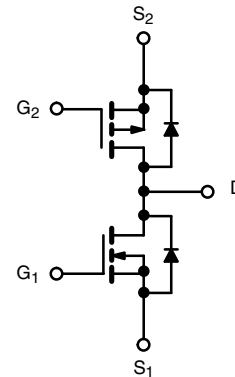
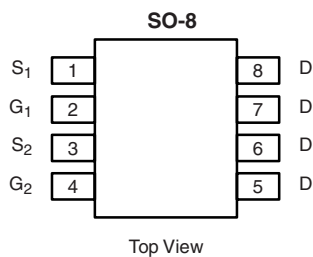
PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.020 at V _{GS} = 4.5 V	9.1
		0.030 at V _{GS} = 2.5 V	7.5
P-Channel	- 20	0.060 at V _{GS} = - 4.5 V	- 5.3
		0.100 at V _{GS} = - 2.5 V	- 4.1

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



Ordering Information: Si4500BDY-T1-E3 (Lead (Pb)-free)
Si4500BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 s	Steady State	10 s	Steady State		
Drain-Source Voltage	V _{DS}	20		- 20		V	
Gate-Source Voltage	V _{GS}	± 12		± 12			
Continuous Drain Current (T _J = 150 °C) ^{a,b}	I _D	T _A = 25 °C	9.1	6.6	- 5.3	- 3.8	A
		T _A = 70 °C	7.3	5.3	- 4.9	- 3.1	
Pulsed Drain Current	I _{DM}	30		- 20		A	
Continuous Source Current (Diode Conduction) ^{a,b}	I _S	2.1	1.1	- 2.1	- 1.1		
Maximum Power Dissipation ^{a,b}	P _D	T _A = 25 °C	2.5	1.3	2.5	1.3	W
		T _A = 70 °C	1.6	0.8	1.6	0.8	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	40	50	41	50	°C/W
		Steady State	75	95	75	95	
Maximum Junction-to-Foot (Drain)	R _{thJF}	20	22	23	26	°C/W	

Notes:

- a. Surface Mounted on FR4 board.
b. t ≤ 10 s.

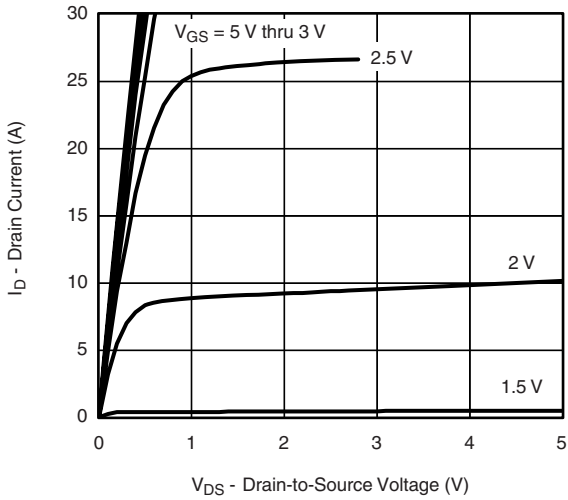
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	0.6		1.5	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-0.6		-1.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}$	N-Ch	30			A
		$V_{DS} = -5\text{ V}, V_{GS} = -4.5\text{ V}$	P-Ch	-20			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 9.1\text{ A}$	N-Ch		0.016	0.020	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -5.3\text{ A}$	P-Ch		0.048	0.060	
		$V_{GS} = 2.5\text{ V}, I_D = 3.3\text{ A}$	N-Ch		0.024	0.030	
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$	P-Ch		0.082	0.100	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 9.1\text{ A}$	N-Ch		29		S
		$V_{DS} = -15\text{ V}, I_D = -5.3\text{ A}$	P-Ch		11		
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -2.1\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.8	-1.2	
Dynamic^a							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.1\text{ A}$	N-Ch		11	17	nC
			P-Ch		6.0	9	
Gate-Source Charge	Q_{gs}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5.3\text{ A}$	N-Ch		2.5		
			P-Ch		1.3		
Gate-Drain Charge	Q_{gd}		N-Ch		3.2		
			P-Ch		1.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \equiv 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$	N-Ch		35	50	ns
Rise Time	t_r		P-Ch		20	30	
		Turn-Off Delay Time	$t_{d(off)}$	N-Ch		50	
P-Ch				35	60		
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \equiv -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$	N-Ch		31	50	
			P-Ch		55	85	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$	N-Ch		30	60	
			P-Ch		25	50	

Notes:

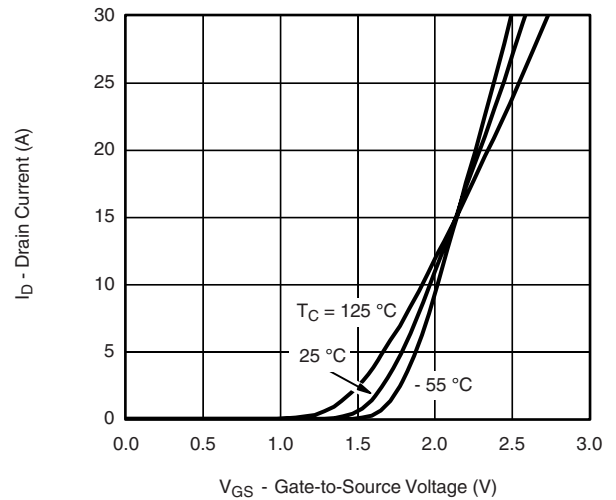
- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

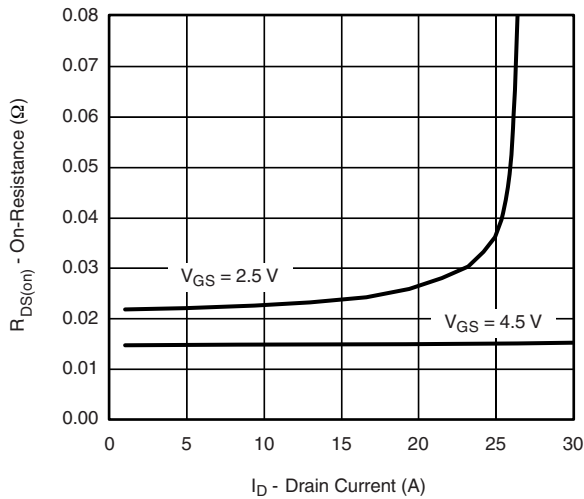
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



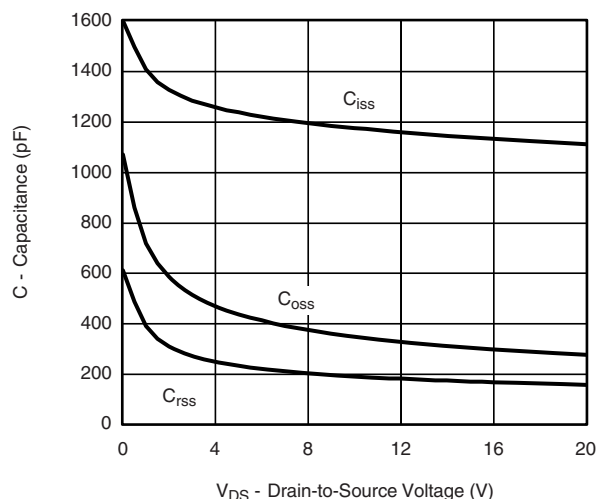
Output Characteristics



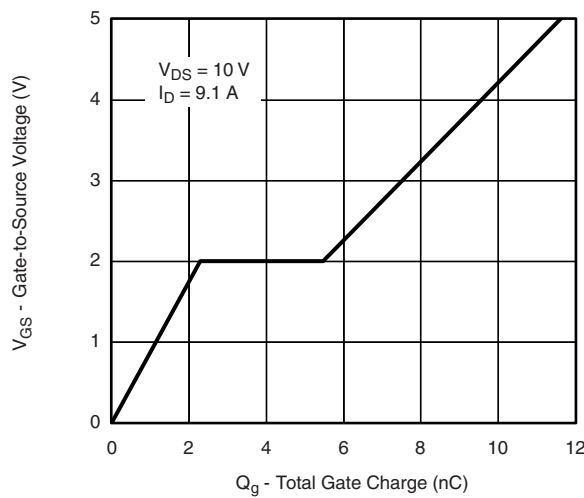
Transfer Characteristics



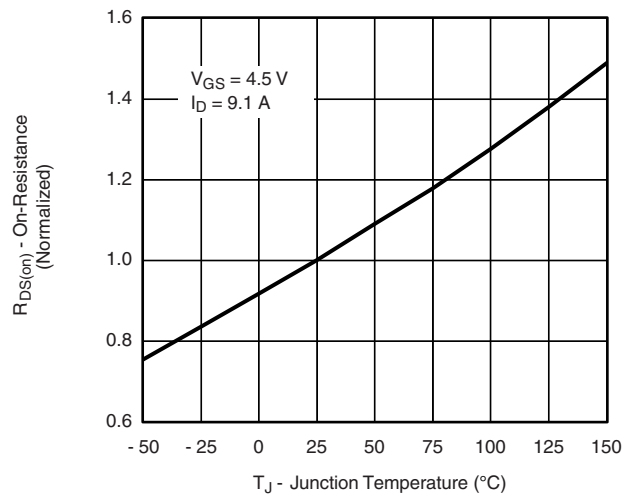
On-Resistance vs. Drain Current



Capacitance

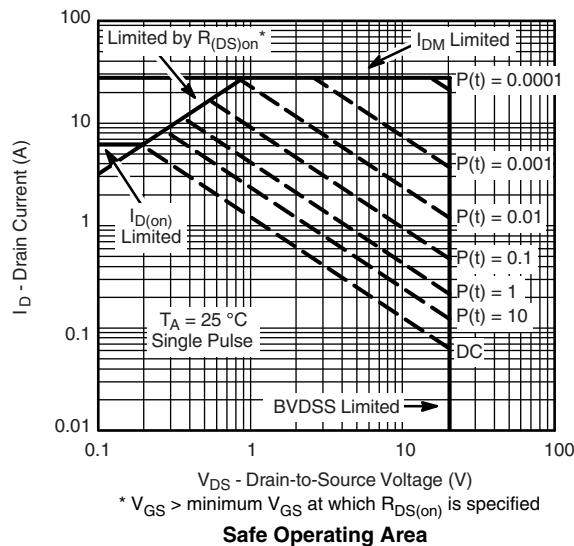
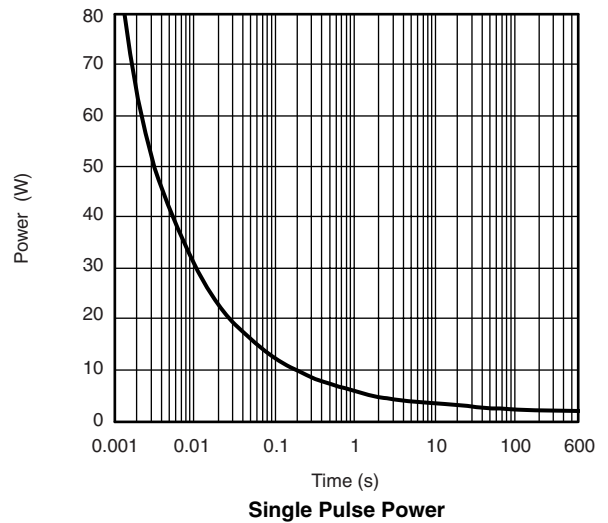
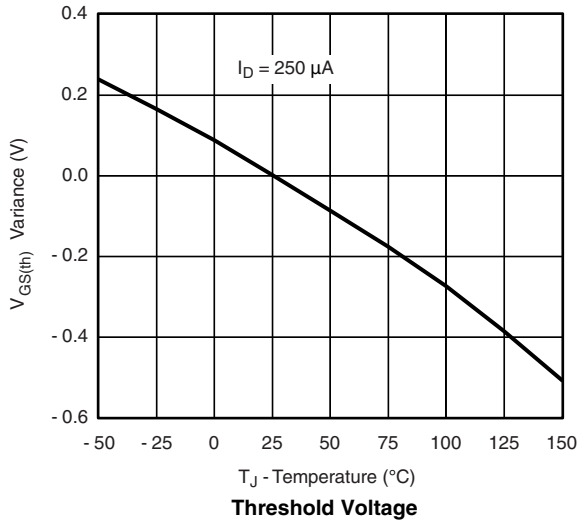
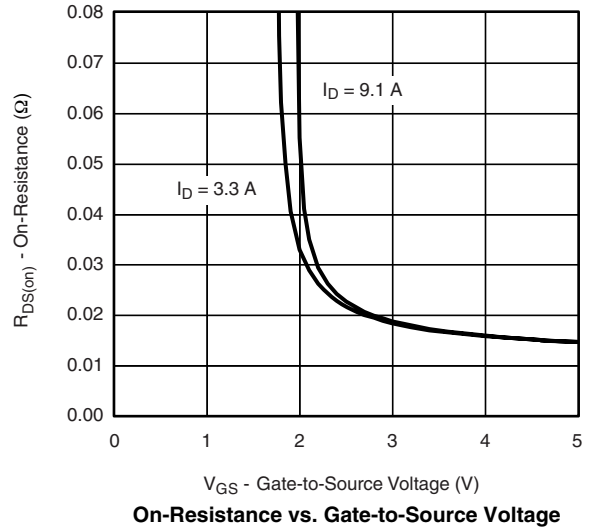
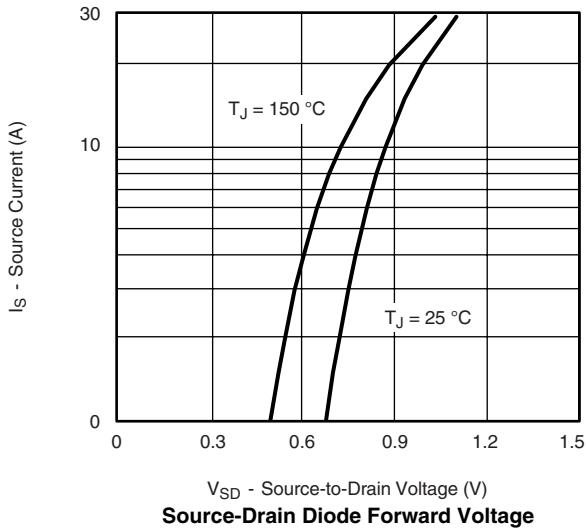


Gate Charge

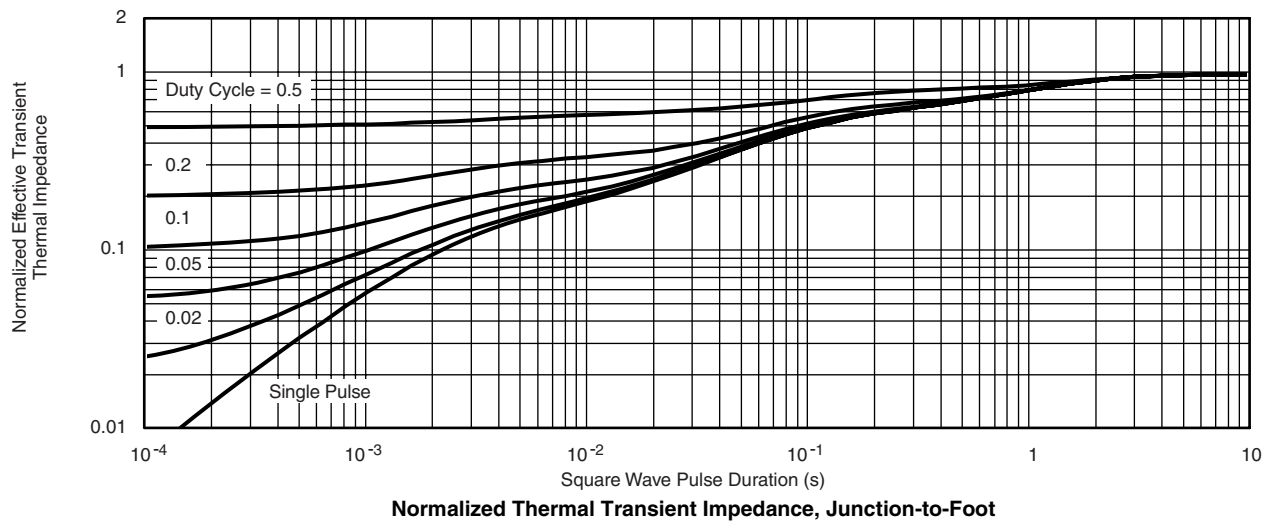
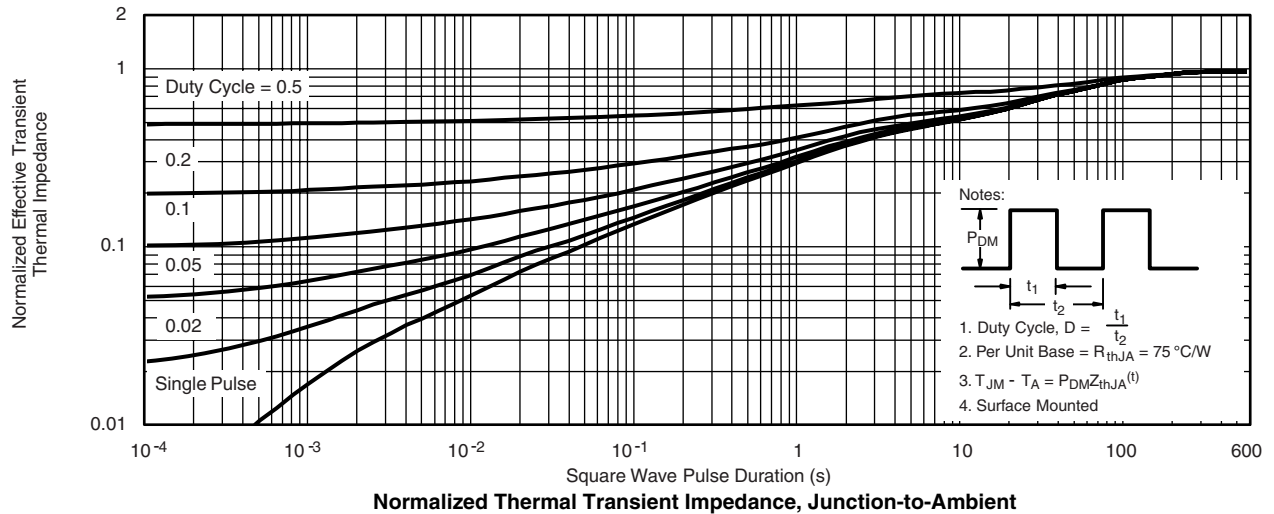


On-Resistance vs. Junction Temperature

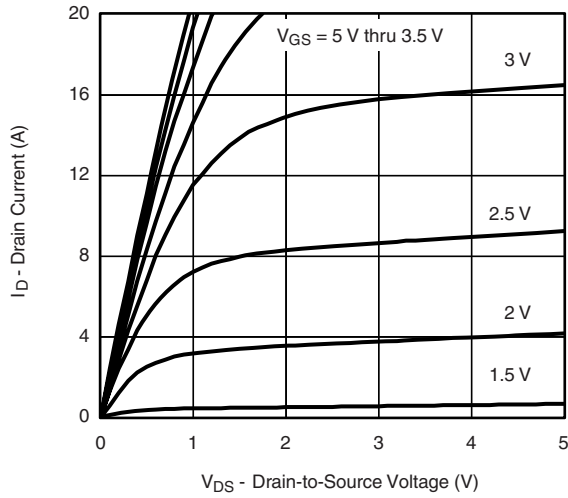
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



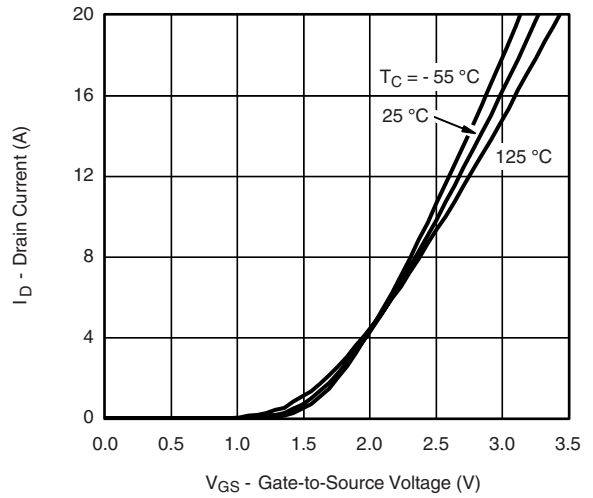
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



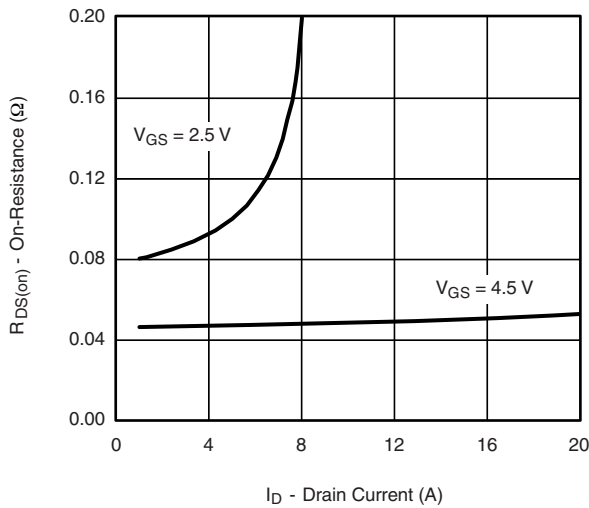
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



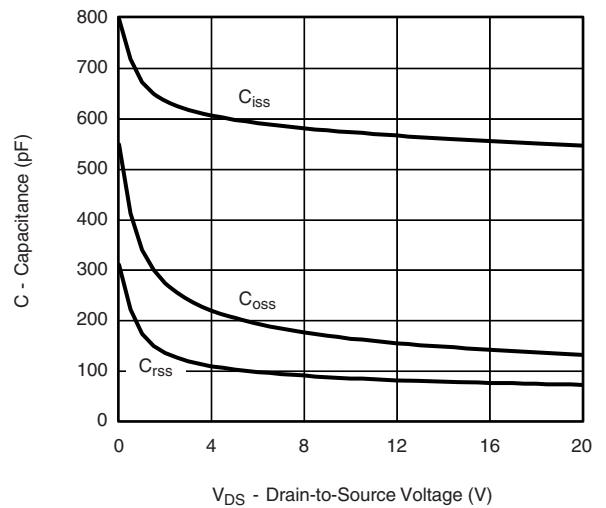
Output Characteristics



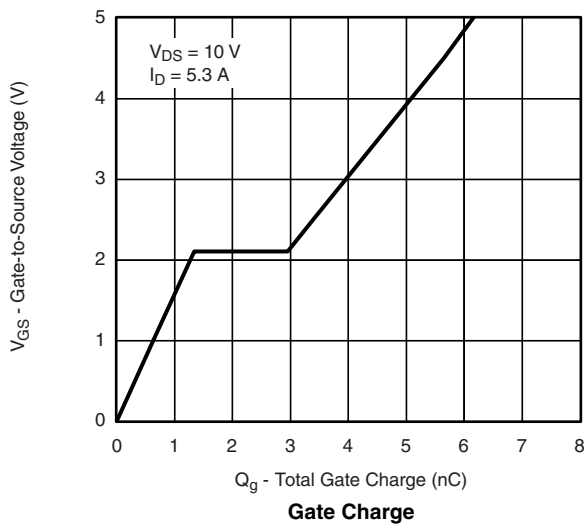
Transfer Characteristics



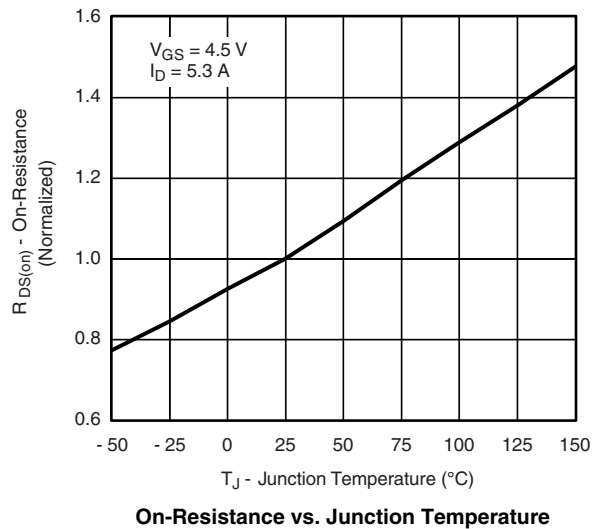
On-Resistance vs. Drain Current



Capacitance

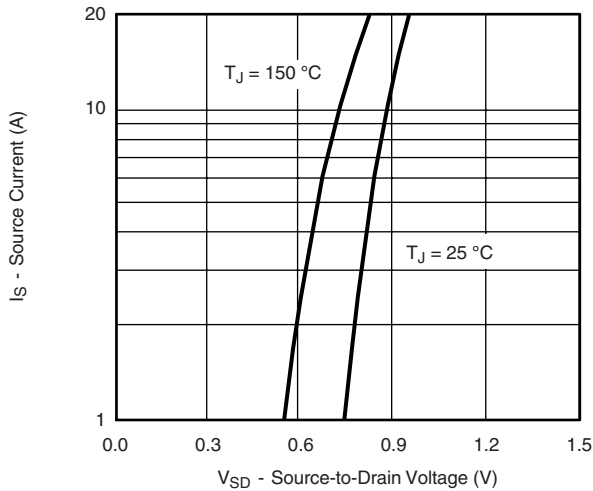


Gate Charge

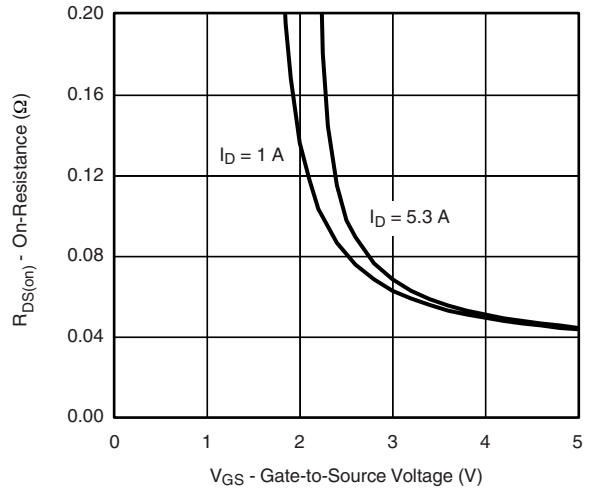


On-Resistance vs. Junction Temperature

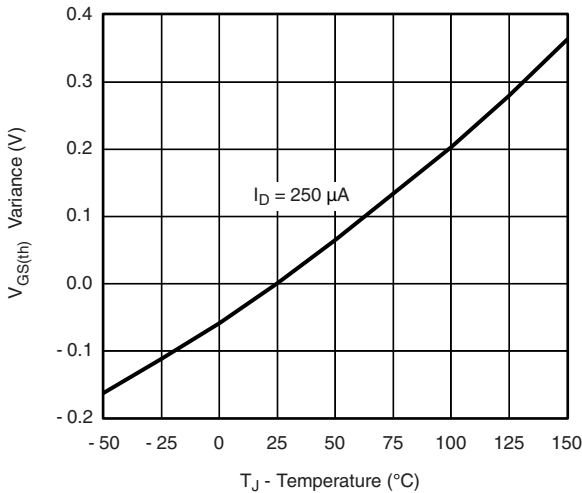
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



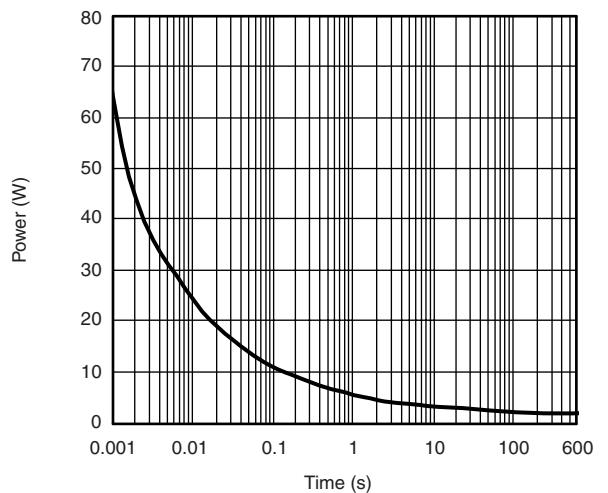
Source-Drain Diode Forward Voltage



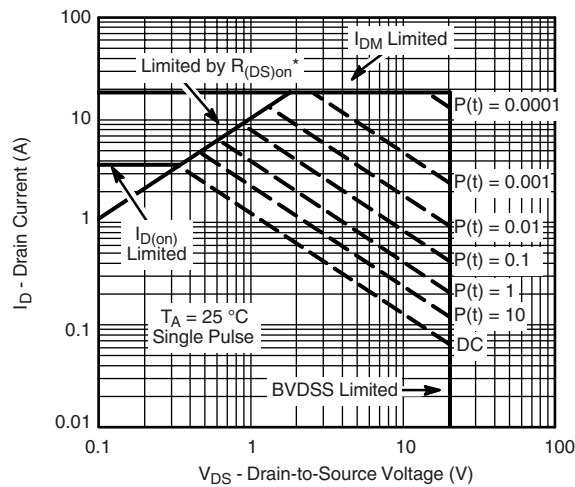
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



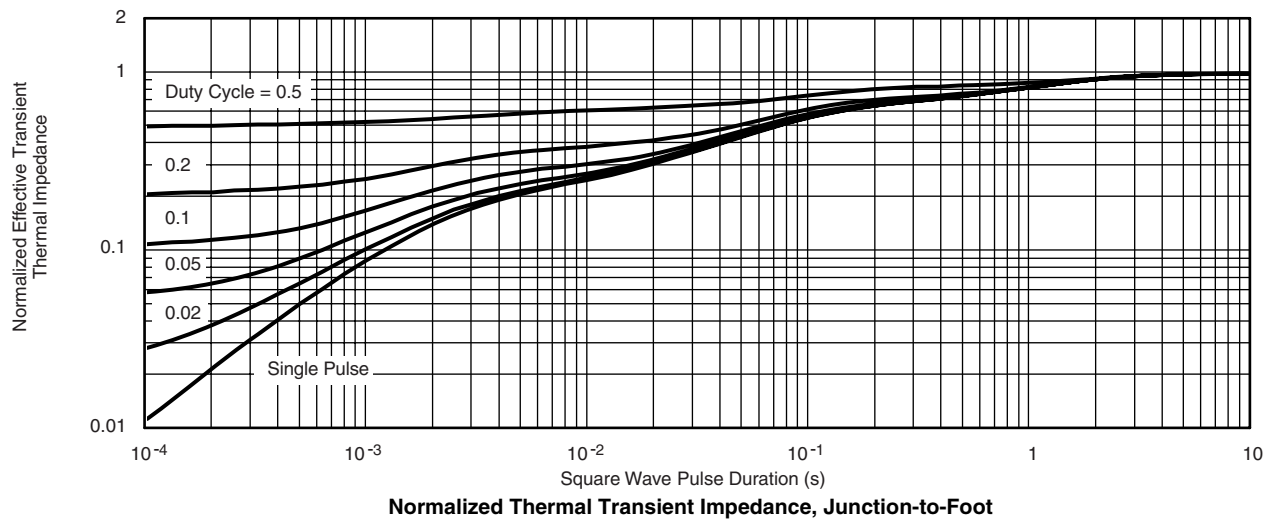
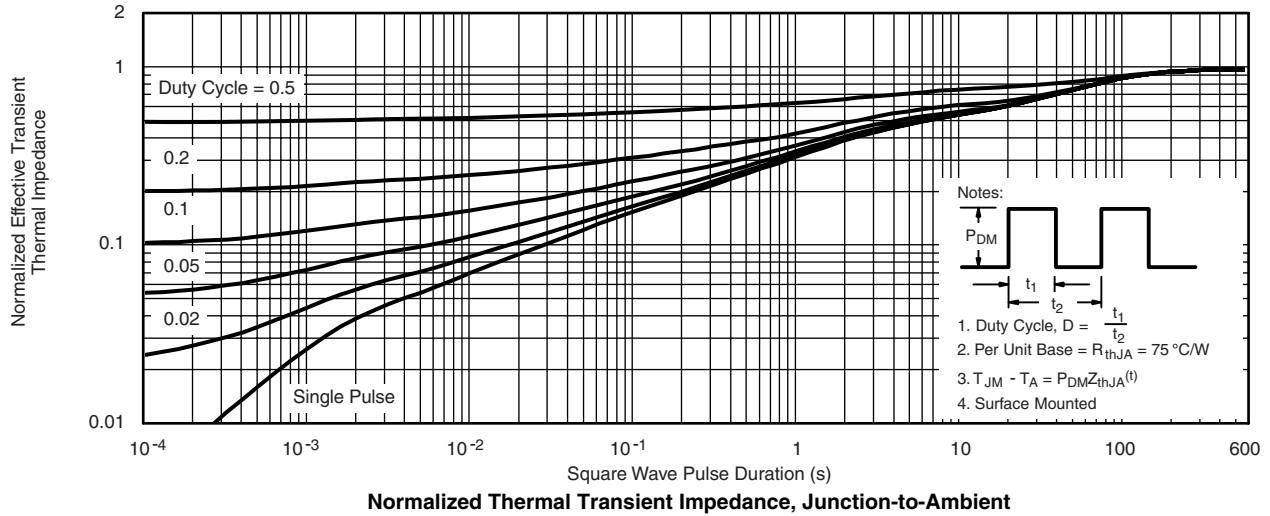
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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