N- and P-Channel Enhancement-Mode MOSFET Pair

Features

- Integrated gate-to-source resistor
- Integrated gate-to-source Zener diode
- Low threshold
- Low on-resistance
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdown
- Low input and output leakage
- Independent, electrically isolated N- and P-channels

Applications

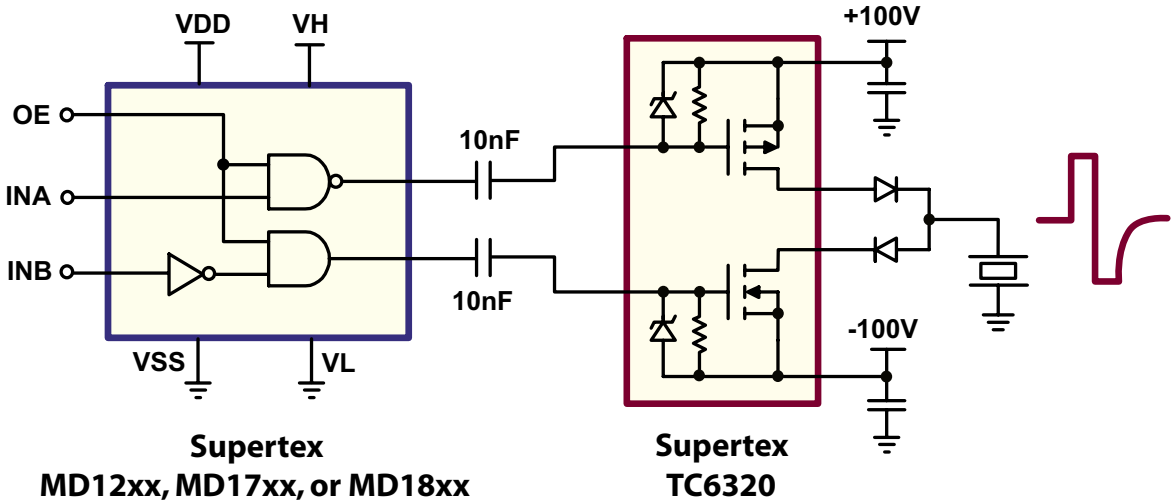
- High voltage pulsers
- Amplifiers
- Buffers
- Piezoelectric transducer drivers
- General purpose line drivers
- Logic level interfaces

General Description

The Supertex TC6320 consists of high voltage, low threshold N-channel and P-channel MOSFETs in 8-Lead SOIC and DFN packages. Both MOSFETs have integrated gate-to-source resistors and gate-to-source Zener diode clamps which are desired for high voltage pulser applications. It is a complimentary, high-speed, high voltage, gate-clamped N- and P-channel MOSFET pair, which utilizes an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Typical Application Circuit



Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (max) (Ω)	
	8-Lead DFN *4.0x4.0mm body 1.0mm height (max) 1.0mm pitch (dual pad)*	8-Lead SOIC *4.9x3.9mm body 1.75mm height (max) 1.27mm pitch*	N-Channel	P-Channel	N-Channel	P-Channel
TC6320	TC6320K6-G	TC6320TG-G	200	-200	7.0	8.0

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

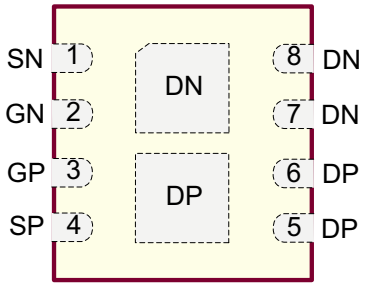
* *Distance of 1.6mm from case for 10 seconds.*

Thermal Characteristics

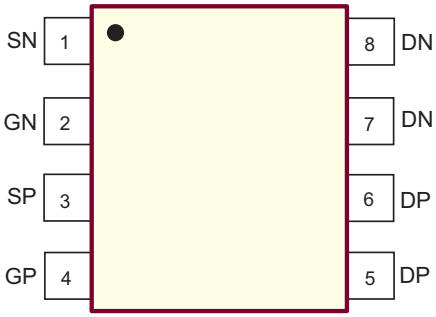
Package	Value
8-Lead DFN (K6)	θ_{ja} = 44°C/W
8-Lead SOIC (TG)	θ_{ja} = 130°C/W

Note:
1.0oz, 4-layer, 3"x4" PCB

Pin Configurations



8-Lead DFN (K6)
(top view)



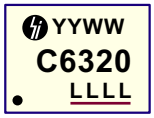
8-Lead SOIC (TG)
(top view)

Package Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead DFN (K6)



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (TG)

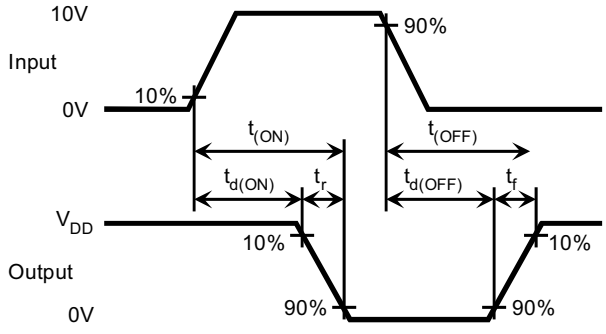
N-Channel Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

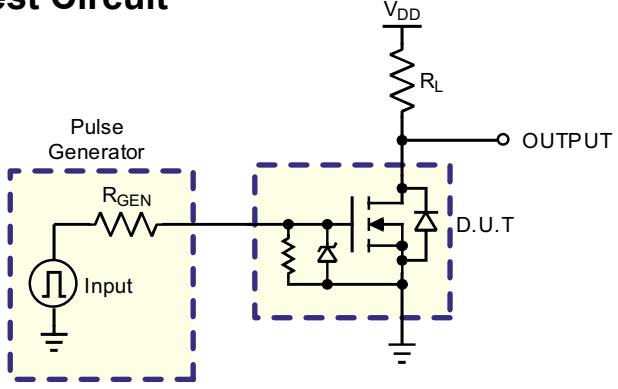
Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	200	-	-	V	V_{GS} = 0V, I_D = 2.0mA
$V_{GS(th)}$	Gate threshold voltage	1.0	-	2.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
R_{GS}	Gate-to-source shunt resistor	10	-	50	KΩ	I_{GS} = 100µA
VZ_{GS}	Gate-to-source Zener voltage	13.2	-	25	V	I_{GS} = 2.0mA
I_{DSS}	Zero gate voltage drain current	-	-	10.0	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	1.0	-	-	A	V_{GS} = 4.5V, V_{DS} = 25V
		2.0	-	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	8.0	Ω	V_{GS} = 4.5V, I_D = 150mA
		-	-	7.0		V_{GS} = 10V, I_D = 1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	V_{GS} = 4.5V, I_D =150mA
G_{FS}	Forward transconductance	400	-	-	mmho	V_{DS} = 25V, I_D = 500mA
C_{ISS}	Input capacitance	-	-	110	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	-	60		
C_{RSS}	Reverse transfer capacitance	-	-	23		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	V_{DD} =25V, I_D = 1.0A, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 500mA

Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

N-Channel Switching Waveforms and Test Circuit





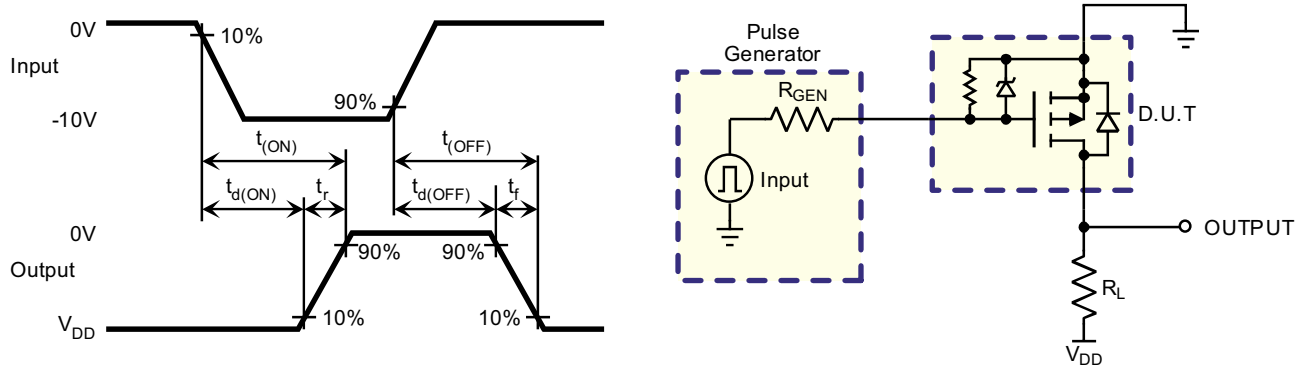
P-Channel Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-200	-	-	V	V_{GS} = 0V, I_D = -2.0mA
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
R_{GS}	Gate-to-source shunt resistor	10	-	50	KΩ	I_{GS} = 100µA
VZ_{GS}	Gate-to-source Zener voltage	13.2	-	25	V	I_{GS} = -2mA
I_{DSS}	Zero gate voltage drain current	-	-	-10	µA	V_{DS} = Max rating, V_{GS} = 0V
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-1.0	-	-	A	V_{GS} = -4.5V, V_{DS} = -25V
		-2.0	-	-		V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	10	Ω	V_{GS} = -4.5V, I_D = -150mA
		-	-	8.0		V_{GS} = -10V, I_D = -1.0A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/°C	V_{GS} = -10V, I_D =-200mA
G_{FS}	Forward transconductance	400	-	-	mmho	V_{DS} = -25V, I_D = -500mA
C_{ISS}	Input capacitance	-	-	200	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	-	55		
C_{RSS}	Reverse transfer capacitance	-	-	30		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	V_{DD} = -25V, I_D = -1.0A, R_{GEN} = 25Ω
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	20		
t_f	Fall time	-	-	15		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	V_{GS} = 0V, I_{SD} = -500mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = -500mA

Notes:

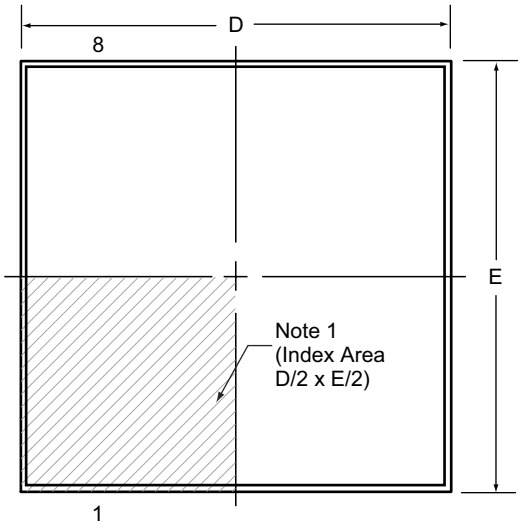
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

P-Channel Switching Waveforms and Test Circuit

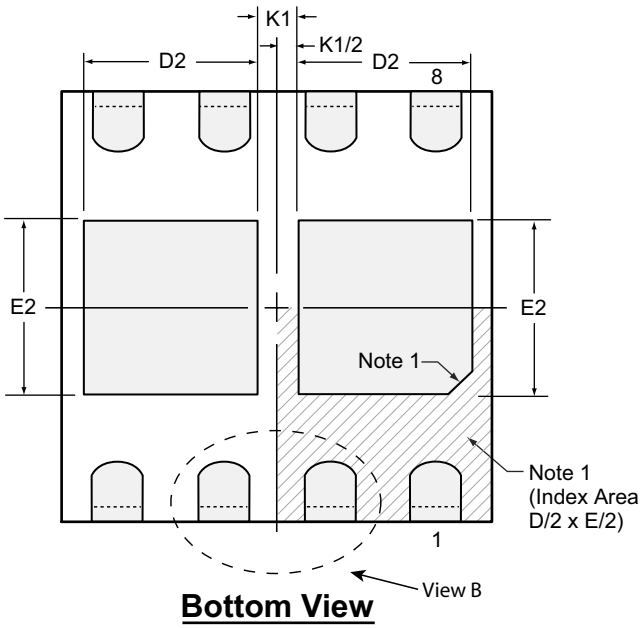


8-Lead DFN Package Outline (K6)

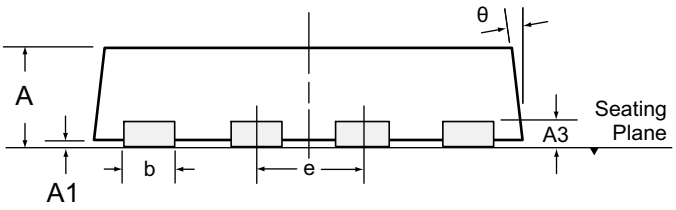
4.00x4.00mm body, 0.90mm height (max), 1.00mm pitch (dual pad)



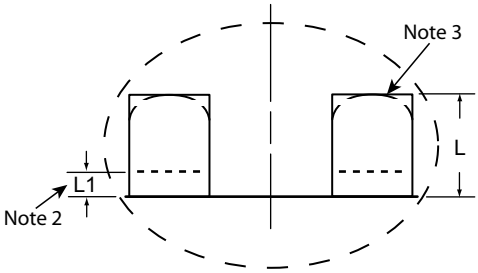
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

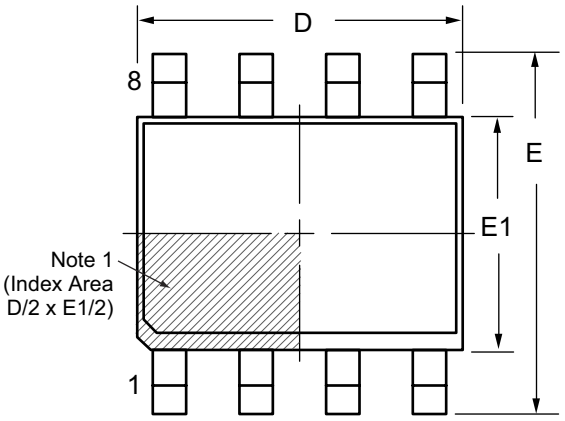
Symbol		A	A1	A3	b	D	D2	E	E2	e	K1	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	3.90	1.35	3.90	1.35	1.00 BSC	0.50 REF	0.40	0.00	0º
	NOM	0.85	-		0.30	4.00	1.45	4.00	1.45			0.50	-	-
	MAX	0.90	0.05		0.35	4.10	1.55	4.10	1.55			0.60	0.15	14º

Drawings not to scale

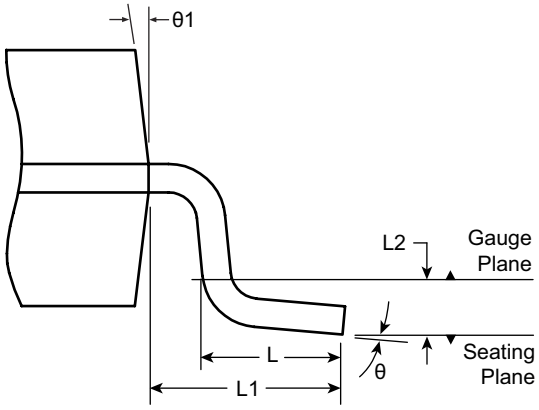
Supertex Doc. #: *DSPD-8DFNK64x4P100, Version B101008*

8-Lead SOIC (Narrow Body) Package Outline (TG)

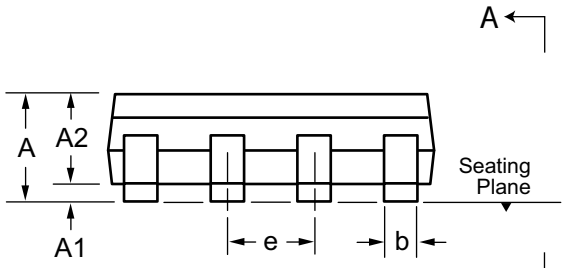
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



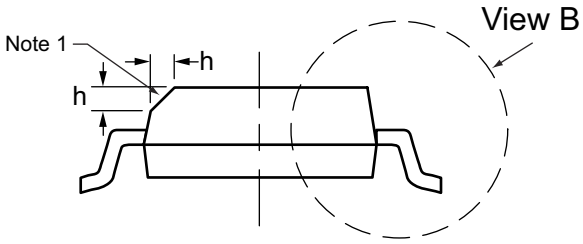
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*

Drawings are not to scale.

***Supertex Doc. #:** DSPD-8SOLGTG, Version H101708.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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