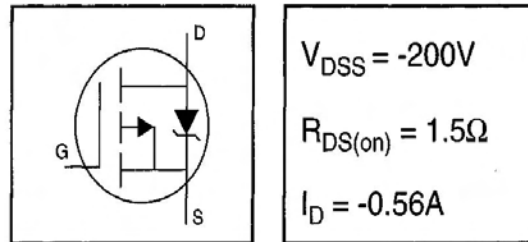


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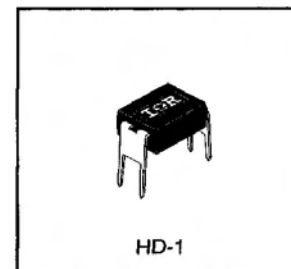
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling
- Lead-Free



Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ -10 V	-0.56	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ -10 V	-0.36	
I_{DM}	Pulsed Drain Current ①	-4.5	
P_D @ $T_C = 25^\circ C$	Power Dissipation	1.0	W
	Linear Derating Factor	0.0083	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	420	mJ
I_{AR}	Avalanche Current ①	-0.56	A
E_{AR}	Repetitive Avalanche Energy ①	0.10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} =0V, I _D =-250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.22	—	V/°C	Reference to 25°C, I _D =-1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V _{GS} =-10V, I _D =-0.34A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
g _{fs}	Forward Transconductance	0.55	—	—	S	V _{DS} =-50V, I _D =-0.35A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} =-200V, V _{GS} =0V
		—	—	-500	μA	V _{DS} =-160V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} =-20V
	Gate-to-Source Reverse Leakage	—	—	100	nA	V _{GS} =20V
Q _g	Total Gate Charge	—	—	15	nC	I _D =-2.1A
Q _{gs}	Gate-to-Source Charge	—	—	3.2	nC	V _{DS} =-160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.4	nC	V _{GS} =-10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	8.8	—	ns	V _{DD} =-100V
t _r	Rise Time	—	27	—		I _D =-3.9A
t _{d(off)}	Turn-Off Delay Time	—	7.3	—		R _G =18Ω
t _f	Fall Time	—	19	—		R _D =24Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	6.0	—		
C _{iss}	Input Capacitance	—	340	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	110	—		V _{DS} =-25V
C _{rss}	Reverse Transfer Capacitance	—	33	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.56	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-4.5		
V _{SD}	Diode Forward Voltage	—	—	-6.3	V	T _J =25°C, I _S =-0.56A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	150	300	ns	T _J =25°C, I _F =-3.9A
Q _{rr}	Reverse Recovery Charge	—	0.97	2.0	μC	di/dt=100A/μs ④

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=-50V, starting T_J=25°C, L=130mH R_G=25Ω, I_{AS}=-2.2A (See Figure 12)
- ③ I_{SD}≤-3.9A, di/dt≤95A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

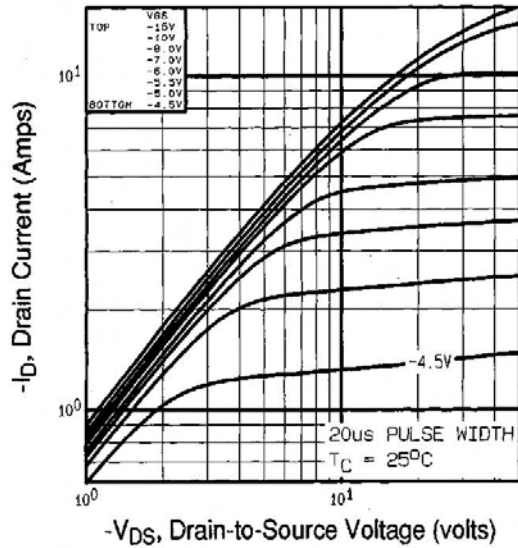


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

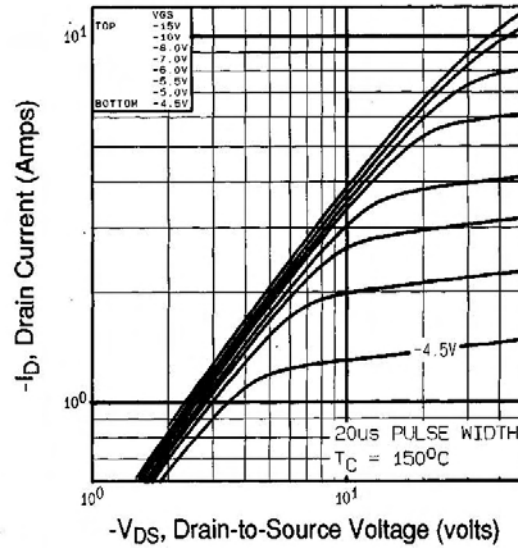


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

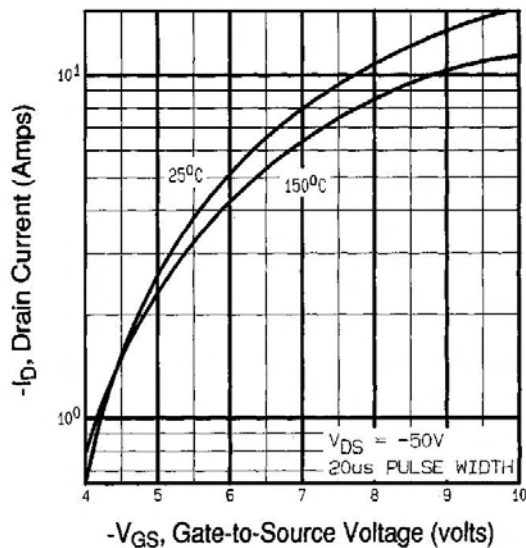


Fig 3. Typical Transfer Characteristics

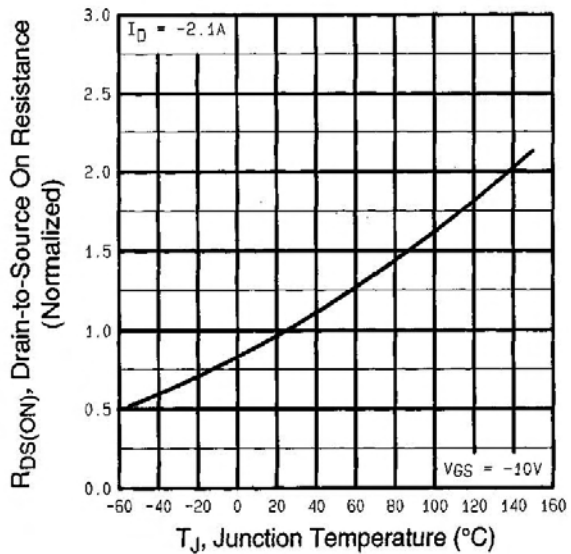


Fig 4. Normalized On-Resistance
Vs. Temperature

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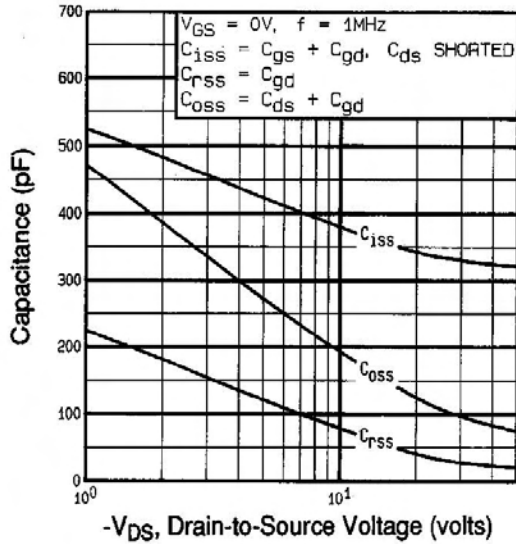


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

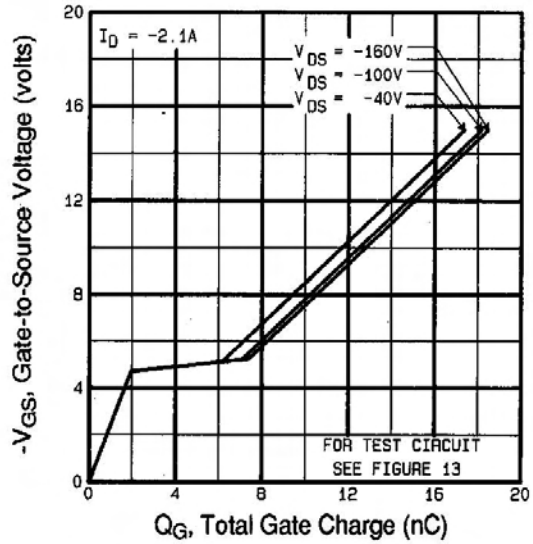


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

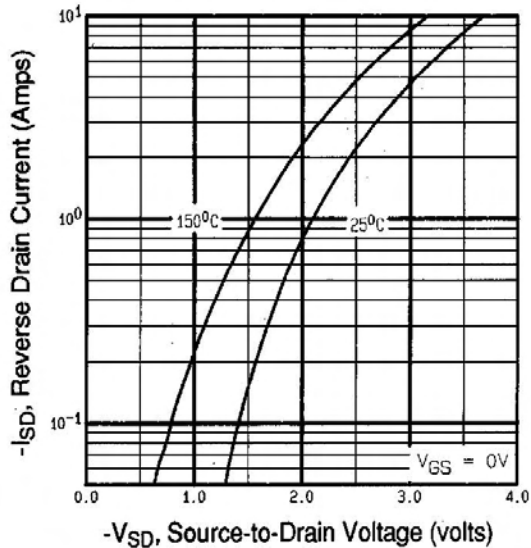


Fig 7. Typical Source-Drain Diode Forward Voltage

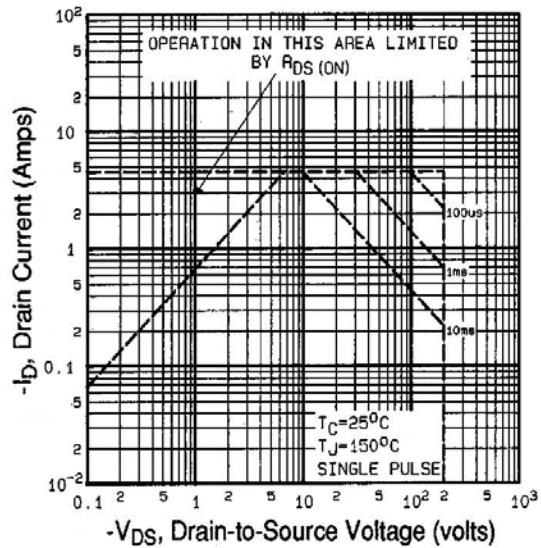


Fig 8. Maximum Safe Operating Area

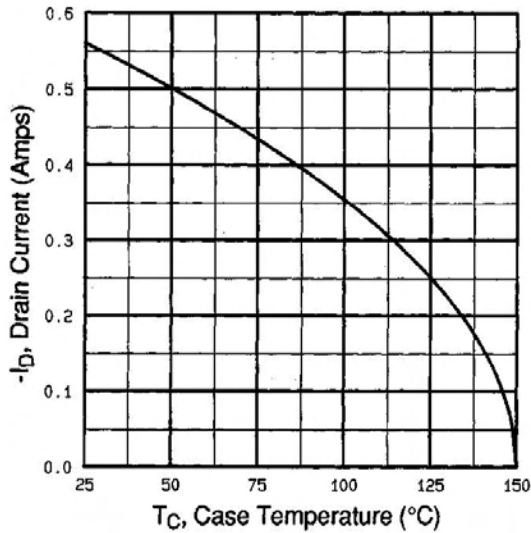


Fig 9. Maximum Drain Current Vs. Case Temperature

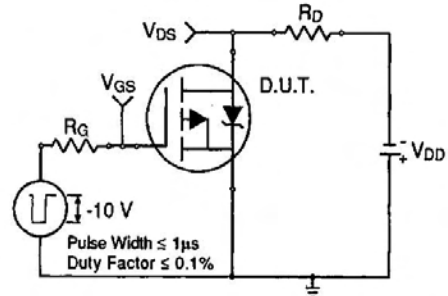


Fig 10a. Switching Time Test Circuit

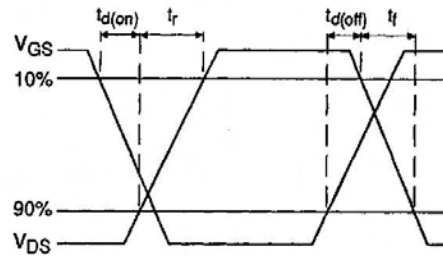


Fig 10b. Switching Time Waveforms

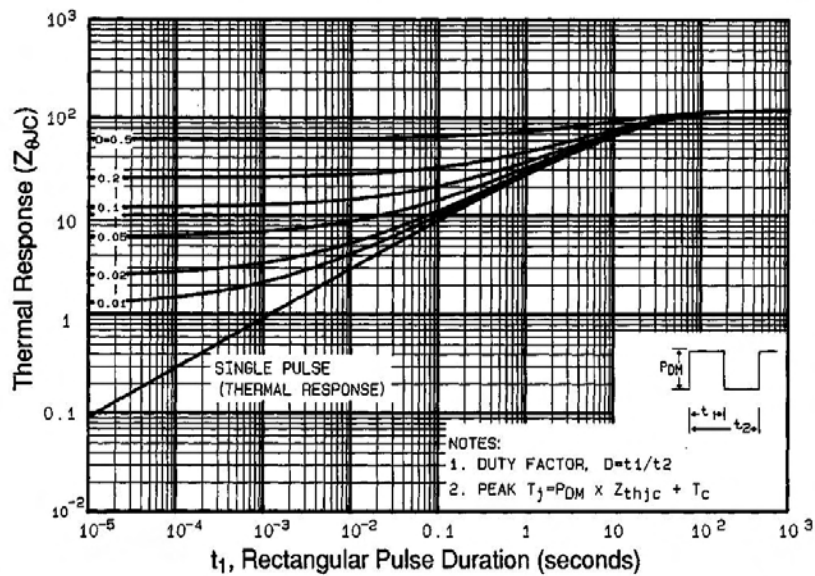


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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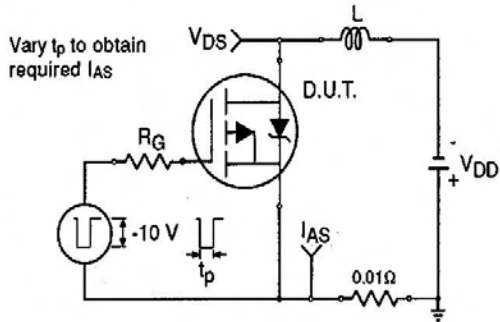


Fig 12a. Unclamped Inductive Test Circuit

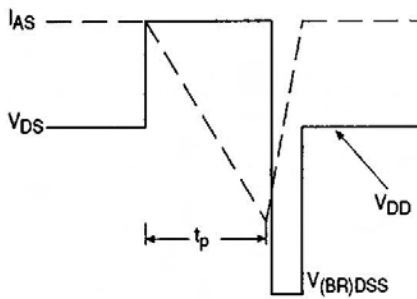


Fig 12b. Unclamped Inductive Waveforms

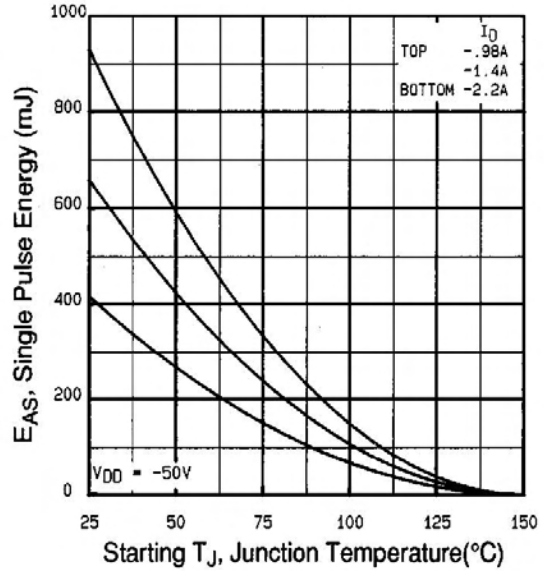


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

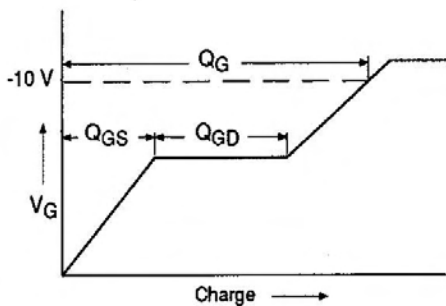


Fig 13a. Basic Gate Charge Waveform

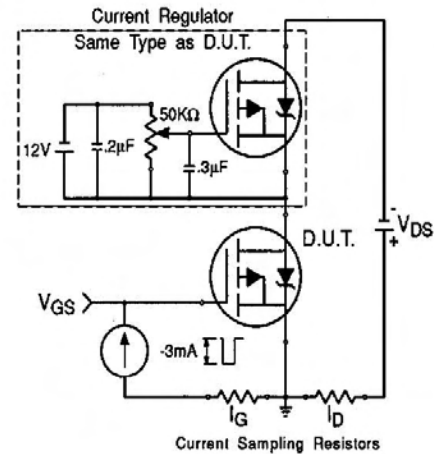


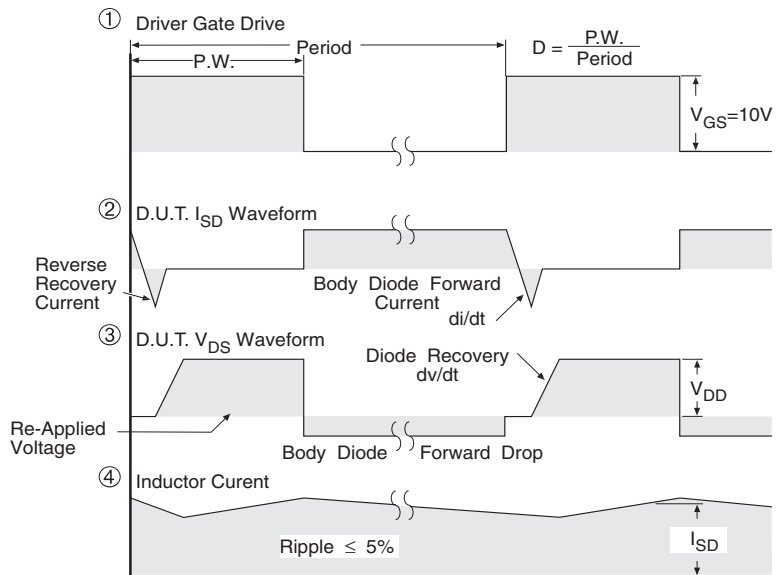
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

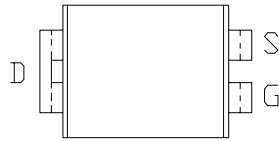
Fig -14 For P Channel HEXFETS

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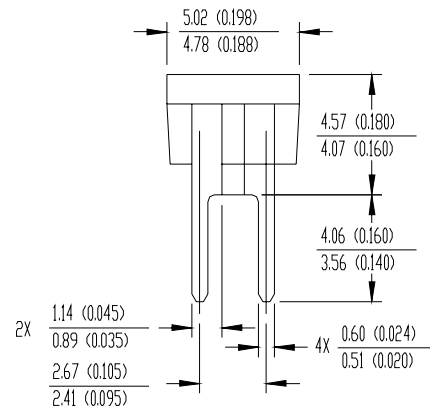
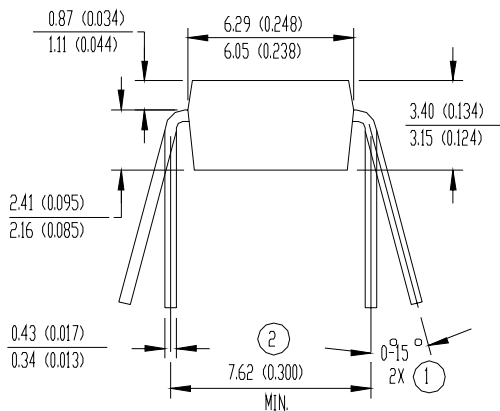
Hexdip Package Outline

Dimensions are shown in millimeters (inches)



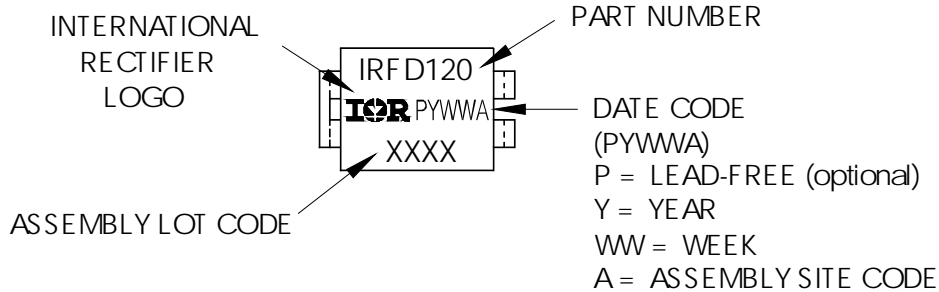
NOTES:

- ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
- ② APPLIES TO INSTALLED LEAD CENTERS
- 3 CONTROLLING DIMENSION: INCH.
- 4 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES).
- 5 CASE STYLE HD-1 (SIMILAR TO JEDEC OUTLINE MO-001AN)
- 6 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP
SOLDER DIP MAX. + 0.16 (0.006)



Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120



Data and specifications subject to change without notice.

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TAC Fax: (310) 252-7903
10/04



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