



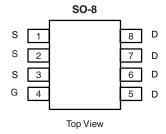
N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
30	0.007 at V _{GS} = 10 V	16		
	0.010 at V _{GS} = 4.5 V	13		

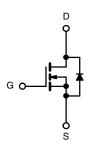
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- High-Efficiency PWM Optimized
- 100 % R_g Tested





Ordering Information: Si4888DY-T1-E3 (Lead (Pb)-free) Si4888DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	30		V	
Gate-Source Voltage		V _{GS}	± 20			
Continuous Drain Current /T 150 °C\a	T _A = 25 °C	I _D	16	11	_	
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		13	8		
Pulsed Drain Current		I _{DM}	± 50		Α	
Continuous Source Current (Diode Conduction) ^a		I _S	3.0	1.40		
W	T _A = 25 °C	- P _D	3.5	1.6	· W	
Maximum Power Dissipation ^a	T _A = 70 °C		2.2	1.0		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum landing to Austingt (MOOFFT)	t ≤ 10 s	- R _{thJA}	29	35	°C/W
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		65	80	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	18	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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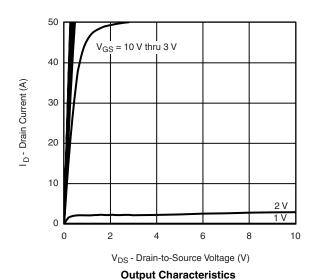
SPECIFICATIONS $T_J = 25 ^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	0.80		1.6	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 20 V$			± 100	nA	
Zava Cata Valtaga Drain Current	1	V _{DS} = 30 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
	В	V _{GS} = 10 V, I _D = 16 A		0.0058	0.007	0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 13 A		0.008	0.010	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 16 A		38		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 3 A, V _{GS} = 0 V		0.74	1.1	V	
Dynamic ^b							
Total Gate Charge	Q_g			16.3	24		
Gate-Source Charge	Q_{gs}	Q_{gs} $V_{DS} = 15 \text{ V}, V_{GS} = 5.0 \text{ V}, I_D = 16 \text{ A}$		4		nC	
Gate-Drain Charge	Q_{gd}			5.9			
Gate Resistance	R_{g}		0.5	1.5	2.6	Ω	
Turn-On Delay Time	t _{d(on)}			14	20		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega$		10	15		
Turn-Off Delay Time	t _{d(off)}	$t_{d(off)}$ $I_D \cong 1 \text{ A, } V_{GEN} = 10 \text{ V, } R_g = 6 \Omega$		44	70	ns	
Fall Time	t _f			20	30		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3 A, dI/dt = 100 A/μs		40	70		

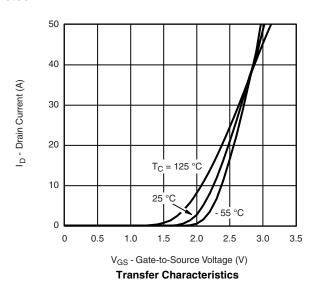
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

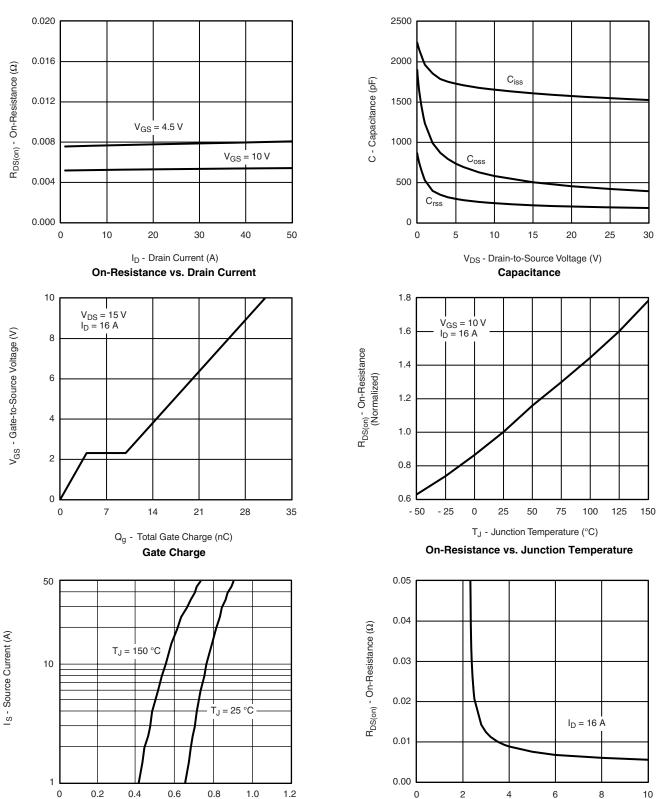








TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



V_{SD} - Source-to-Drain Voltage (V)

Source-Drain Diode Forward Voltage

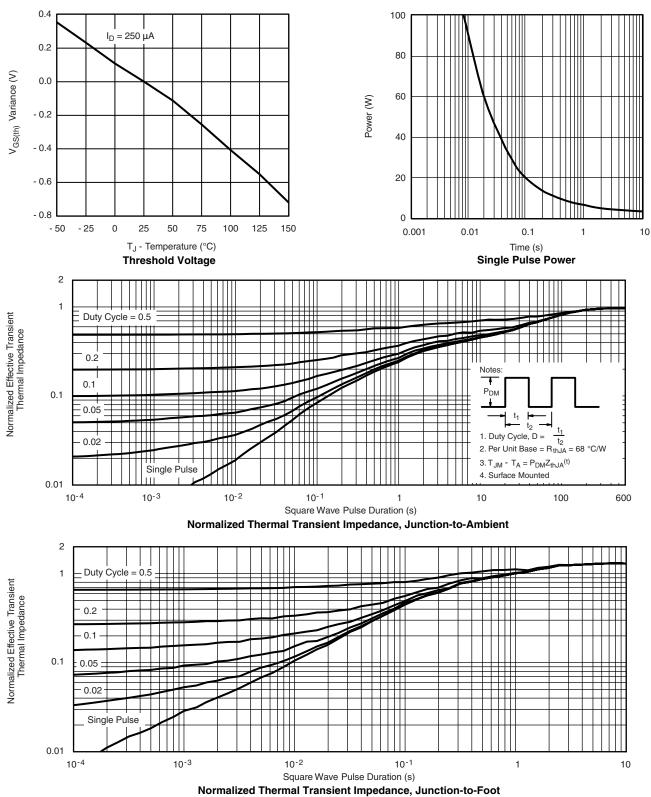
V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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