



P-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Low threshold (-2.4V max.)
- ▶ High input impedance
- ▶ Low input capacitance (95pF typical)
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

The Quad-Array package, 20-Lead SOW (WG), uses four independent DMOS transistors which provide four independent channels.

Ordering Information

Device	Package Options		BV _{DSS} /BV _{DGS} (V)	R _{DS(ON)} (max) (Ω)	I _{D(ON)} (min) (A)	V _{GS(th)} (max) (V)
	TO-92	20-Lead SOW				
TP0604	TP0604N3-G	TP0604WG-G	-40	2.0	-2.0	-2.4

-G indicates package is RoHS compliant ('Green')



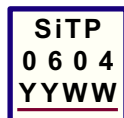
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV _{DSS}
Drain-to-gate voltage	BV _{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Product Marking

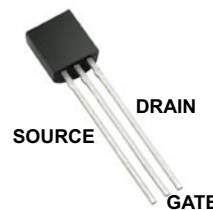


YY = Year Sealed
 WW = Week Sealed
 _____ = "Green" Packaging

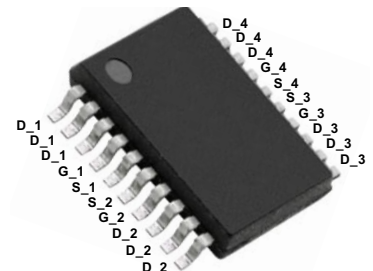
Package may or may not include the following marks: Si or

TO-92 (N3)

Pin Configurations

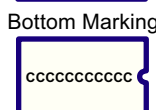


TO-92 (N3)



20-Lead SOW (WG)

Product Marking



YY = Year Sealed
 WW = Week Sealed
 A = Assembler ID
 L = Lot Number
 C = Country of Origin*
 _____ = "Green" Packaging

*May be part of top marking

Package may or may not include the following marks: Si or

20-Lead SOW (WG)

Thermal Characteristics

Package	I_D (continuous) [†] (A)	I_D (pulsed) (A)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C}/\text{W}$)	θ_{ja} ($^\circ\text{C}/\text{W}$)	I_{DR}^\dagger (A)	I_{DRM} (A)
TO-92	-0.43	-4.2	1.0	125	170	-0.43	-4.2
20-Lead SOW	-0.6	-2.0	1.5	-	84	-0.6	-2.0

Notes:

[†] I_D (continuous) is limited by max rated T_j .

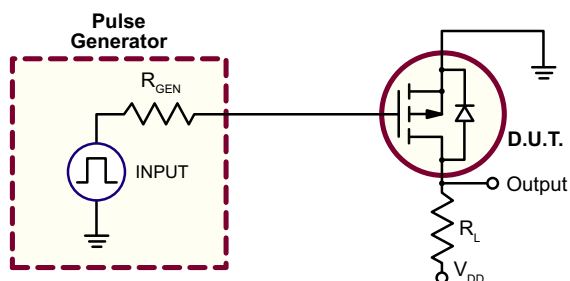
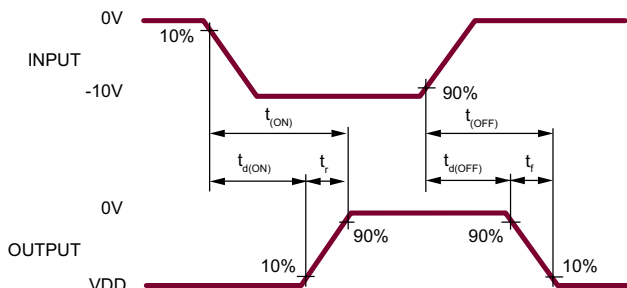
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-40	-	-	V	$V_{GS} = 0\text{V}, I_D = -2.0\text{mA}$
$V_{GS(th)}$	Gate threshold voltage	-1.0	-	-2.4	V	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.0	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0\text{mA}$
I_{GSS}	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
I_{DSS}	Zero gate voltage drain current	-	-	-10	μA	$V_{GS} = 0\text{V}, V_{DS} = \text{Max Rating}$
		-	-	-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0\text{V}, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-state drain current	-0.4	-0.6	-	A	$V_{GS} = -5.0\text{V}, V_{DS} = -20\text{V}$
		-2.0	-3.3	-		$V_{GS} = -10\text{V}, V_{DS} = -20\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	2.0	3.5	Ω	$V_{GS} = -5.0\text{V}, I_D = -250\text{mA}$
		-	1.5	2.0		$V_{GS} = -10\text{V}, I_D = -1.0\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.2	%/ $^\circ\text{C}$	$V_{GS} = -10\text{V}, I_D = -1.0\text{A}$
G_{FS}	Forward transductance	400	600	-	mmho	$V_{DS} = -20\text{V}, I_D = -1.0\text{A}$
C_{ISS}	Input capacitance	-	95	150	pF	$V_{GS} = 0\text{V}, V_{DS} = -20\text{V}, f = 1.0\text{MHz}$
C_{OSS}	Common source output capacitance	-	85	120		
C_{RSS}	Reverse transfer capacitance	-	35	60		
$t_{d(ON)}$	Turn-on delay time	-	5.0	8.0	ns	$V_{DD} = -20\text{V}, I_D = -1.0\text{A}, R_{GEN} = 25\Omega$
t_r	Rise time	-	7.0	18		
$t_{d(OFF)}$	Turn-off delay time	-	10	15		
t_f	Fall time	-	6.0	19		
V_{SD}	Diode forward voltage drop	-	-1.3	-2.0	V	$V_{GS} = 0\text{V}, I_{SD} = -1.5\text{A}$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0\text{V}, I_{SD} = -1.5\text{A}$

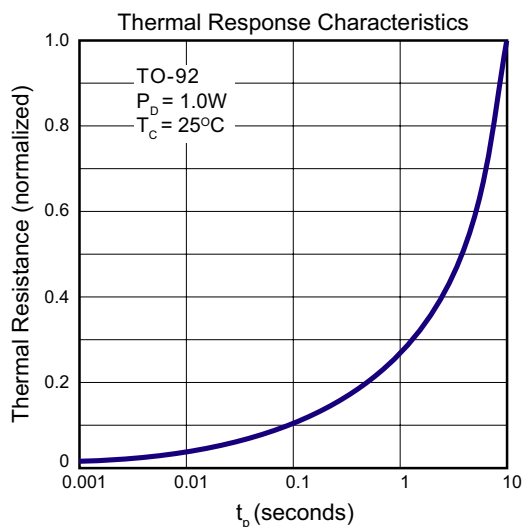
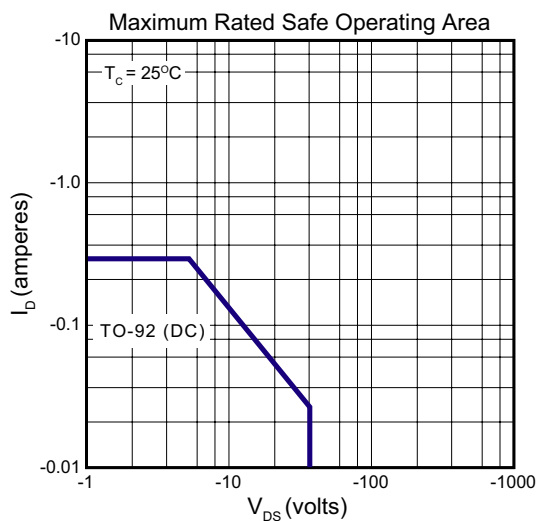
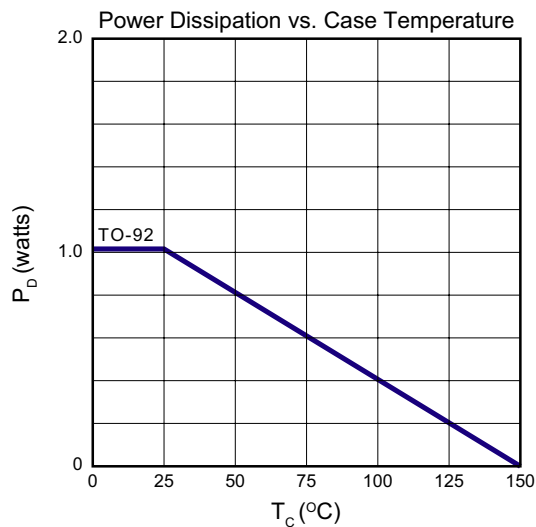
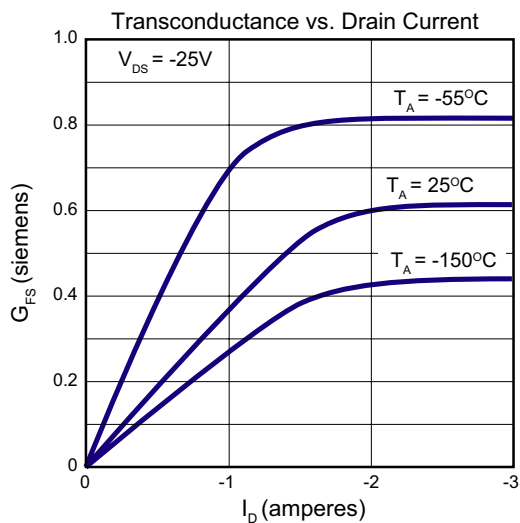
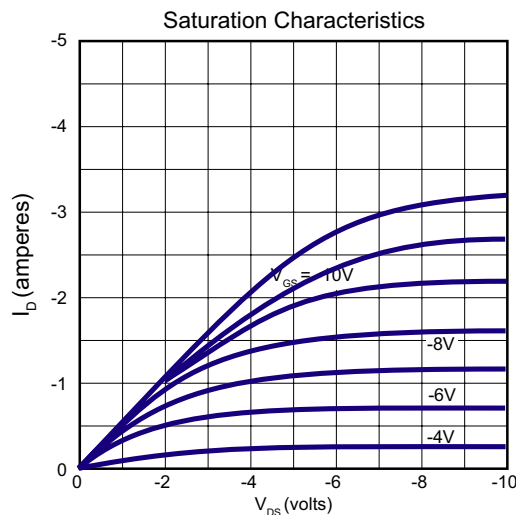
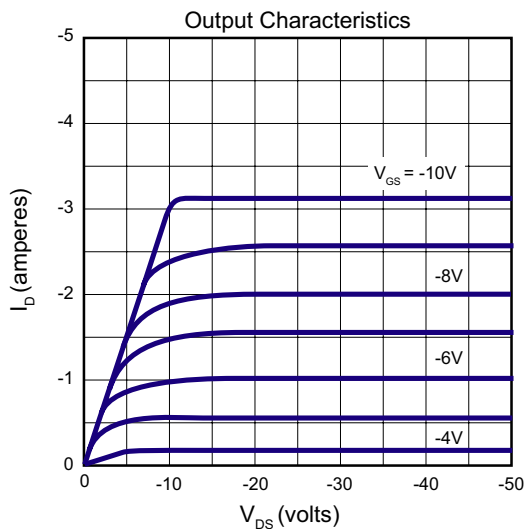
Notes:

- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

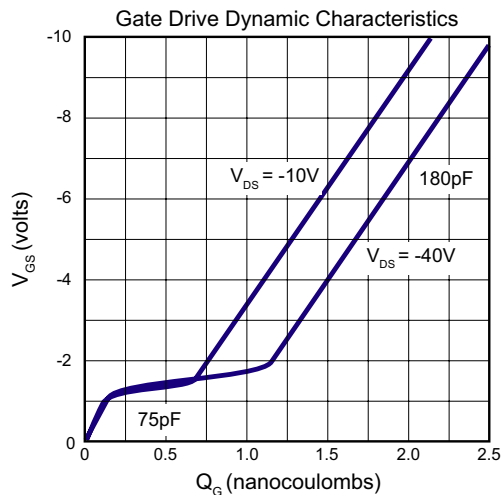
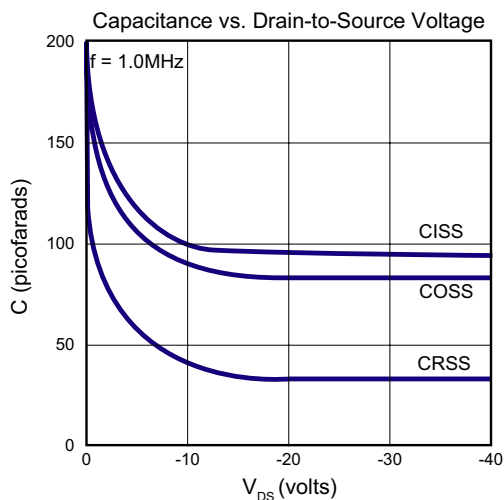
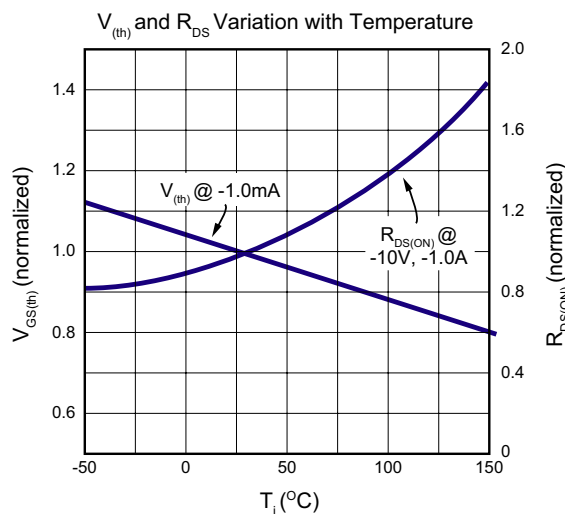
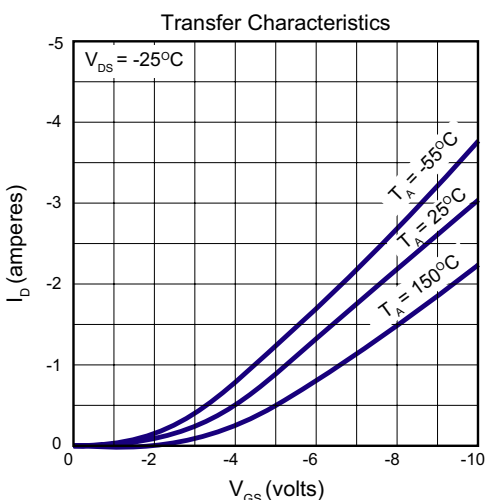
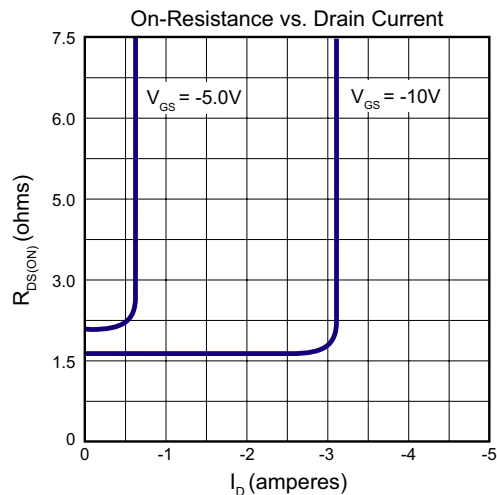
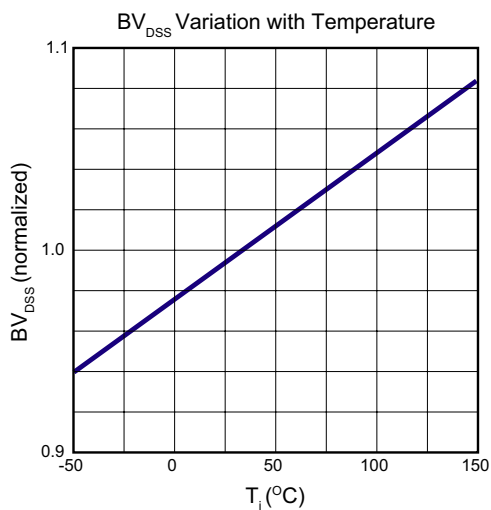
Switching Waveforms and Test Circuit



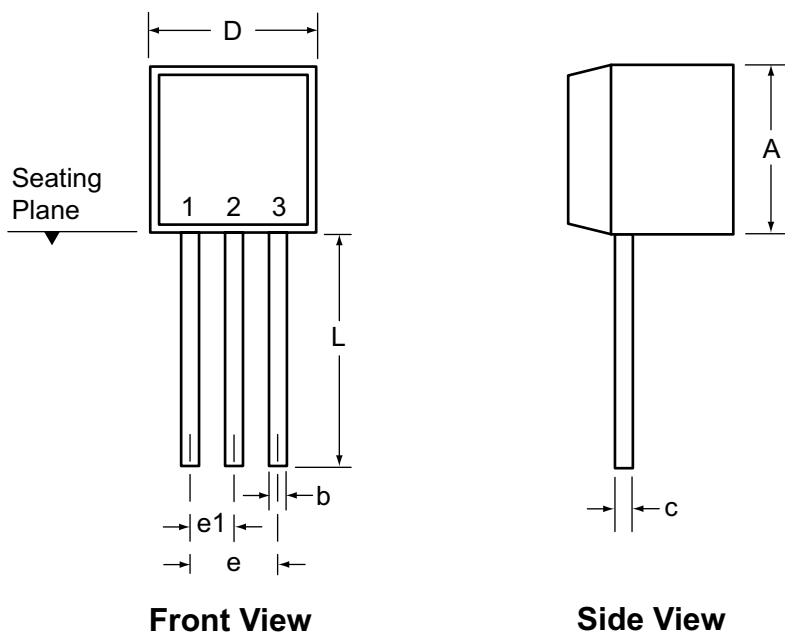
Typical Performance Curves



Typical Performance Curves (cont.)



3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

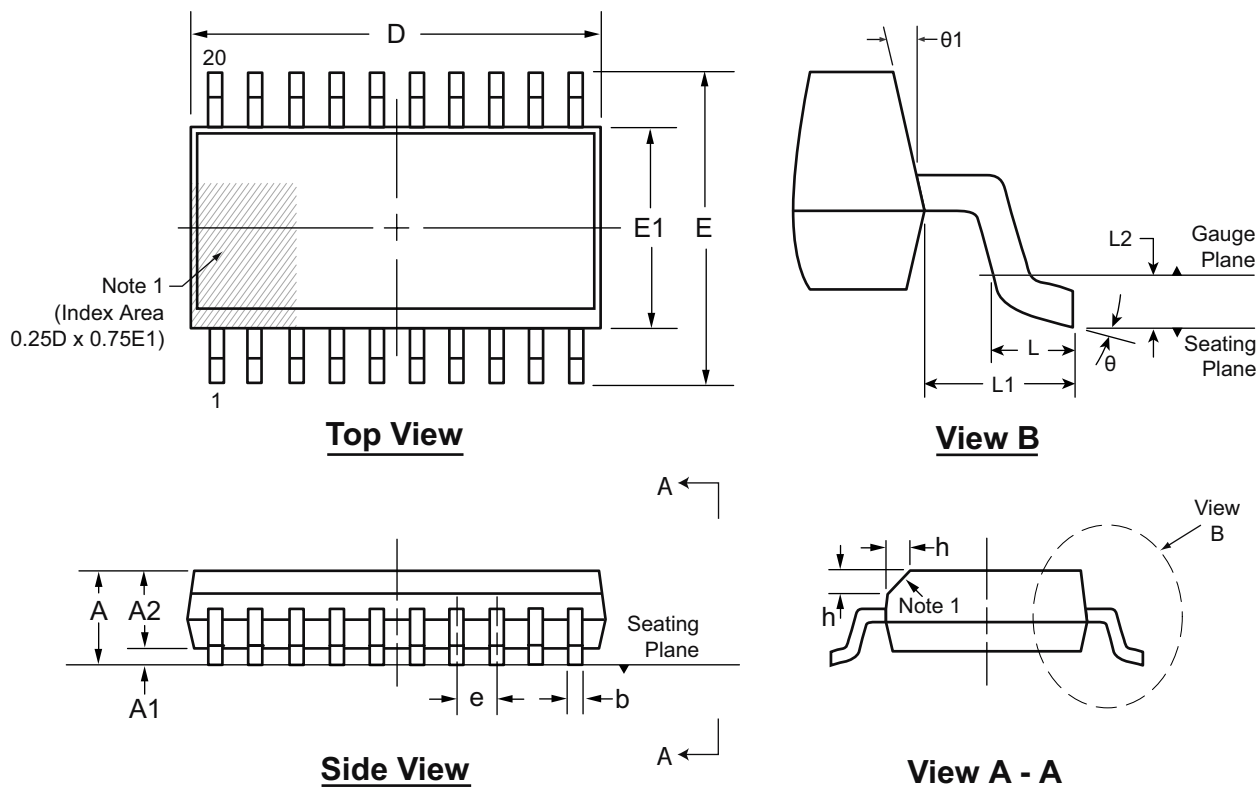
† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

20-Lead SOW (Wide Body) Package Outline (WG)

12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	2.15*	0.10	2.05	0.31	12.60*	9.97*	7.40*	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	12.80	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55*	0.51	13.00*	10.63*	7.60*		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-20SOWWG, Version D041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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