P-Channel Enhancement-Mode Lateral MOSFET

Features

- Ultra-low threshold
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Freedom from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers

General Description

These enhancement-mode (normally-off) transistors utilize a lateral MOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices.

Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown. The low threshold voltage and low on-resistance characteristics are ideally suited for hand held, battery operated applications.

Ordering Information

Device	Package Options		BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Ω)	$V_{GS(TH)}$ (max) (V)	$I_{D(ON)}$ (min) (A)
	8-Lead SOIC (Narrow Body)	TO-92				
LP0701	LP0701LG-G	LP0701N3-G	-16.5	1.5	-1.0	-1.25

-G indicates package is RoHS compliant ('Green')

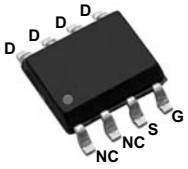
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±10V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

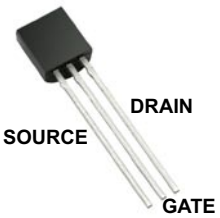
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* *Distance of 1.6mm from case for 10 seconds.*

Pin Configurations



8-Lead SOIC (LG)



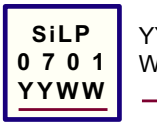
TO-92 (N3)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (LG)



YY = Year Sealed
WW = Week Sealed
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Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed)† (A)	Power Dissipation @T_c = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR} (mA)	I_{DRM}† (A)
8-Lead SOIC	-700	-1.25	1.5‡	83	104‡	-700	-1.25
TO-92	-500	-1.25	1.0	125	170	-500	-1.25

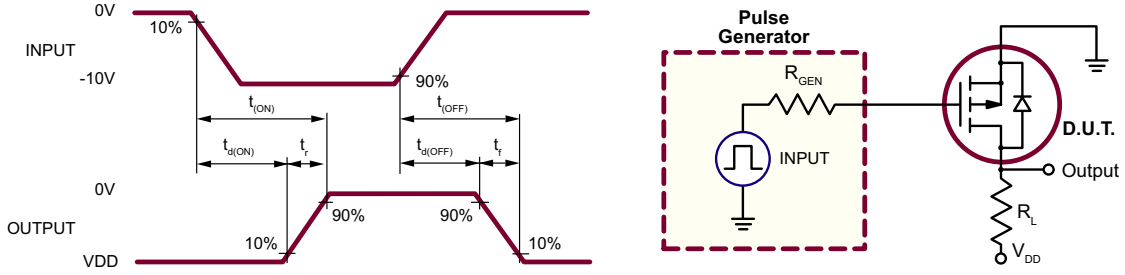
Notes:
† I_D (continuous) is limited by max rated T_j.
‡ Mounted on FR4 board, 25mm x 25mm x 1.57mm

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-16.5	-	-	V	V_{GS} = 0V, I_D = -1.0mA
V_{GS}	Gate threshold voltage	-0.5	-0.7	-1.0	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.0	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate body leakage	-	-	-100	nA	V_{GS} = ±10V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	-100	nA	V_{DS} = -15V, V_{GS} = 0V
		-	-	-1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	-	-0.4	-	A	V_{GS} = V_{DS} = -2.0V
		-0.6	-1.0	-		V_{GS} = V_{DS} = -3.0V
		-1.25	-2.3	-		V_{GS} = V_{DS} = -5.0V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	2.0	4.0	Ω	V_{GS} = -2.0V, I_D = -50mA
		-	1.7	2.0		V_{GS} = -3.0V, I_D = -150mA
		-	1.3	1.5		V_{GS} = -5.0V, I_D = -300mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/°C	V_{GS} = -5.0V, I_D = -300mA
G_{FS}	Forward transconductance	500	700	-	mmho	V_{GS} = -15V, I_D = -1.0A
C_{ISS}	Input capacitance	-	120	250	pF	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	100	125		
C_{RSS}	Reverse transfer capacitance	-	40	60		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	V_{DD} = -15V, I_D = -1.25A, R_{GEN} = 25Ω
t_r	Rise time	-	-	20		
$t_{d(OFF)}$	Turn-off delay time	-	-	30		
t_f	Fall time	-	-	30		
V_{SD}	Diode forward voltage drop	-	-1.2	-1.5	V	V_{GS} = 0V, I_{SD} = -500mA

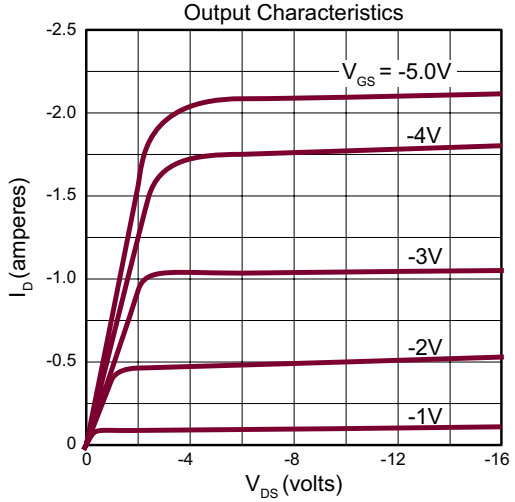
Notes:
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

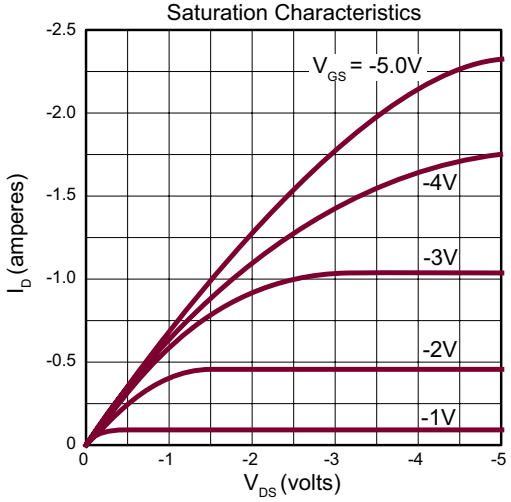


Typical Performance Curves

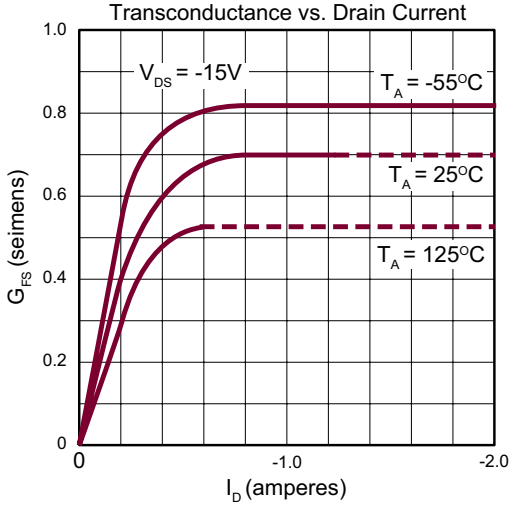
Output Characteristics



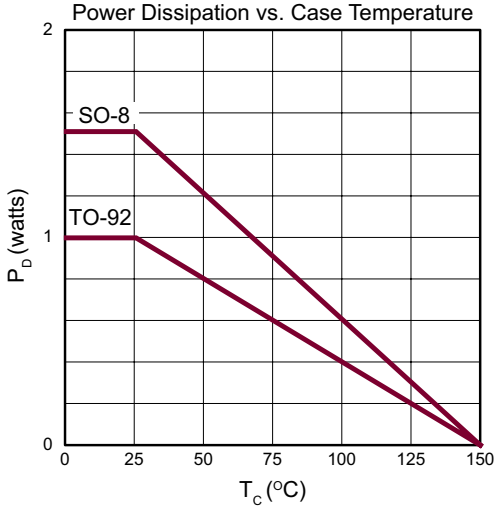
Saturation Characteristics



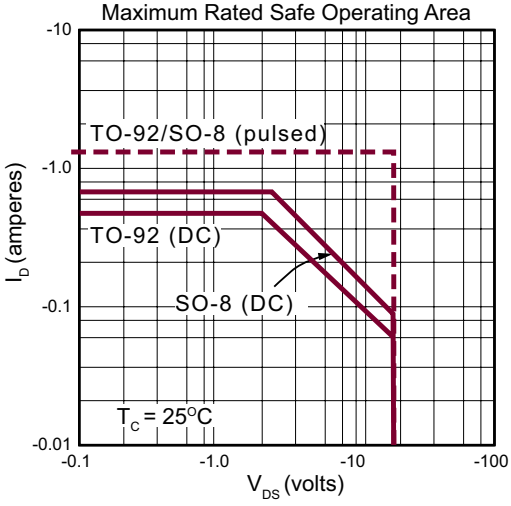
Transconductance vs. Drain Current



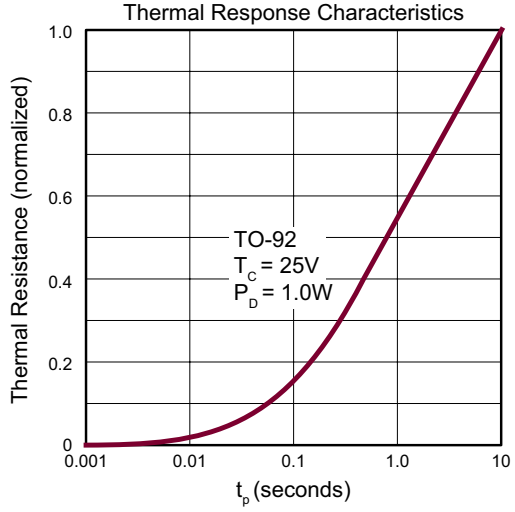
Power Dissipation vs. Case Temperature



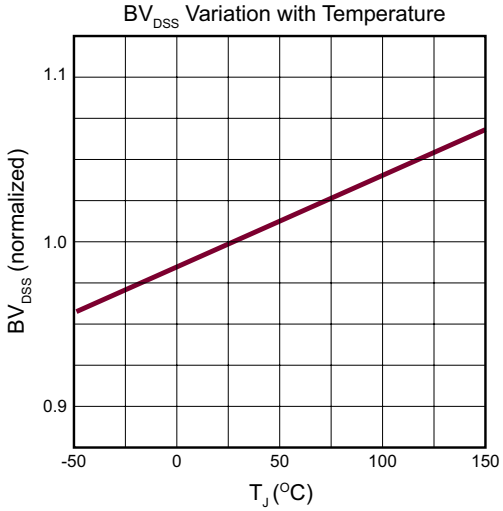
Maximum Rated Safe Operating Area

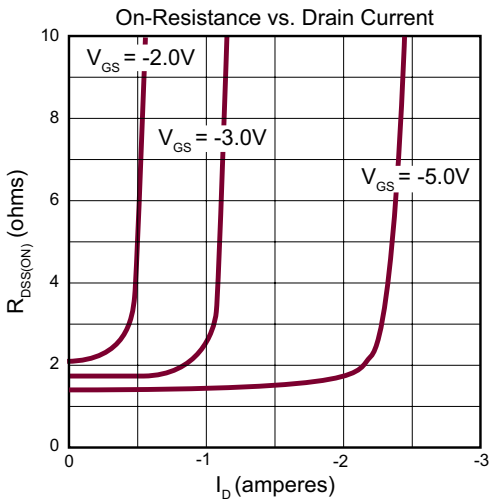


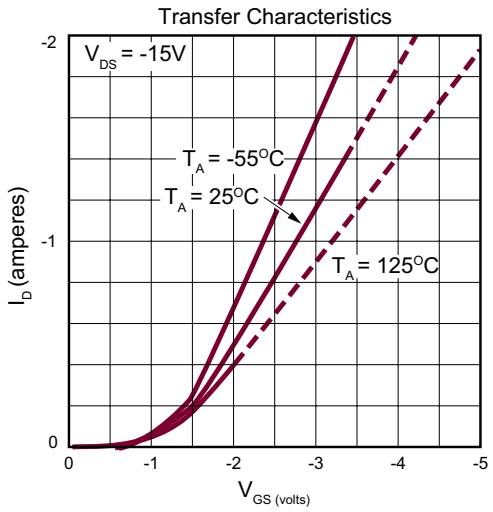
Thermal Response Characteristics

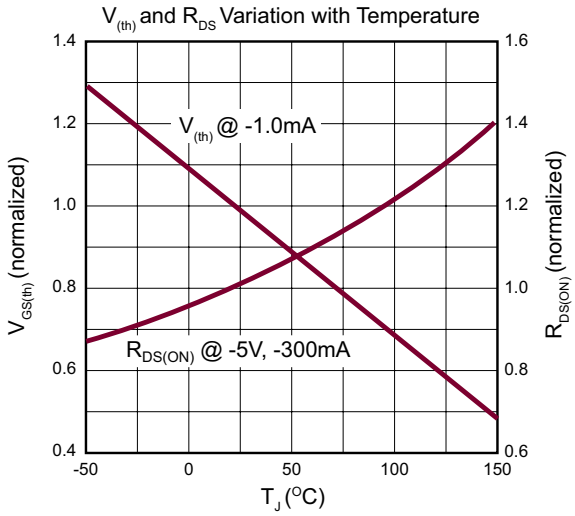


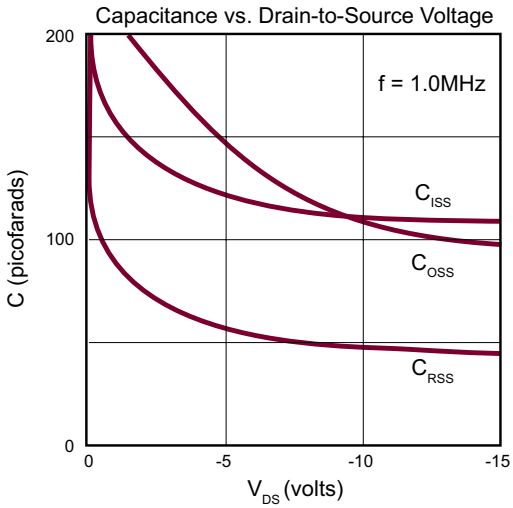
Typical Performance Curves (cont.)

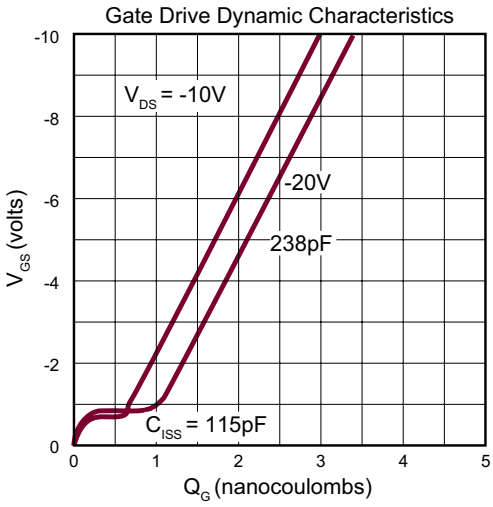


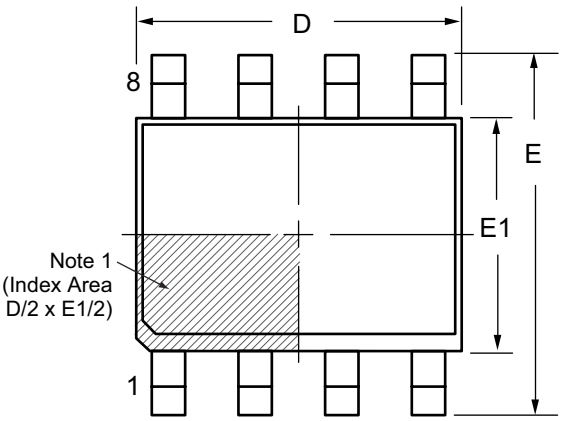




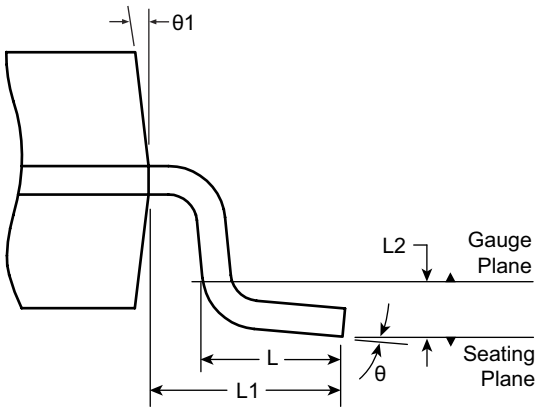




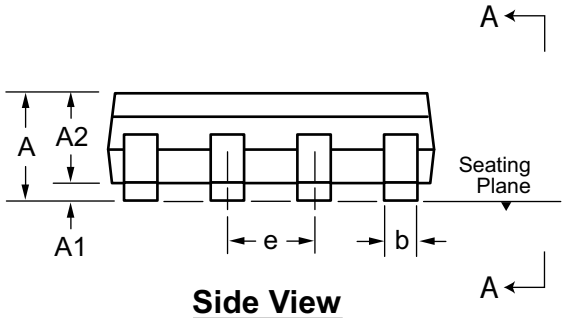




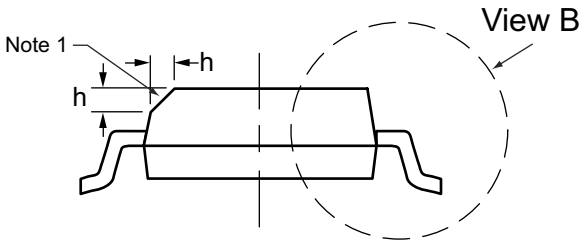
Top View



View B



Side View



View A-A

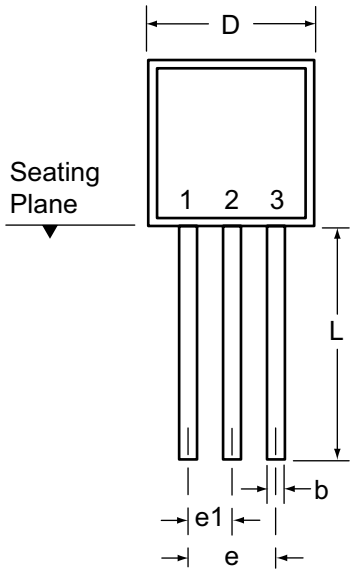
Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

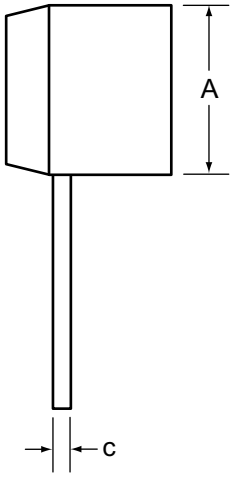
Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
Supertex Doc. #: *DSPD-8SOLGTG, Version I041309.*

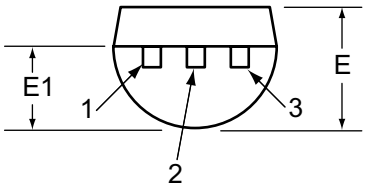
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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