



N-Channel Enhancement-Mode Vertical DMOS FETs

Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low C_{iss} and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options				BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ max (Ω)	$V_{GS(th)}$ max (V)
	TO-92	14-Lead PDIP	TO-243AA (SOT-89)	Die*			
VN3205	VN3205N3-G	VN3205P-G	VN3205N8-G	VN3205ND	50	0.3	2.4

-G indicates package is RoHS compliant ('Green')
* MIL visual screening available.



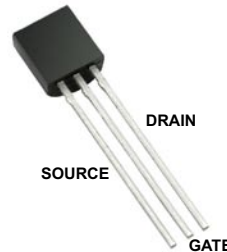
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$+300^{\circ}C$

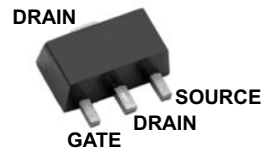
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

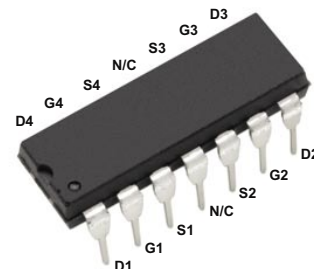
Pin Configurations



TO-92 (N3)



TO-243AA (SOT-89) (N8)



14-Lead PDIP (P)

Product Markings



YY = Year Sealed
 WW = Week Sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)



W = Code for week sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

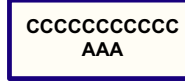
TO-243AA (SOT-89) (N8)

Top Marking



YY = Year Sealed
 WW = Week Sealed
 L = Lot Number
 C = Country of Origin*
 A = Assembler ID*
 _____ = "Green" Packaging

Bottom Marking



*May be part of top marking

Package may or may not include the following marks: Si or

14-Lead PDIP (P)

Thermal Characteristics

Package	I _D (continuous) [*] (A)	I _D (pulsed) (A)	Power Dissipation @T _c = 25°C (W)	θ _{jc} (°C/W)	θ _{ja} (°C/W)	I _{DR} [†] (A)	I _{DRM} (A)
TO-92	1.2	8.0	1.0	125	170	1.2	8.0
14-Lead PDIP	1.5	8.0	3.0 [‡]	41.6 [‡]	83.3 [‡]	1.5	8.0
TO-243AA	1.5	8.0	1.6 (T _A = 25°)	15	78 [‡]	1.5	8.0

Notes:

- * I_D (continuous) is limited by max rated T_J, T_A = 25°C.
- † Total for package.
- ‡ Mounted on FR5 board, 25mm x 25mm x 1.57mm.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions	
BV _{DSS}	Drain-to-source breakdown voltage	50	-	-	V	V _{GS} = 0V, I _D = 10mA	
V _{GS(th)}	Gate threshold voltage	0.8	-	2.4	V	V _{GS} = V _{DS} , I _D = 10mA	
ΔV _{GS(th)}	Change in V _{GS(th)} with temperature	-	-4.3	-5.5	mV/°C	V _{GS} = V _{DS} , I _D = 10mA	
I _{GSS}	Gate body leakage current	-	1.0	100	nA	V _{GS} = ±20V, V _{DS} = 0V	
I _{DSS}	Zero gate voltage drain current	-	-	10	μA	V _{GS} = 0V, V _{DS} = Max Rating	
		-	-	1.0	mA	V _{DS} = 0.8 Max Rating, V _{GS} = 0V, T _A = 125°C	
I _{D(ON)}	On-state drain current	3.0	14	-	A	V _{GS} = 10V, V _{DS} = 5.0V	
R _{DS(ON)}	Static drain-to-source on-state resistance	TO-92 and PDIP	-	-	0.45	Ω	V _{GS} = 4.5V, I _D = 1.5A
		TO-243AA	-	-	0.45		V _{GS} = 4.5V, I _D = 0.75A
		TO-92 and PDIP	-	-	0.3		V _{GS} = 10V, I _D = 3.0A
		TO-243AA	-	-	0.3		V _{GS} = 10V, I _D = 1.5A
ΔR _{DS(ON)}	Change in R _{DS(ON)} with temperature	-	0.85	1.2	%/°C	V _{GS} = 10V, I _D = 3.0A	
G _{FS}	Forward transconductance	1.0	1.5	-	mho	V _{DS} = 25V, I _D = 2.0A	

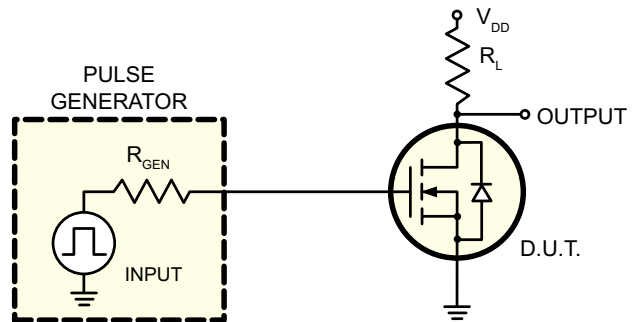
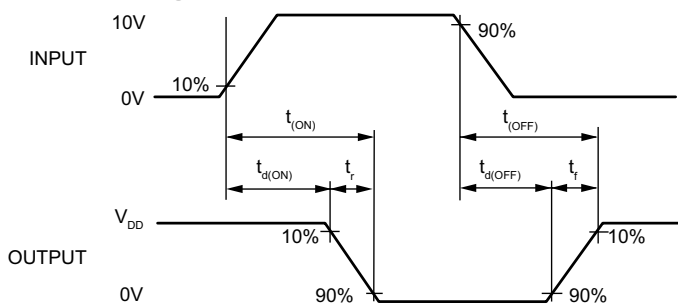
Electrical Characteristics (cont.) ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
C_{ISS}	Input capacitance	-	220	300	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0\text{MHz}$
C_{OSS}	Common source output capacitance	-	70	120		
C_{RSS}	Reverse transfer capacitance	-	20	30		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = 25V,$ $I_D = 2.0A,$ $R_{GEN} = 10\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	25		
t_f	Fall time	-	-	25		
V_{SD}	Diode forward voltage drop	-	-	1.6	V	$V_{GS} = 0V, I_{SD} = 1.5A$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 1.0A$

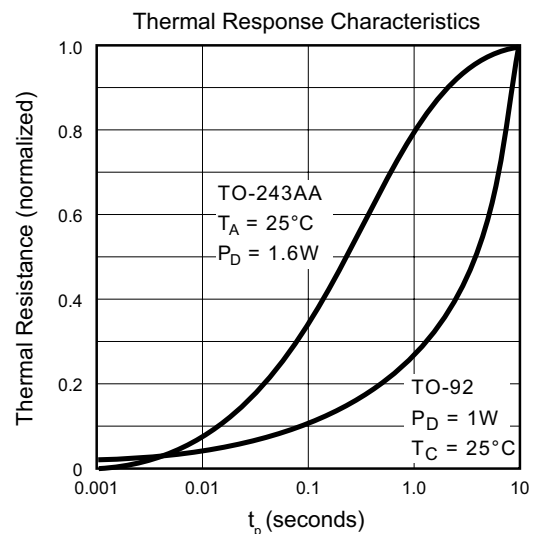
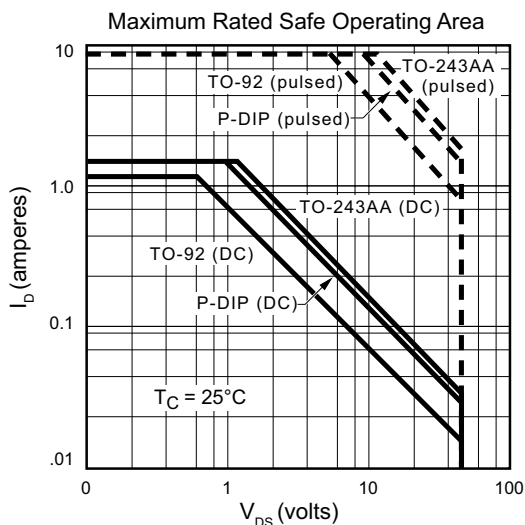
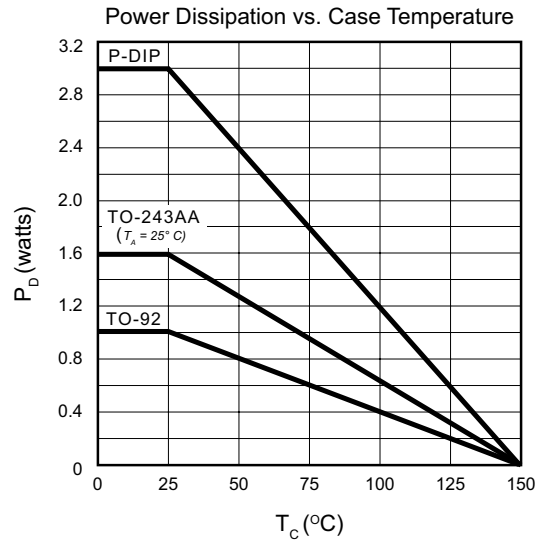
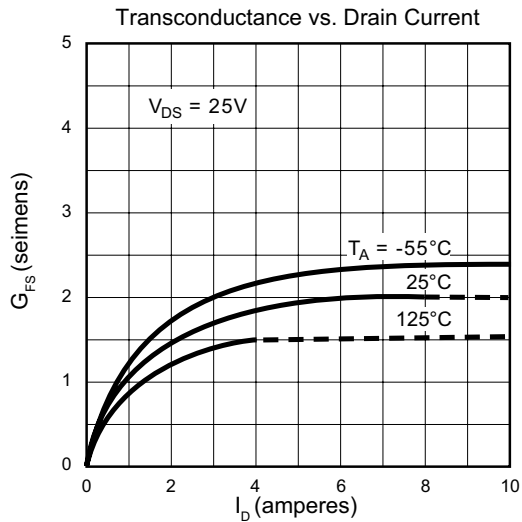
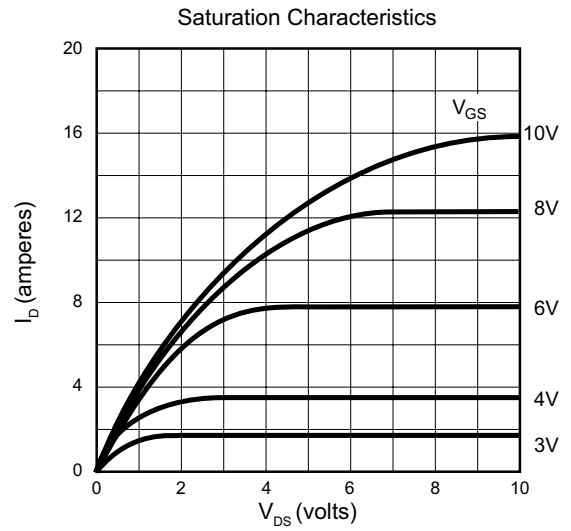
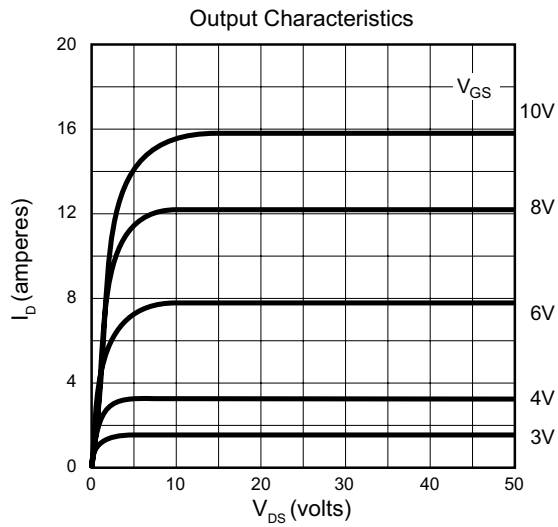
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu\text{s}$ pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

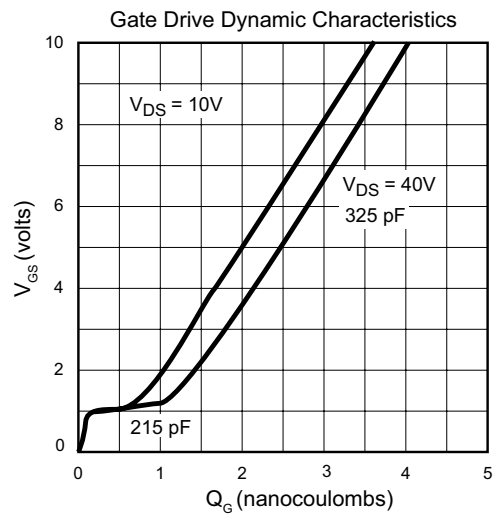
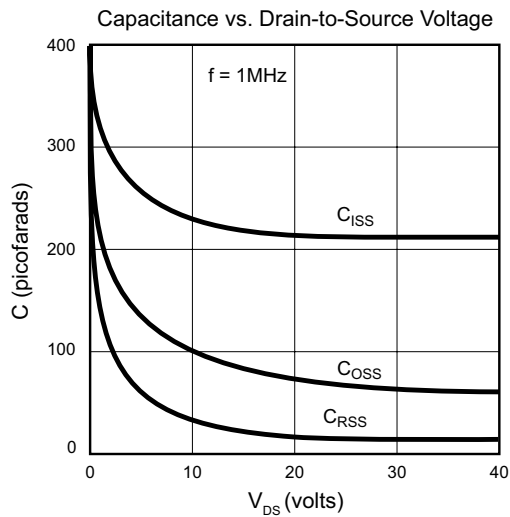
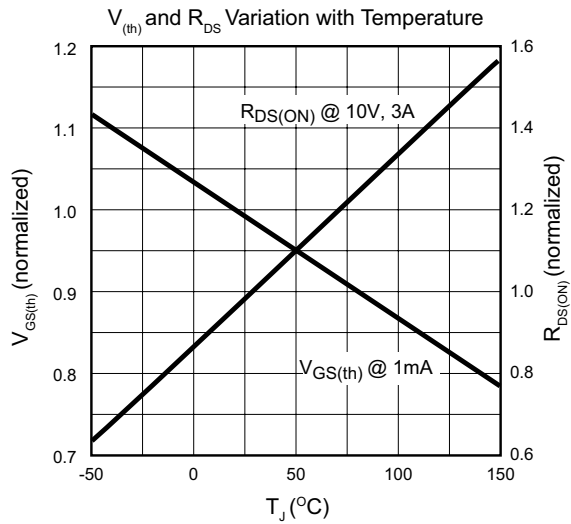
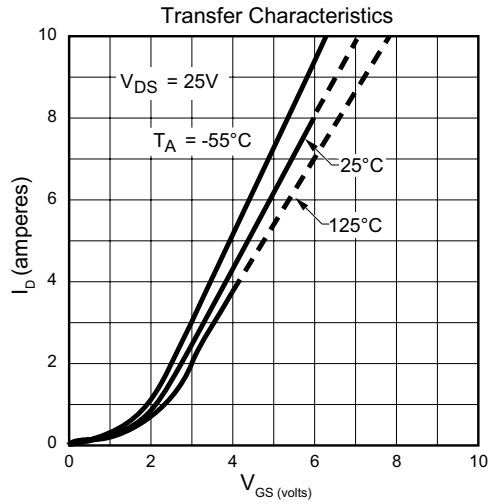
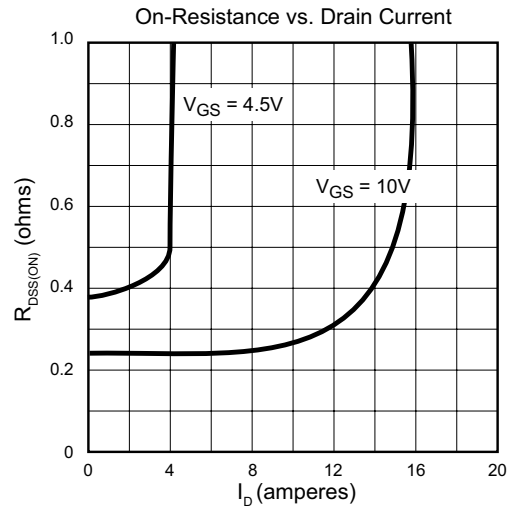
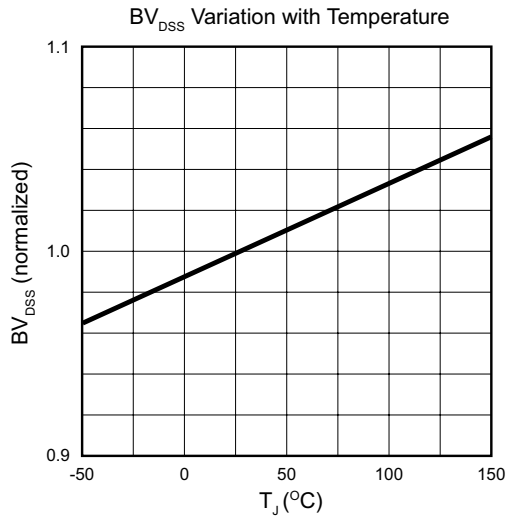
Switching Waveforms and Test Circuit



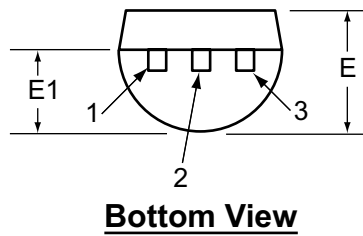
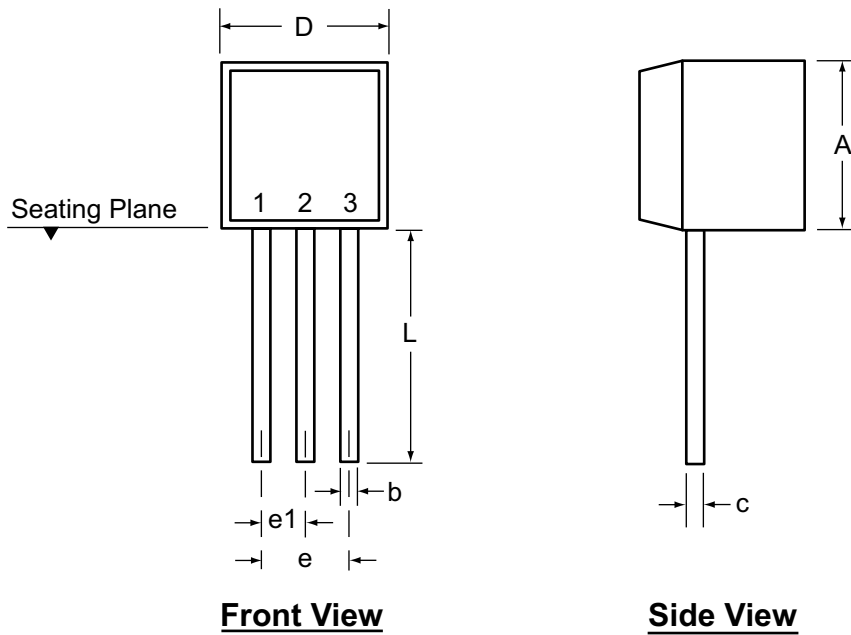
Typical Performance Curves



Typical Performance Curves (cont.)



3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

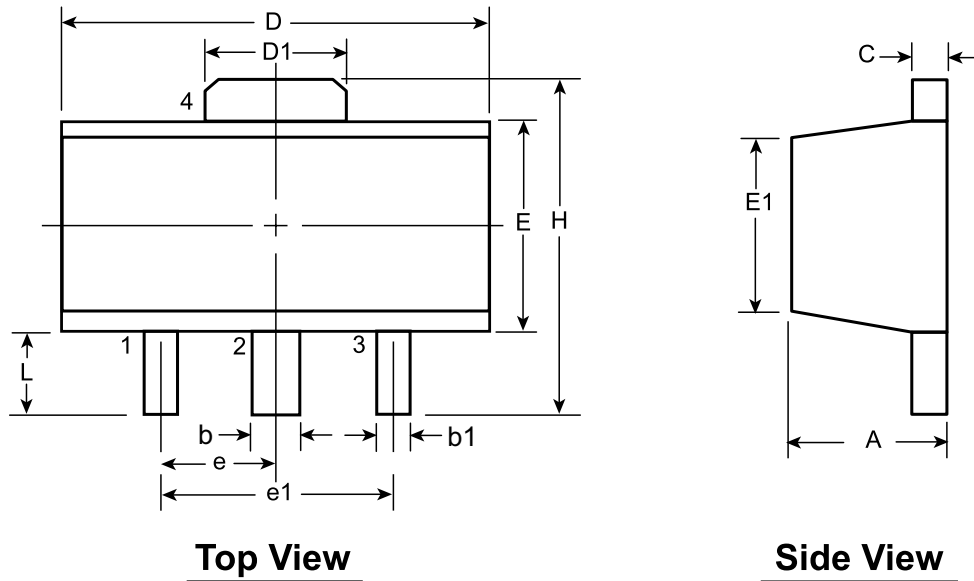
* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00 [†]	1.50 BSC	3.00 BSC	3.94	0.89
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

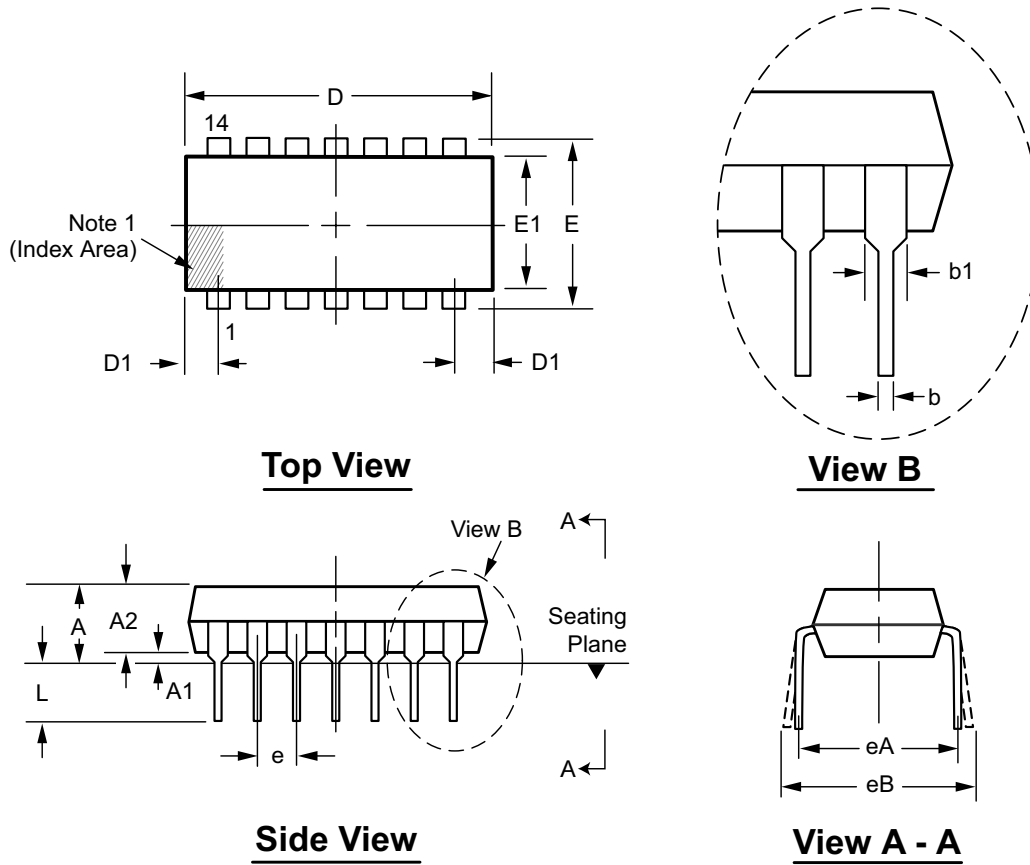
[†] This dimension differs from the JEDEC drawing

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version E051509.

14-Lead PDIP (.300in Row Spacing) Package Outline (P)

.750x.250in body, .210in height (max), .100in pitch



Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	eA	eB	L	
Dimension (inches)	MIN	.130*	.015	.115	.014	.045	.735	.065†	.290†	.240	.100 BSC	.300 BSC	.300*	.115
	NOM	-	-	.130	.018	.060	.750	-	.310	.250			-	.130
	MAX	.210	.035*	.195	.023†	.070	.810†	.085*	.325	.280			.430	.150

JEDEC Registration MS-001, Variation AA, Issue D, June, 1993.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-14DIPP, Version B041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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