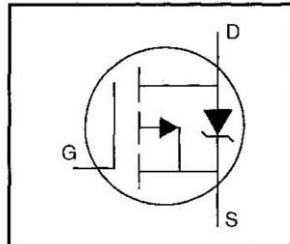


IRFI9620GPbF

HEXFET® Power MOSFET

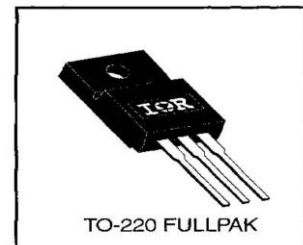
- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- P-Channel
- Dynamic dv/dt Rating
- Low Thermal Resistance
- Lead-Free



$$V_{DSS} = -200V$$

$$R_{DS(on)} = 1.5\Omega$$

$$I_D = -3.0A$$



Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-3.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-1.9	
I_{DM}	Pulsed Drain Current ①	-12	
$P_D @ T_C = 25^\circ C$	Power Dissipation	30	W
	Linear Derating Factor	0.24	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	80	mJ
I_{AR}	Avalanche Current ①	-3.0	A
E_{AR}	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} =0V, I _D =-250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.22	—	V/°C	Reference to 25°C, I _D =-1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V _{GS} =-10V, I _D =-1.8A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} =V _{GS} , I _D =-250μA
g _{fs}	Forward Transconductance	1.3	—	—	S	V _{DS} =-50V, I _D =-1.8A ④
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} =-200V, V _{GS} =0V
		—	—	-500	μA	V _{DS} =-160V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} =-20V
	Gate-to-Source Reverse Leakage	—	—	100	nA	V _{GS} =20V
Q _g	Total Gate Charge	—	—	15	nC	I _D =-2.1A
Q _{gs}	Gate-to-Source Charge	—	—	3.2	nC	V _{DS} =-160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.4	nC	V _{GS} =-10V See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	8.8	—	ns	V _{DD} =-100V
t _r	Rise Time	—	27	—		I _D =-3.9A
t _{d(off)}	Turn-Off Delay Time	—	7.3	—		R _G =18Ω
t _f	Fall Time	—	19	—		R _D =24Ω See Figure 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	340	—	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	110	—		V _{DS} =-15V
C _{rss}	Reverse Transfer Capacitance	—	33	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—		f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-3.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-12		
V _{SD}	Diode Forward Voltage	—	—	-6.3	V	T _J =25°C, I _S =-3.0A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	150	300	ns	T _J =25°C, I _F =-3.9A
Q _{rr}	Reverse Recovery Charge	—	0.97	2.0	μC	di/dt=100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V_{DD}=-50V, starting T_J=25°C, L=13mH R_G=25Ω, I_{AS}=-3.0A (See Figure 12)
- ③ I_{SD}≤-3.9A, di/dt≤95A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.
- ⑤ t=60s, f=60Hz

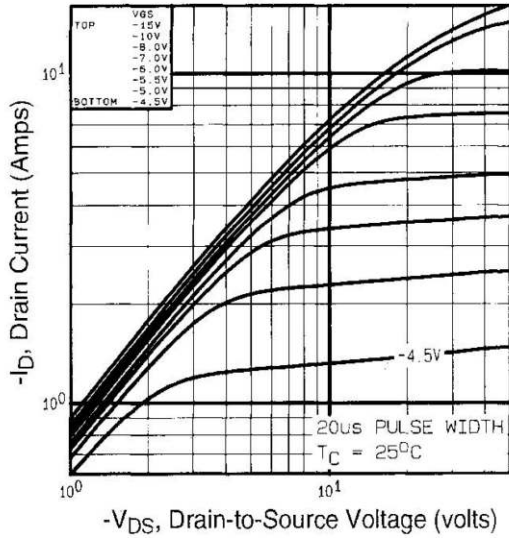


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

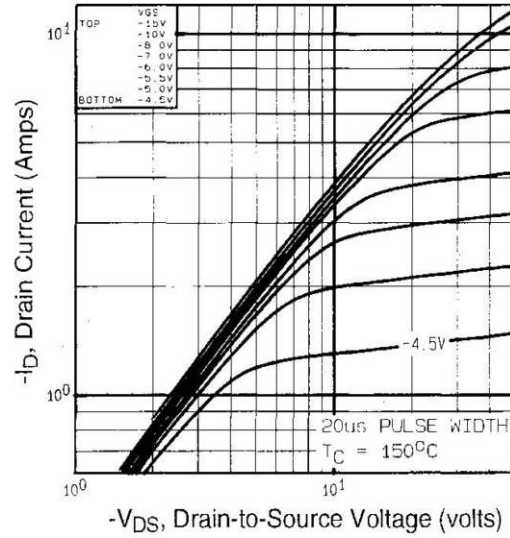


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

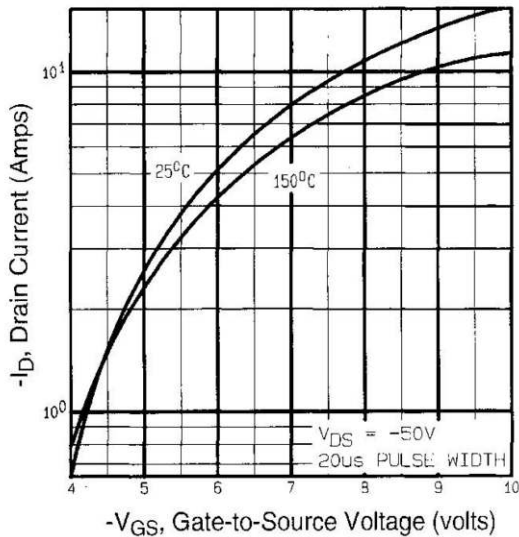


Fig 3. Typical Transfer Characteristics

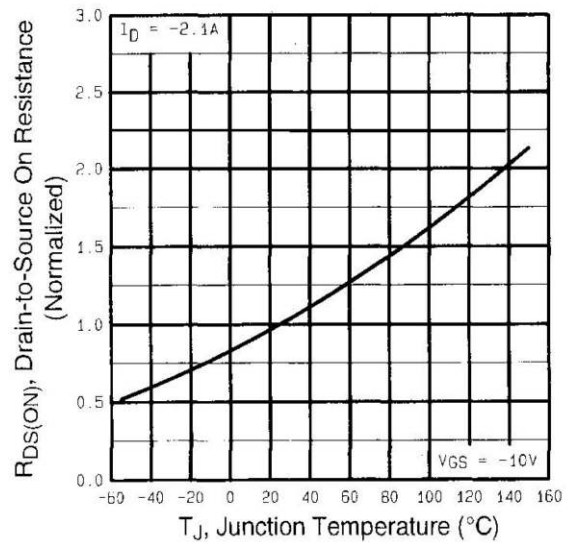


Fig 4. Normalized On-Resistance
 Vs. Temperature

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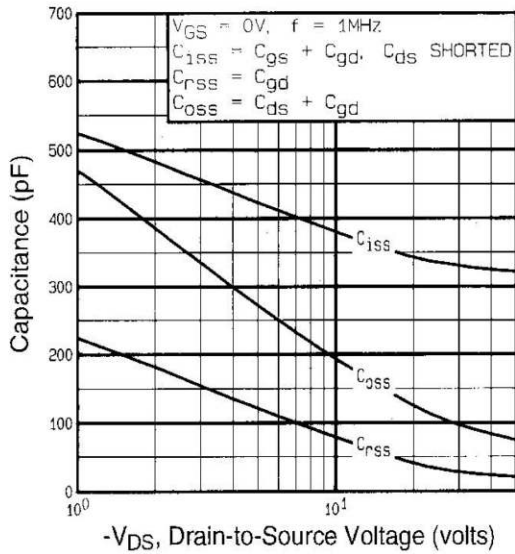


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

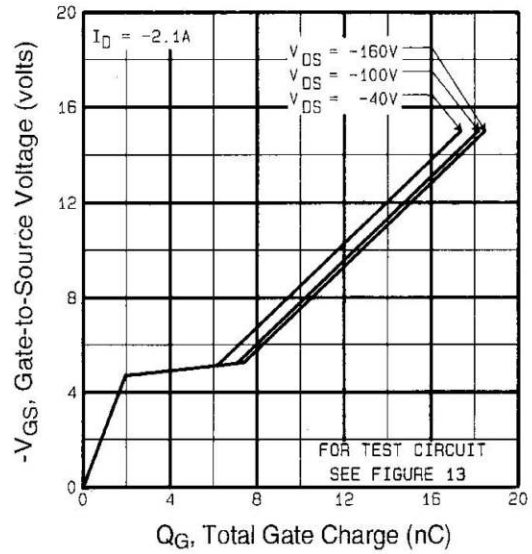


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

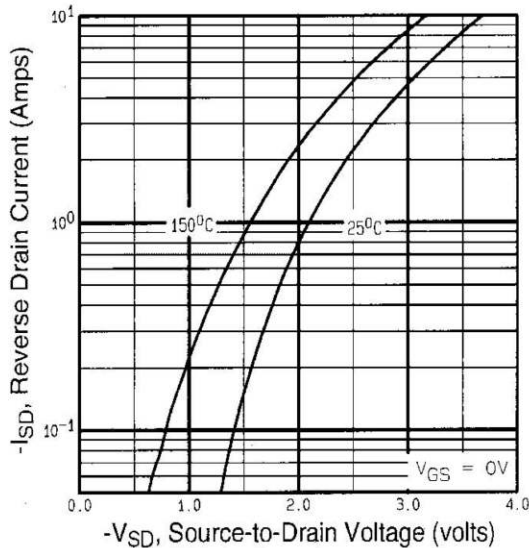


Fig 7. Typical Source-Drain Diode Forward Voltage

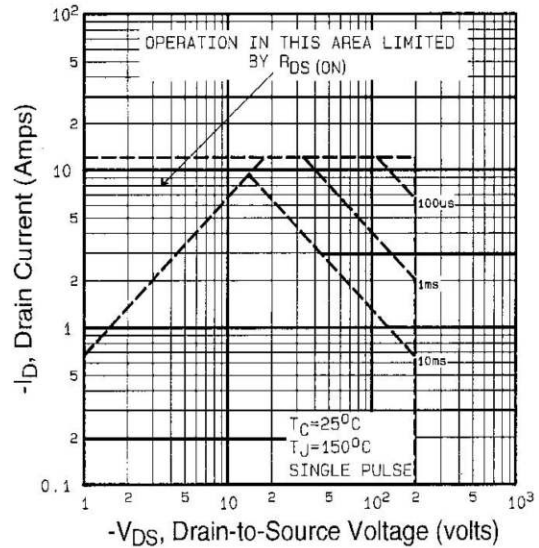


Fig 8. Maximum Safe Operating Area

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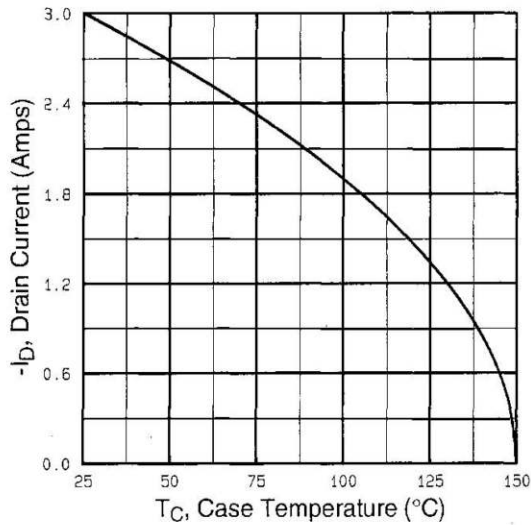


Fig 9. Maximum Drain Current Vs. Case Temperature

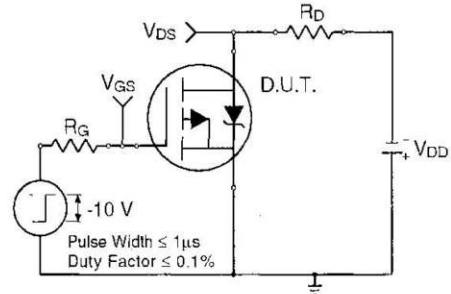


Fig 10a. Switching Time Test Circuit

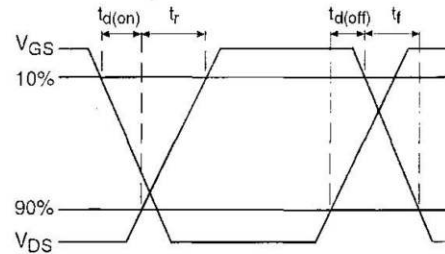


Fig 10b. Switching Time Waveforms

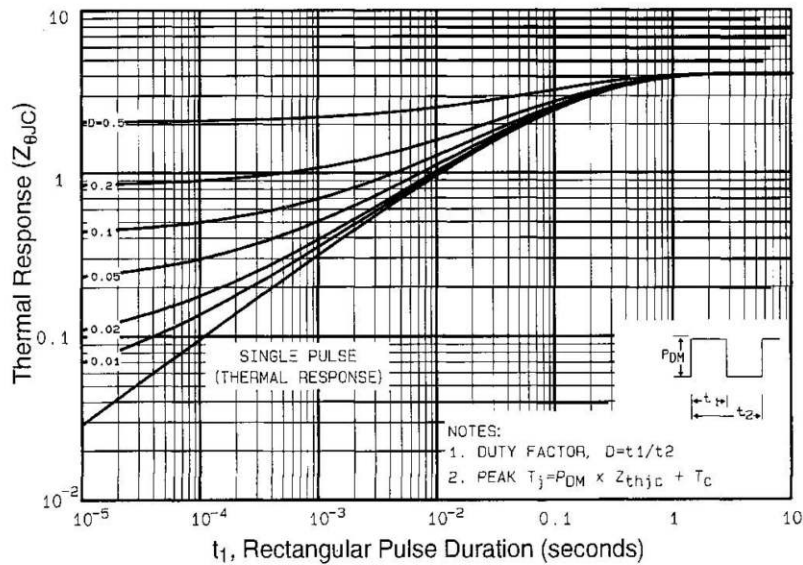


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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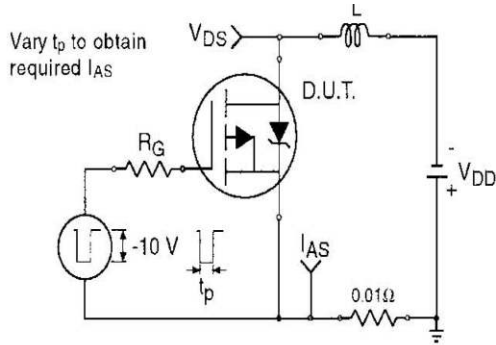


Fig 12a. Unclamped Inductive Test Circuit

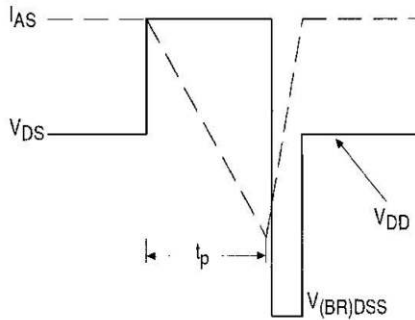


Fig 12b. Unclamped Inductive Waveforms

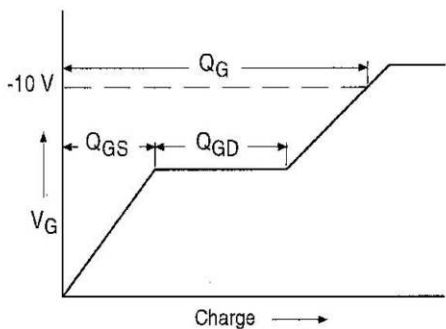


Fig 13a. Basic Gate Charge Waveform

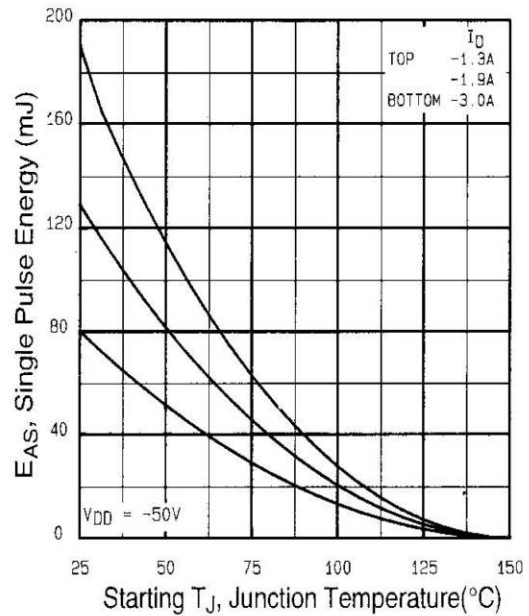


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

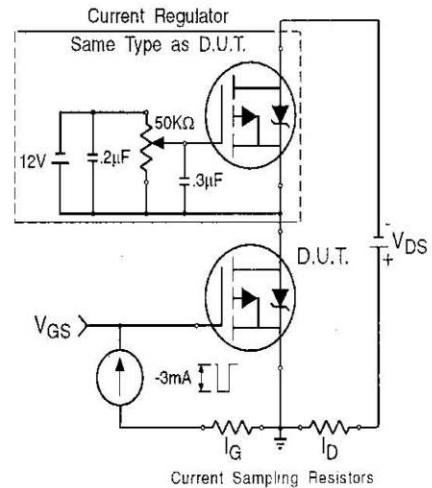
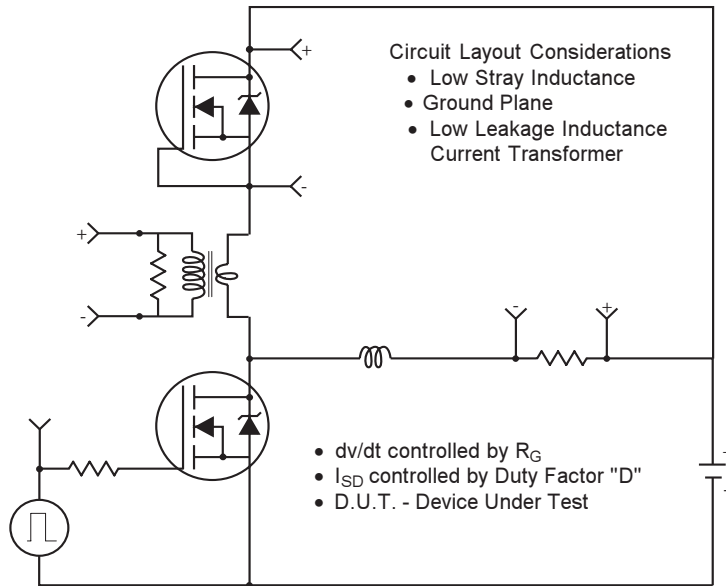


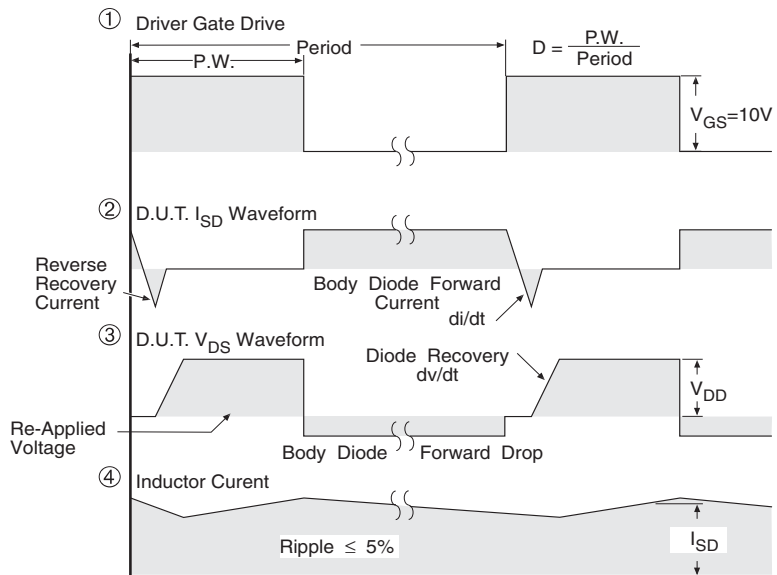
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

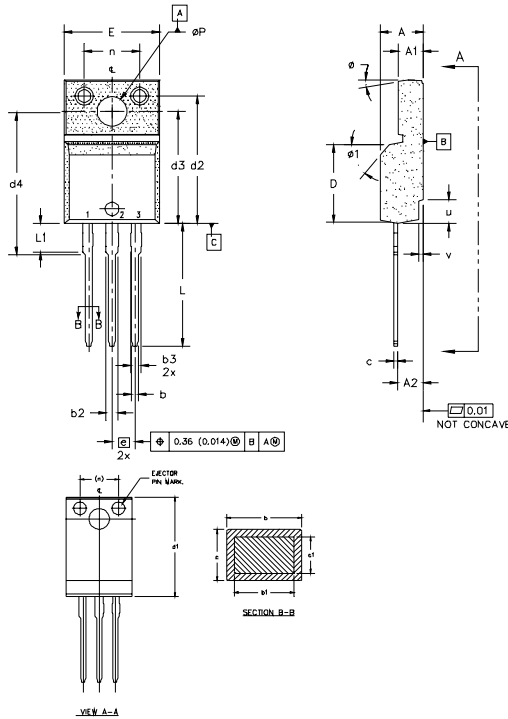
Fig -14 For P Channel HEXFETS

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TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)

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- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5.0 DIMENSION ø1 APPLY TO BASE METAL ONLY.
 - 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
 - 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	0.180	0.190	
A1	2.97	2.85	0.101	0.114	
A2	2.51	2.85	0.099	0.112	
b	0.622	0.89	0.024	0.035	
b1	0.622	0.838	0.024	0.033	5
b2	1.229	1.400	0.048	0.055	
b3	1.229	1.400	0.048	0.055	
c	0.440	0.529	0.017	0.025	
ct	0.440	0.584	0.017	0.023	
D	8.65	9.80	0.341	0.386	4
d1	15.80	16.12	0.622	0.635	
d2	13.97	14.22	0.550	0.560	
d3	12.30	12.92	0.484	0.509	
d4	8.64	9.91	0.340	0.390	4
E	10.36	10.63	0.408	0.419	
e	2.54 BSC		0.100 BSC		
L	13.20	13.73	0.520	0.541	
L1	3.10	3.50	0.122	0.138	3
n	6.05	6.16	0.238	0.242	
n1	3.05	3.45	0.120	0.136	
p	2.40	2.50	0.094	0.098	6
v	0.40	0.50	0.016	0.020	6
w	3"	45"	3"	45"	
ø1					

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

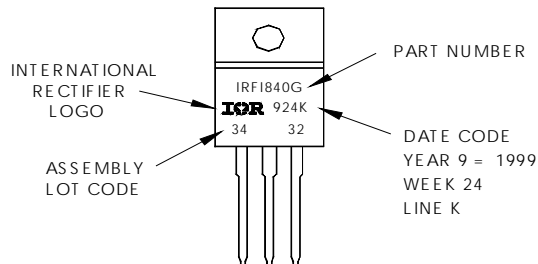
IGBTs CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International
IR Rectifier

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TAC Fax: (310) 252-7903
08/04

Document Number: 91166

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