

P-Channel 1.2-V (G-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 8	0.035 at $V_{GS} = -4.5$ V	- 11.7	21 nC
	0.042 at $V_{GS} = -2.5$ V	- 10.7	
	0.052 at $V_{GS} = -1.8$ V	- 9.6	
	0.069 at $V_{GS} = -1.5$ V	- 8.3	
	0.098 at $V_{GS} = -1.2$ V	- 1.02	

FEATURES

- TrenchFET[®] Power MOSFET
- Industry First 1.2 V Rated MOSFET
- Ultra Small MICRO FOOT[®] Chipscale Packaging Reduces Footprint Area, Profile (0.62 mm) and On-Resistance Per Footprint Area

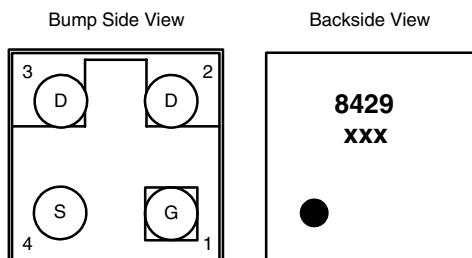


RoHS
COMPLIANT

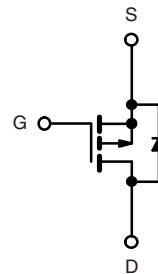
APPLICATIONS

- Low Threshold Load Switch for Portable Devices
 - Low Power Consumption
 - Increased Battery Life
- Ultra Low Voltage Load Switch

MICRO FOOT



Device Marking: 8429
xxx = Date/Lot Traceability Code



Ordering Information: Si8429DB-T1-E1 (Lead (Pb)-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 8	V
Gate-Source Voltage	V_{GS}	± 5	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	- 11.7
		$T_C = 70$ °C	- 9.4
		$T_A = 25$ °C	- 7.8 ^{b, c}
		$T_A = 70$ °C	- 6.3 ^{b, c}
Pulsed Drain Current	I_{DM}	- 25	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	- 2.5 ^{b, c}
Maximum Power Dissipation	P_D	$T_C = 25$ °C	6.25
		$T_C = 70$ °C	4
		$T_A = 25$ °C	2.77 ^{b, c}
		$T_A = 70$ °C	1.77 ^{b, c}
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions ^d	IR/Convection	260	

Notes:

- Based on $T_C = 25$ °C.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Refer to IPC/JEDEC (J-STD-020C), no manual or hand soldering.
- In this document, any reference to the *Case* represents the body of the MICRO FOOT device and *Foot* is the bump.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	R_{thJA}	35	45	°C/W
Maximum Junction-to-Foot (Drain)	Steady State R_{thJF}	16	20	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 85 °C/W.

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-8			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-7.5		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-2.2		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.35		-0.8	V
		$V_{DS} = V_{GS}, I_D = -5\text{ mA}$		-0.6		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -8\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ °C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5\text{ V}, V_{GS} = -4.5\text{ V}$	-5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -1\text{ A}$		0.029	0.035	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -1\text{ A}$		0.035	0.042	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.043	0.052	
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$		0.051	0.069	
		$V_{GS} = -1.2\text{ V}, I_D = -1\text{ A}$		0.065	0.098	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -4\text{ V}, I_D = -1\text{ A}$		0.7	1.2	S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -4\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1640		pF
Output Capacitance	C_{oss}			590		
Reverse Transfer Capacitance	C_{rss}			380		
Total Gate Charge	Q_g	$V_{DS} = -4\text{ V}, V_{GS} = -5\text{ V}, I_D = -1\text{ A}$		24	26	nC
				21	32	
Gate-Source Charge	Q_{gs}	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = 1\text{ A}$		1.8		
Gate-Drain Charge	Q_{gd}			3.7		
Gate Resistance	R_g	$V_{GS} = -0.1\text{ V}, f = 1\text{ MHz}$		22		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 6\text{ }\Omega$		12	20	ns
Rise Time	t_r			25	40	
Turn-Off Delay Time	$t_{d(off)}$			260	390	
Fall Time	t_f			155	240	



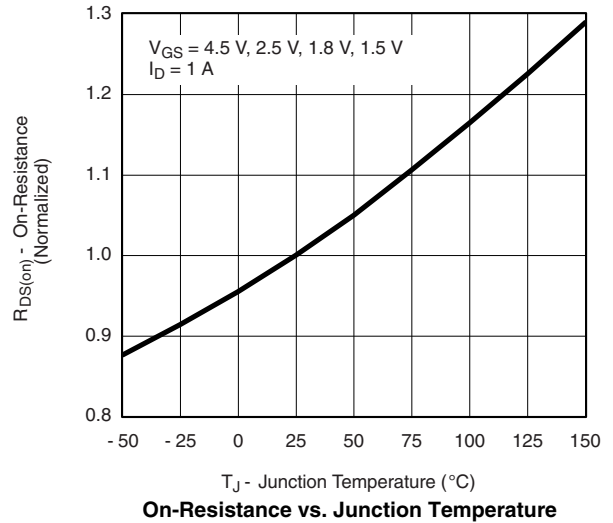
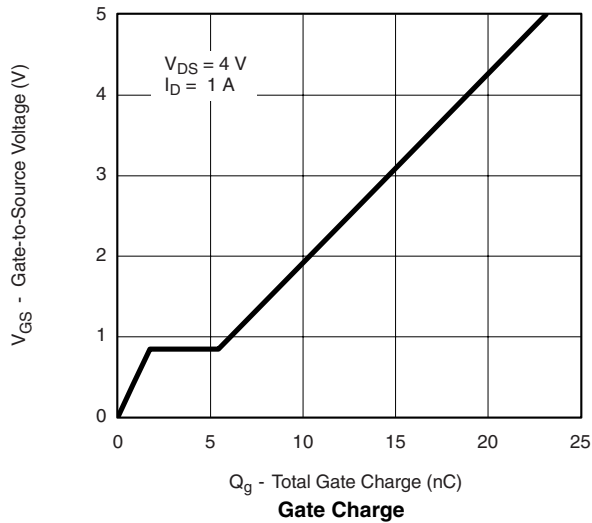
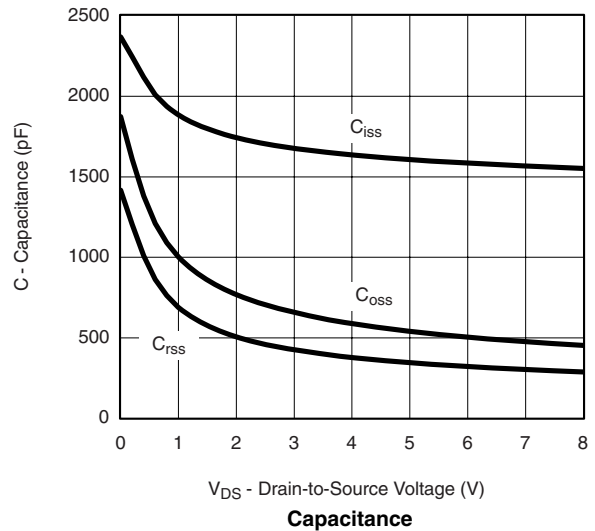
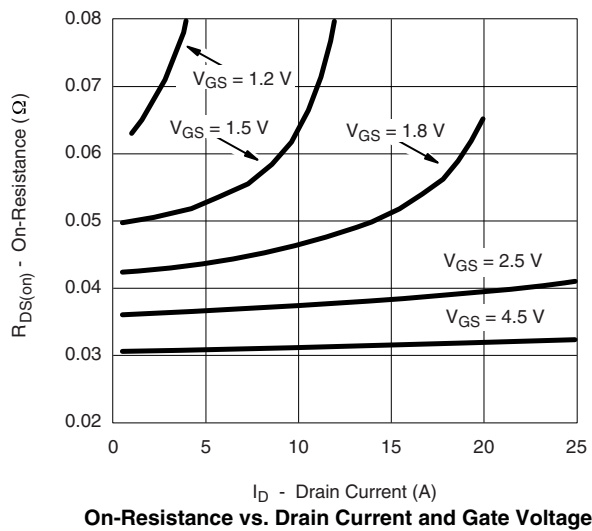
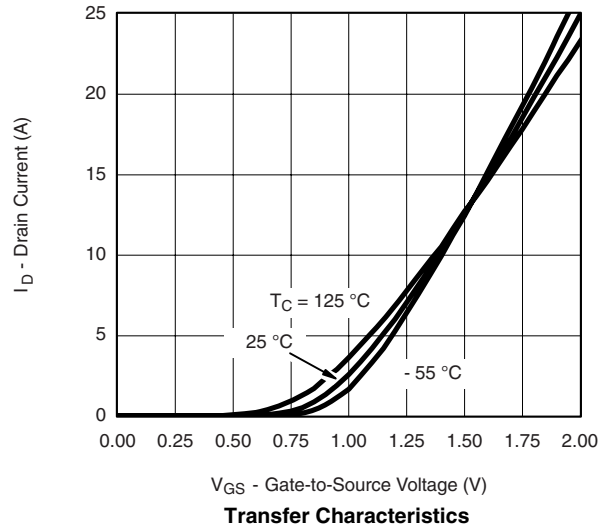
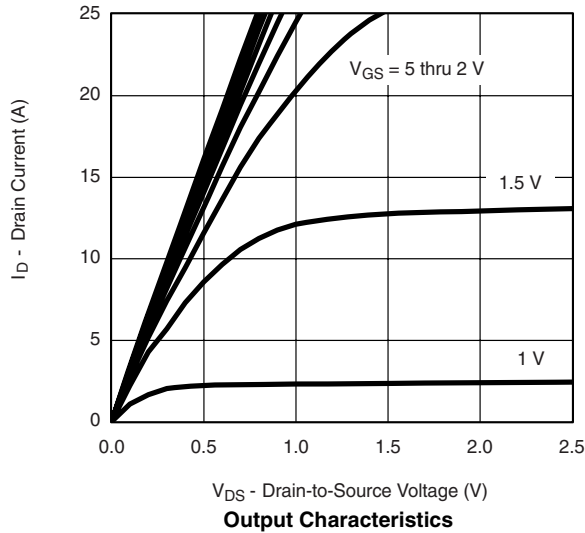
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			- 2.5	A
Pulse Diode Forward Current	I_{SM}				- 25	
Body Diode Voltage	V_{SD}	$I_S = - 1\text{ A}, V_{GS} = 0\text{ V}$		- 0.7	- 1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = - 1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		150	250	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	230	nC
Reverse Recovery Fall Time	t_a			57		ns
Reverse Recovery Rise Time	t_b			93		

Notes:

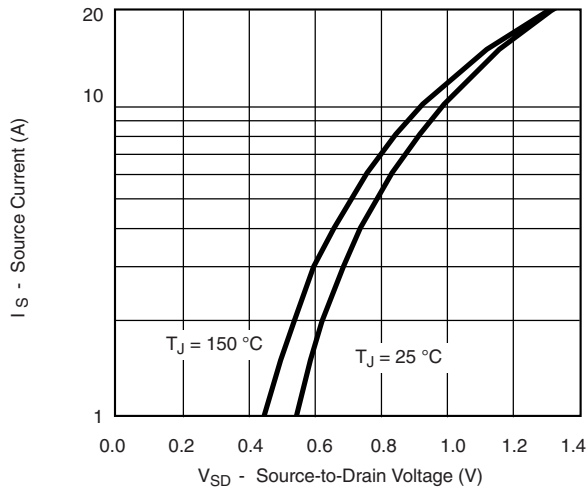
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

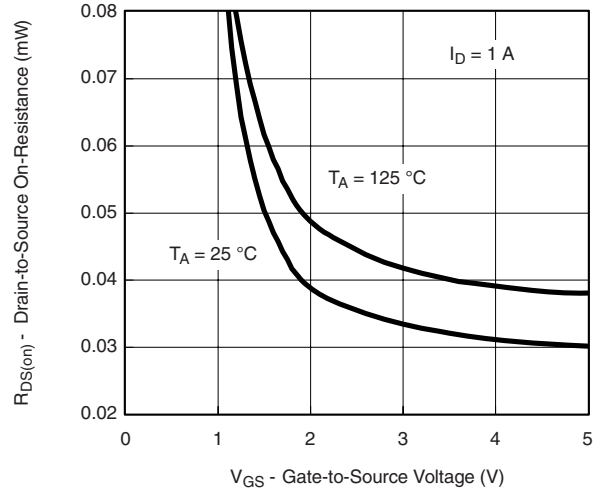
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



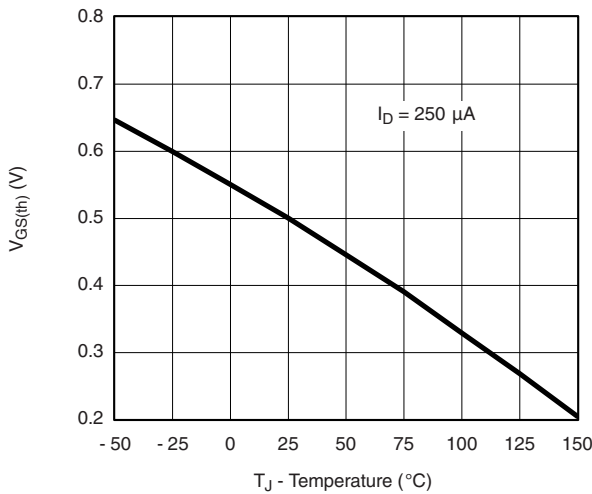
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



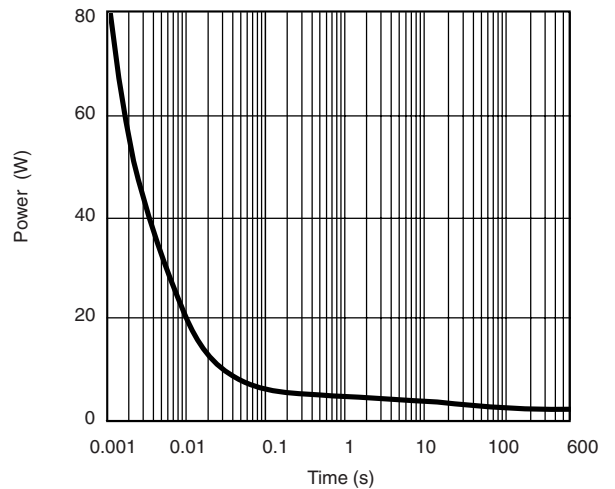
Source-Drain Diode Forward Voltage



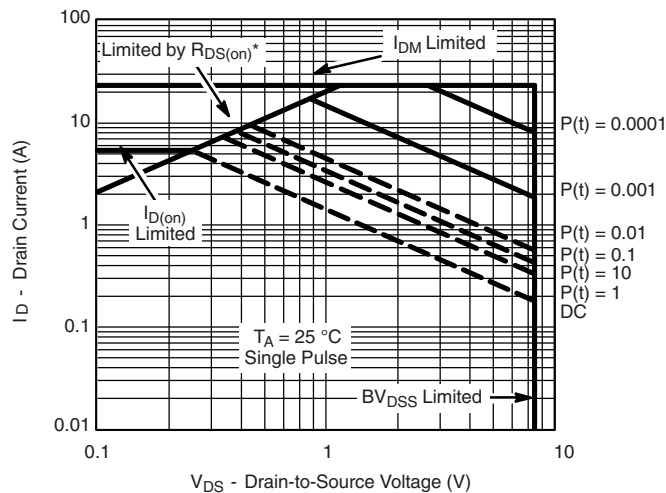
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



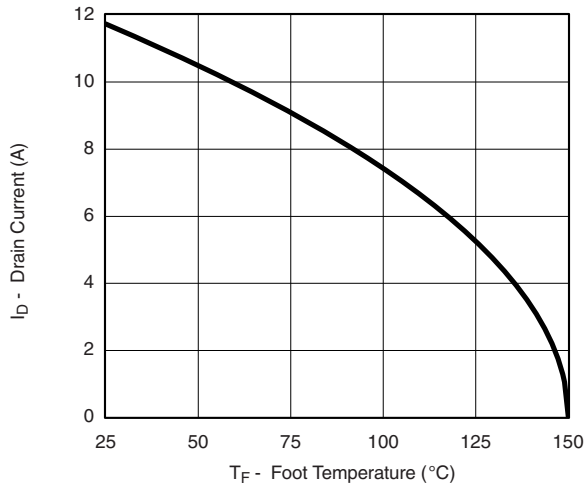
Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

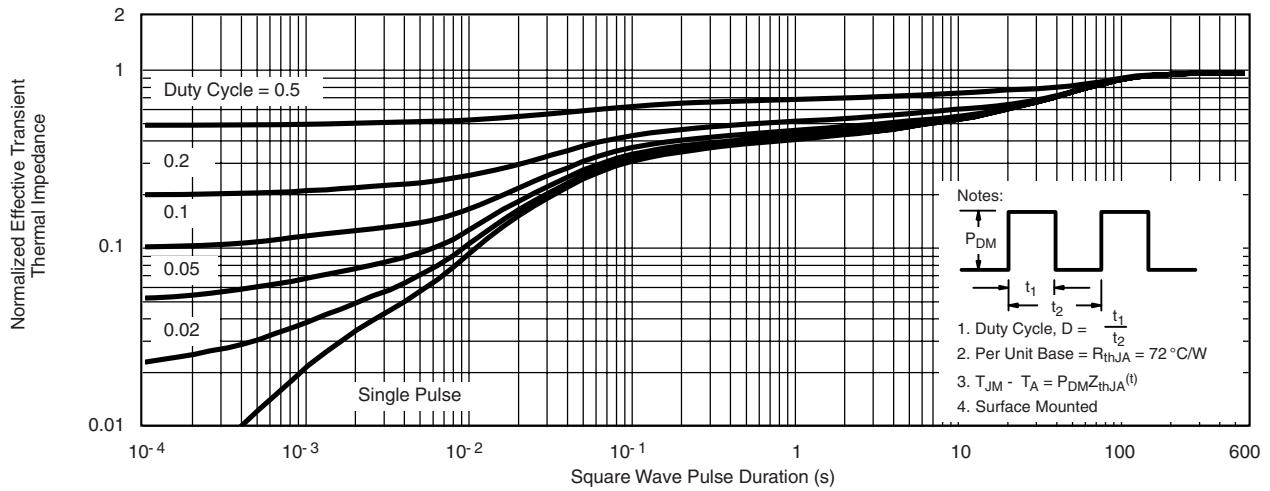
Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

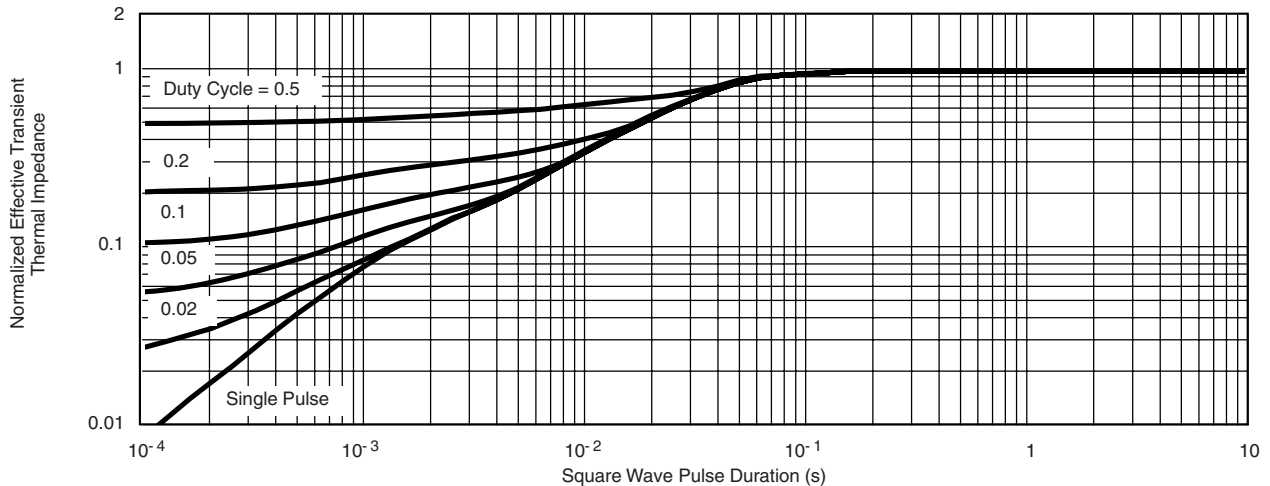


Current Derating*

* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



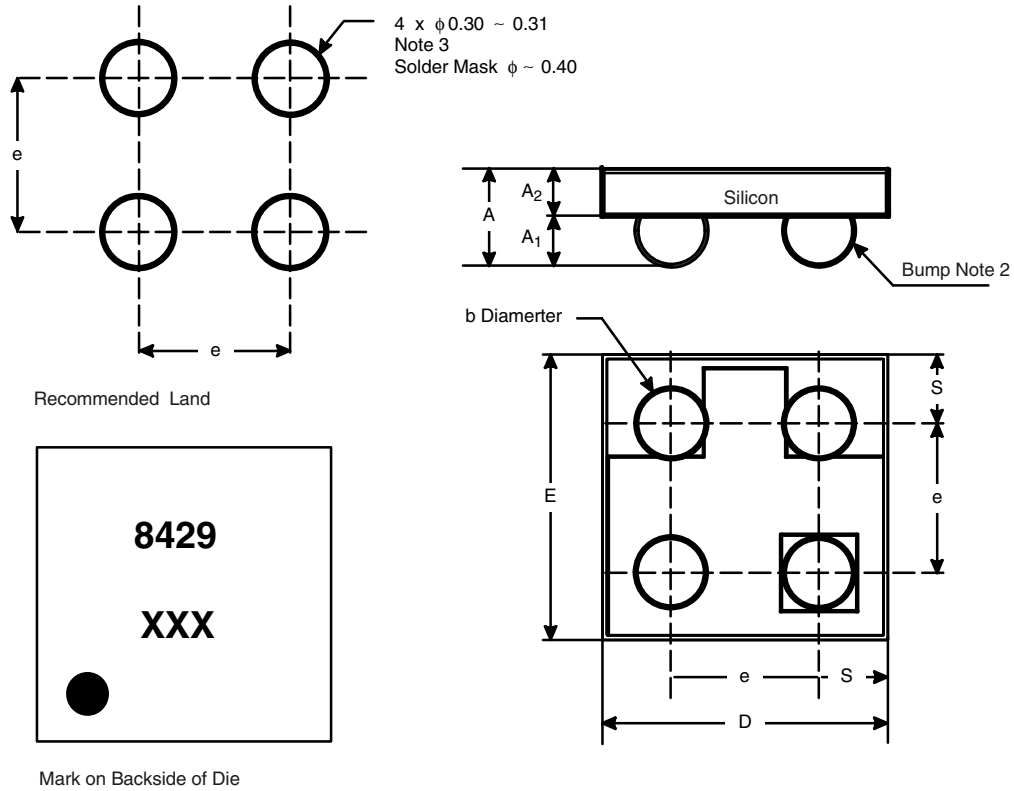
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (2 x 2, 0.8 mm PITCH)



Notes (Unless Otherwise Specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Sn/Ag/Cu.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters ^a		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A ₁	0.260	0.290	0.0102	0.0114
A ₂	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.750	0.850	0.0295	0.0335
S	0.370	0.380	0.0146	0.0150

Notes:

- a. Use millimeters as the primary measurement

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