

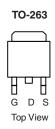
# N-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>(BR)DSS</sub> (V)	$r_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	
100	0.030 at V <sub>GS</sub> = 10 V	40	
	0.034 at V <sub>GS</sub> = 6 V	37.5	

#### **FEATURES**

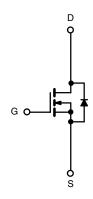
- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package





Ordering Information: SUM40N10-30

SUM40N10-30-E3 (Lead (Pb)-free)



N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
Continuous Drain Current /T 175 °C\	T <sub>C</sub> = 25 °C	1	40		
Continuous Drain Current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 125 °C	I <sub>D</sub>	23	_	
Pulsed Drain Current		I <sub>DM</sub>	75	A .	
Avalanche Current		I <sub>AR</sub>	35		
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AR</sub>	61	mJ	
	T <sub>C</sub> = 25 °C		107 <sup>b</sup>	14/	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C <sup>c</sup>	P <sub>D</sub>	3.75	W	
Operating Junction and Storage Temperature Range		T <sub>.I</sub> , T <sub>sta</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	(PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)		R <sub>thJC</sub>	1.4	J/VV	

#### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).

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<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	<u> </u>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{SS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	100			.,	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1		
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125 \text{ °C}$			50	μΑ	
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 175 \text{ °C}$			250	1	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	75			Α	
Drain-Source On-State Resistance <sup>a</sup>	, ,	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.024	0.030		
	_	$V_{GS} = 6 \text{ V}, I_D = 10 \text{ A}$		0.026	0.034		
	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C			0.054	Ω	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C			0.067		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	10			S	
Dynamic <sup>b</sup>				!			
Input Capacitance	C <sub>iss</sub>			2400		pF	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		270			
Reverse Transfer Capacitance	C <sub>rss</sub>			90			
Total Gate Charge <sup>c</sup>	Qg			35	60	nC	
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 40 \text{ A}$		11			
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			9			
Gate Resistance	$R_{G}$			1.7		Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			11	20	ns	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 1.25 $\Omega$ $I_D$ $\cong$ 40 A, $V_{GEN}$ = 10 V, $R_G$ = 2.5 $\Omega$		12	20		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			30	45		
Fall Time <sup>c</sup>	t <sub>f</sub>			12	20		
Source-Drain Diode Ratings and Cha	aracteristics 7	<sub>C</sub> = 25 °C <sup>b</sup>					
Continuous Current	I <sub>S</sub>				40		
Pulsed Current	I <sub>SM</sub>				75	A	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 30 \text{ A}, V_{GS} = 0 \text{ V}$		1.0	1.5	٧	
Reverse Recovery Time	t <sub>rr</sub>			60	100	ns	
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 30 A, di/dt = 100 A/μs		5	8	Α	
Reverse Recovery Charge	Q <sub>rr</sub>			0.15	0.4	μC	

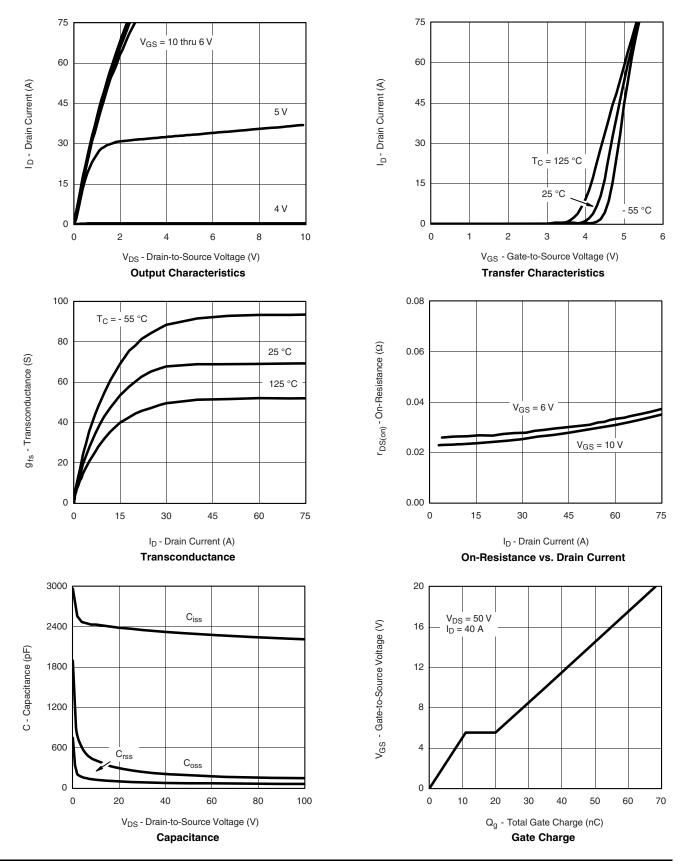
### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

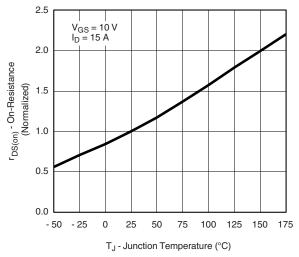


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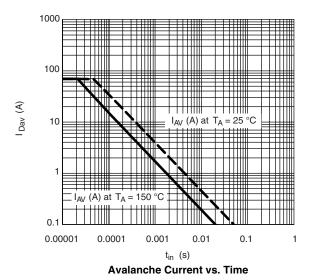
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# VISHAY

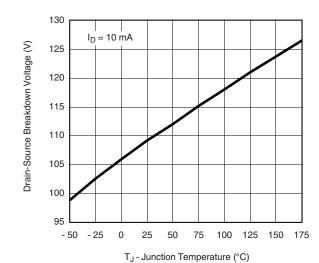
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On-Resistance vs. Junction Temperature



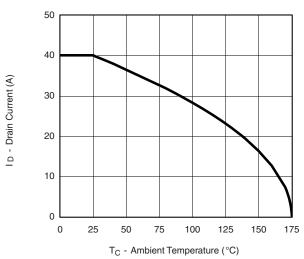
Source-Drain Diode Forward Voltage



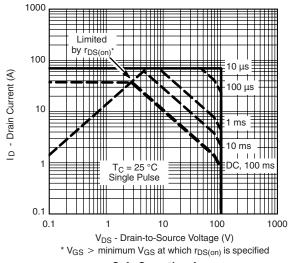
Drain-Source Breakdown Voltage vs. Junction Temperature



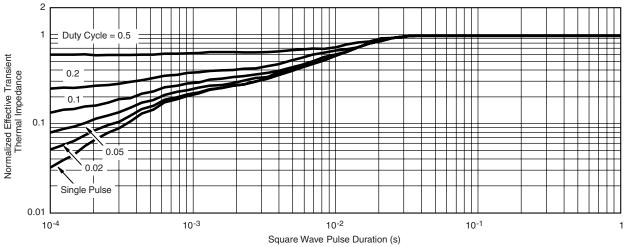
### THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?72134">http://www.vishay.com/ppg?72134</a>.

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