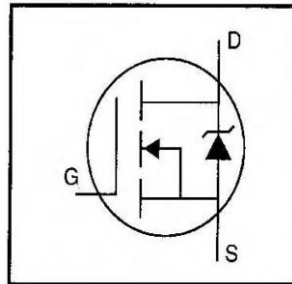


# IRFIBF20GPbF

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance
- Lead-Free



$$V_{DSS} = 900V$$

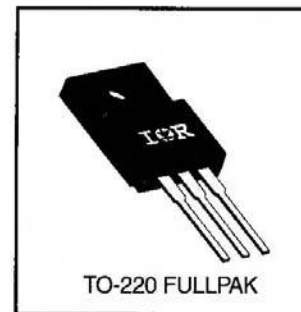
$$R_{DS(on)} = 8.0\Omega$$

$$I_D = 1.2A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	0.79	
$I_{DM}$	Pulsed Drain Current ①	4.8	
$P_D @ T_C = 25^\circ C$	Power Dissipation	30	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	150	mJ
$I_{AR}$	Avalanche Current ①	1.2	A
$E_{AR}$	Repetitive Avalanche Energy ①	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.5	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

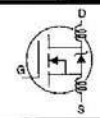
### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

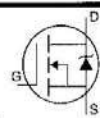
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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	900	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	1.1	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	8.0	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =0.72A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	Forward Transconductance	0.90	—	—	S	V <sub>DS</sub> =50V, I <sub>D</sub> =0.72A ④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	100	μA	V <sub>DS</sub> =900V, V <sub>GS</sub> =0V
		—	—	500		V <sub>DS</sub> =720V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> =20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> =-20V
Q <sub>g</sub>	Total Gate Charge	—	—	38	nC	I <sub>D</sub> =1.7A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	4.7		V <sub>DS</sub> =360V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	21		V <sub>GS</sub> =10V See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.0	—	ns	V <sub>DD</sub> =450V
t <sub>r</sub>	Rise Time	—	21	—		I <sub>D</sub> =1.7A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	56	—		R <sub>G</sub> =18Ω
t <sub>f</sub>	Fall Time	—	32	—		R <sub>D</sub> =280Ω See Figure 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	490	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	Output Capacitance	—	55	—		V <sub>DS</sub> =25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	18	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—		f=1.0MHz

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	1.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	4.8		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =1.2A, V <sub>GS</sub> =0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	350	530	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =1.7A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.85	1.3	μC	di/dt=100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

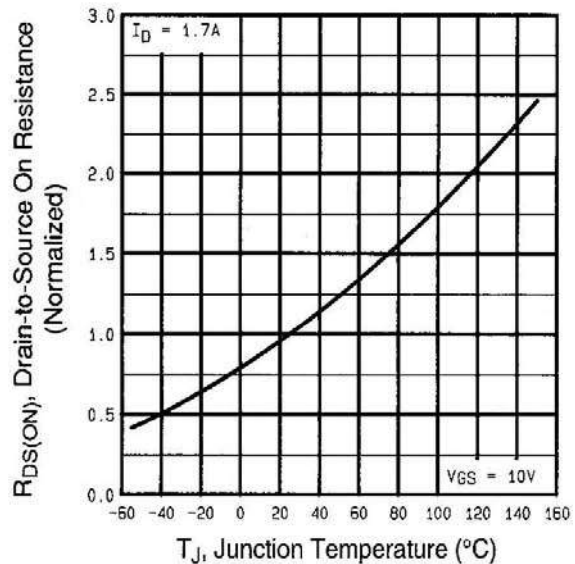
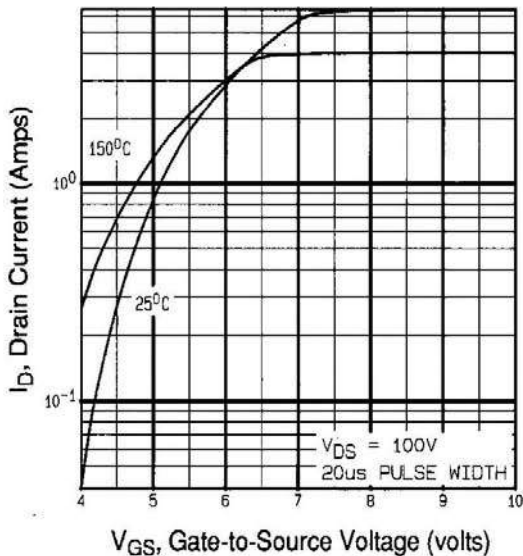
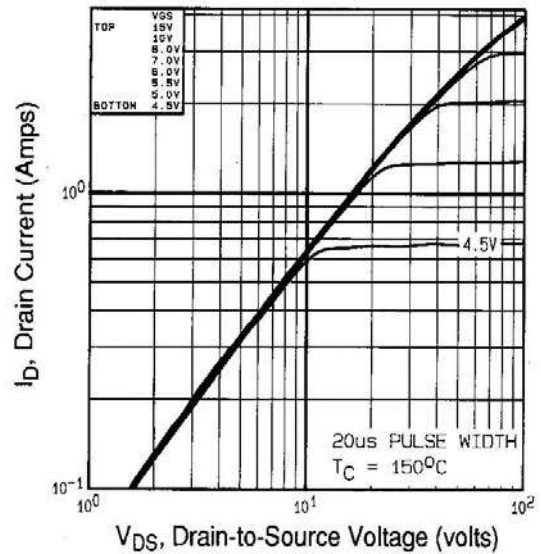
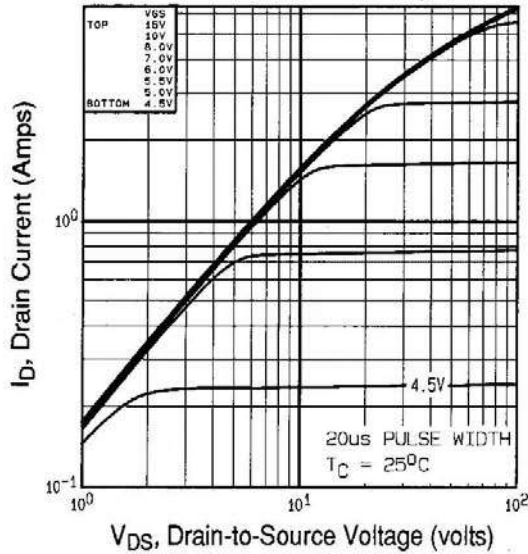
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=196mH, R<sub>G</sub>=25Ω, I<sub>AS</sub>=1.2A (See Figure 12)
- ③ I<sub>SD</sub>≤1.7A, di/dt≤70A/μs, V<sub>DD</sub>≤600, T<sub>J</sub>≤150°C
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%
- ⑤ t=60s, f=60Hz

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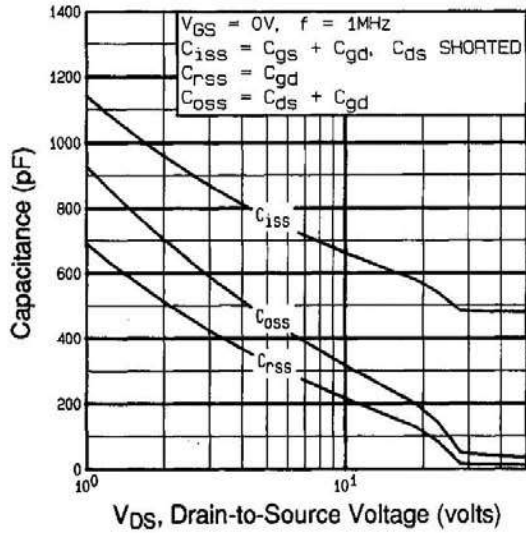
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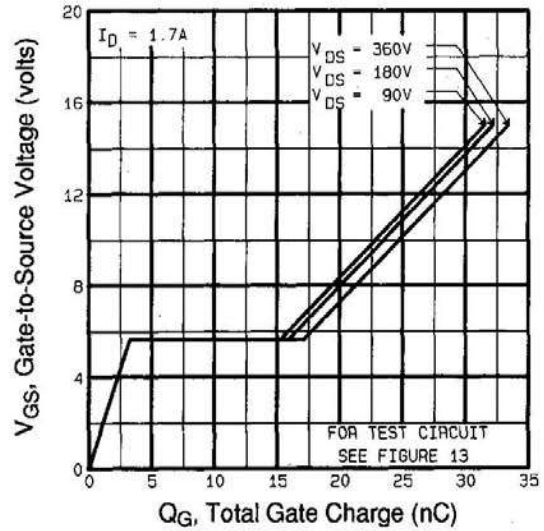


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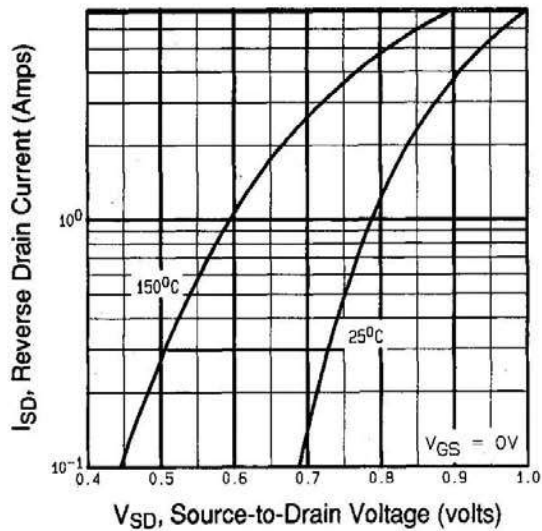
International  
IR Rectifier



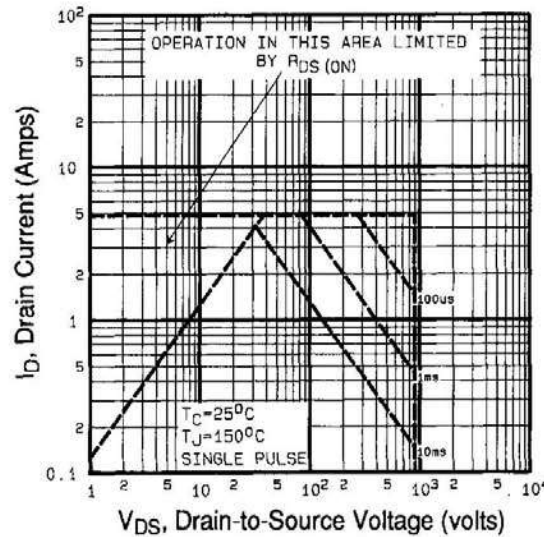
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



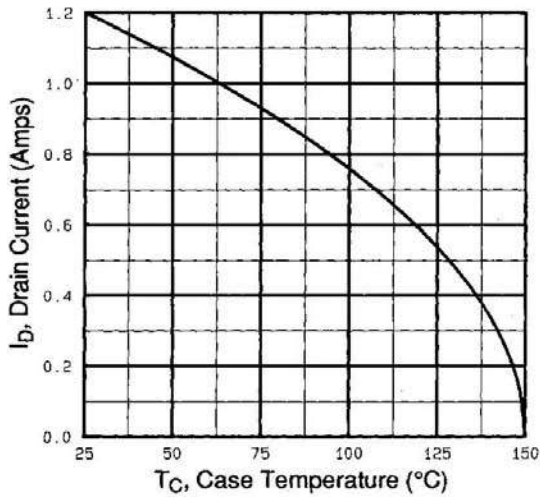
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



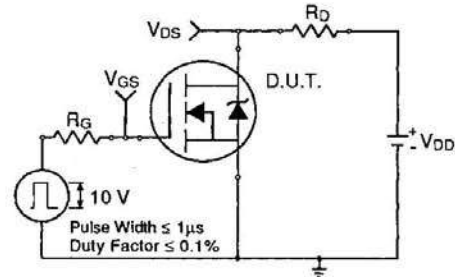
**Fig 7.** Typical Source-Drain Diode Forward Voltage



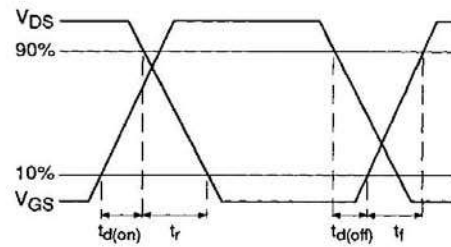
**Fig 8.** Maximum Safe Operating Area



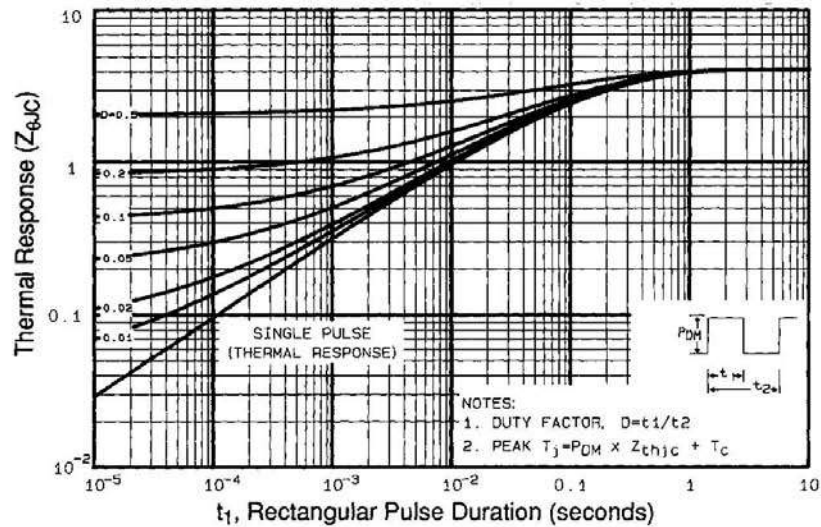
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

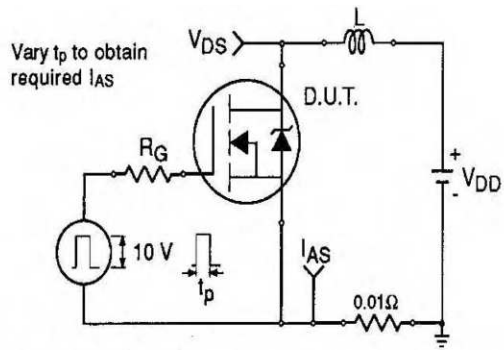


**Fig 10b.** Switching Time Waveforms

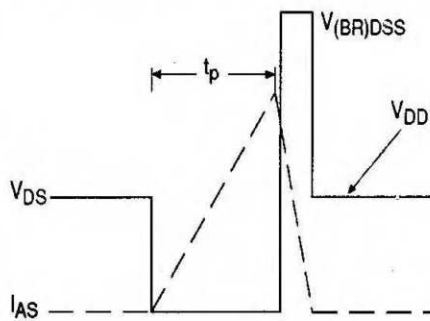


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

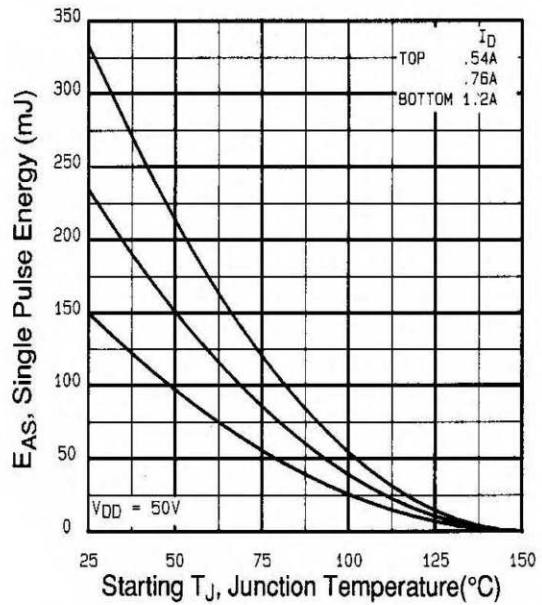
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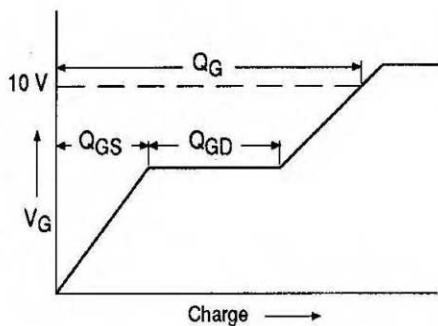
**Fig 12a.** Unclamped Inductive Test Circuit



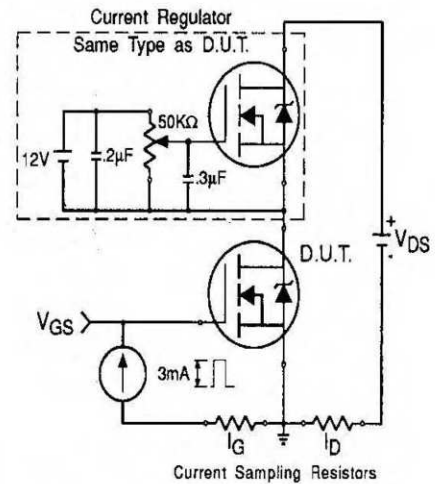
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

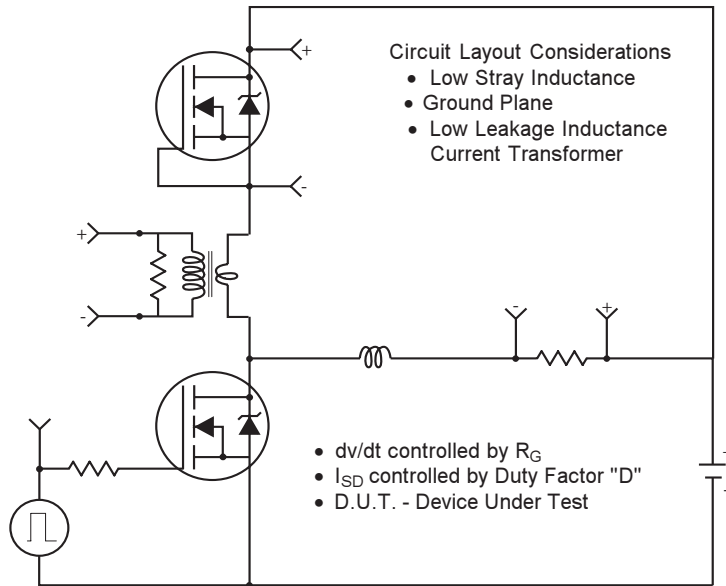


**Fig 13a.** Basic Gate Charge Waveform



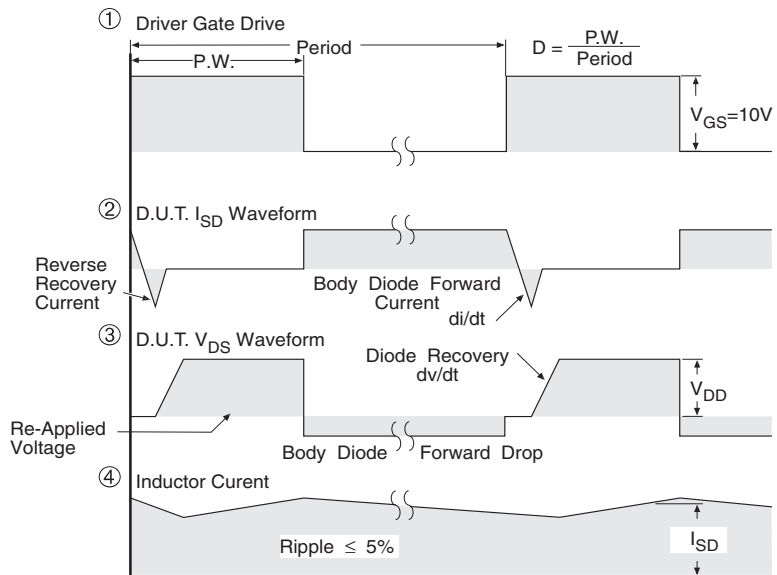
**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

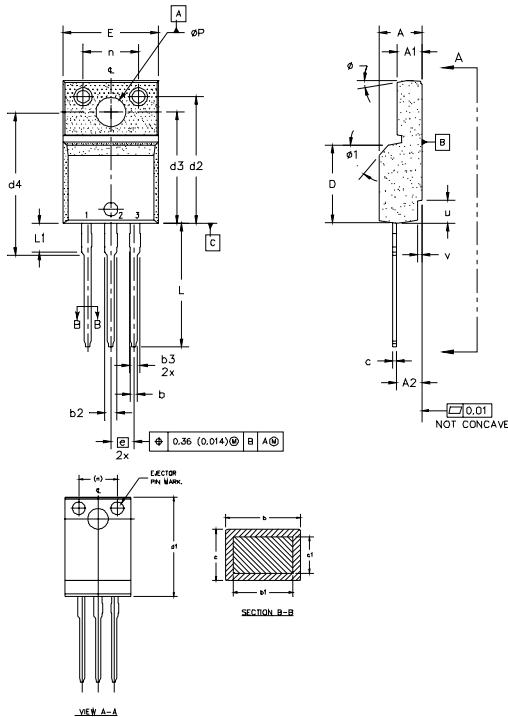
**Fig -14** For N Channel HEXFETS

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## TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



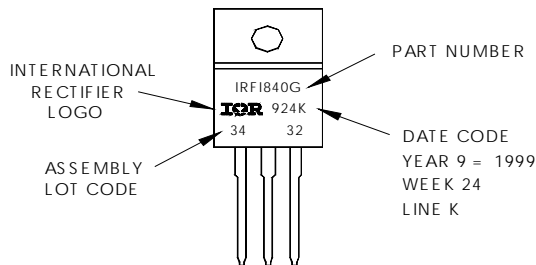
- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
  - 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
  - 6.0 STEP: OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
  - 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.57	4.83	0.180	0.190		
A1	2.57	2.85	0.101	0.114		HEXFET
b	0.622	0.89	0.024	0.035		1.- GATE 2.- DRAIN 3.- SOURCE
b1	0.622	0.838	0.024	0.033	5	
b2	1.229	1.400	0.048	0.055		
b3	1.229	1.400	0.048	0.055		
c	0.440	0.629	0.017	0.025		
c1	0.440	0.584	0.017	0.023		
D	8.65	9.80	0.341	0.386	4	IGBTs, CoPACK
d1	16.80	16.12	0.622	0.635		1.- GATE 2.- COLLECTOR 3.- EMITTER
d2	13.97	14.22	0.550	0.560		
d3	12.30	12.92	0.484	0.509		
d4	8.64	9.91	0.340	0.390		
E	10.36	10.63	0.408	0.419	4	
e	2.54 BSC		0.100 BSC			
L	13.20	13.73	0.520	0.541		
L1	3.10	3.50	0.122	0.138	3	
n	6.08	6.15	0.238	0.242		
phi P	3.05	3.45	0.120	0.136		
u	2.40	2.50	0.094	0.098	6	
v	0.40	0.50	0.016	0.020	6	
phi	3°		3°	7°		
phi 1		45°		45°		

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24 1999  
IN THE ASSEMBLY LINE "K"

**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903  
07/04

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