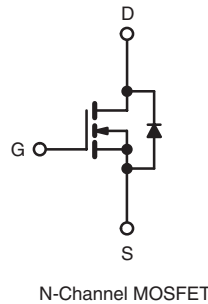


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.24
Q_g (Max.) (nC)	150
Q_{gs} (nC)	45
Q_{gd} (nC)	76
Configuration	Single



FEATURES

- Hard Switching Primary or PFS Switch
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dV/dt Capability
- Lead (Pb)-free Available



BENEFITS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP22N60KPbF
	SiHFP22N60K-E3
SnPb	IRFP22N60K
	SiHFP22N60K


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	I_D	22	A
		$T_C = 100\text{ }^\circ\text{C}$		14	
Pulsed Drain Current ^a			I_{DM}	88	
Linear Derating Factor				2.9	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b			E_{AS}	380	mJ
Repetitive Avalanche Current ^a			I_{AR}	22	A
Repetitive Avalanche Energy ^a			E_{AR}	37	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		P_D	370	W
Peak Diode Recovery dV/dt^c			dV/dt	15	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.5\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 22\text{ A}$ (see fig. 12).
- $I_{SD} \leq 22\text{ A}$, $dI/dt \leq 360\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.34	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	0.30	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	50	μA
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}^b$	-	0.240	0.280	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 13\text{ A}^b$	11	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	3570	-	pF
Output Capacitance	C_{oss}		-	350	-	
Reverse Transfer Capacitance	C_{rss}		-	36	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	4710	-
			$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	92	-
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	180	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}, I_D = 22\text{ A}, V_{DS} = 480\text{ V}$ see fig. 6 and 13 ^b	-	-	150	nC
Gate-Source Charge	Q_{gs}		-	-	45	
Gate-Drain Charge	Q_{gd}		-	-	76	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 22\text{ A}, R_G = 6.2, V_{GS} = 10\text{ V}$, see fig. 10 ^b	-	26	-	ns
Rise Time	t_r		-	99	-	
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	
Fall Time	t_f		-	37	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	22	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	88	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 22\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$	-	590	890	ns
		$T_J = 125\text{ }^\circ\text{C}$	-	670	1010	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$	-	7.2	11	μC
		$T_J = 125\text{ }^\circ\text{C}$	-	8.5	13	
Reverse Recovery Current	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$	-	26	39	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

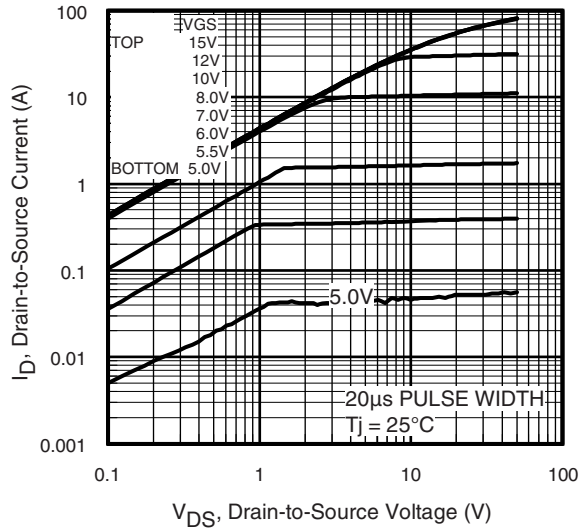


Fig. 1 - Typical Output Characteristics

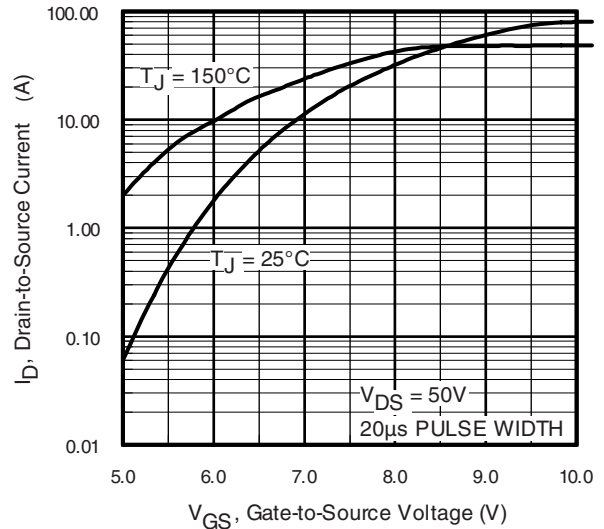


Fig. 3 - Typical Transfer Characteristics

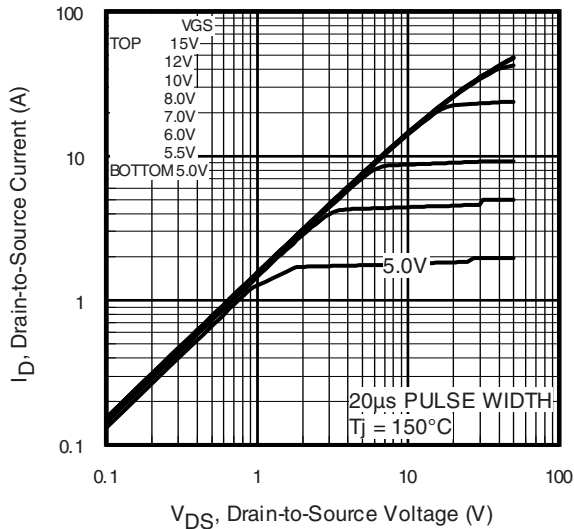


Fig. 2 - Typical Output Characteristics

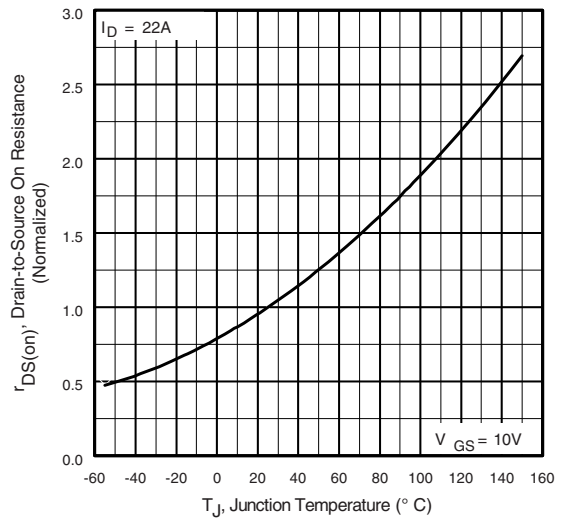


Fig. 4 - Normalized On-Resistance vs. Temperature

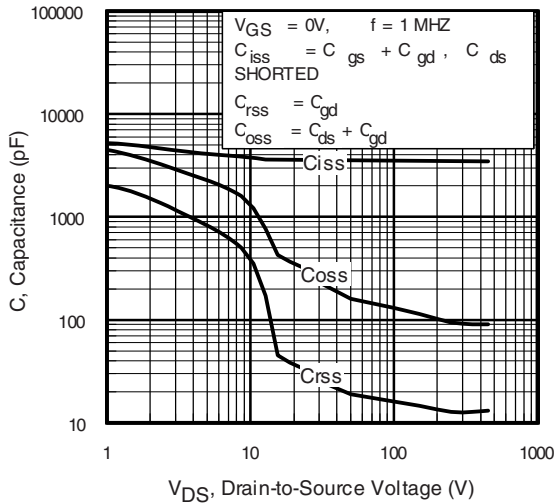


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

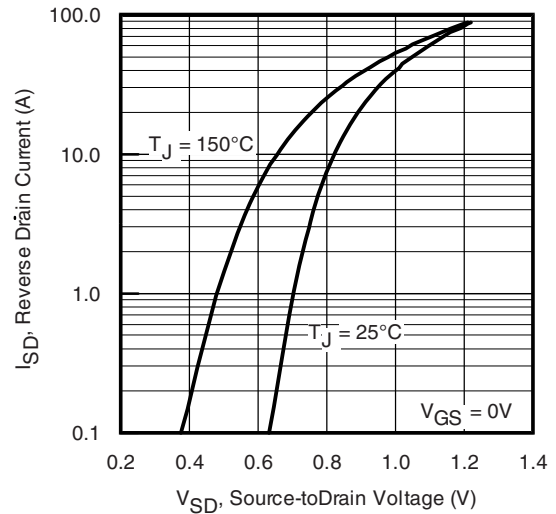


Fig. 7 - Typical Source-Drain Diode Forward Voltage

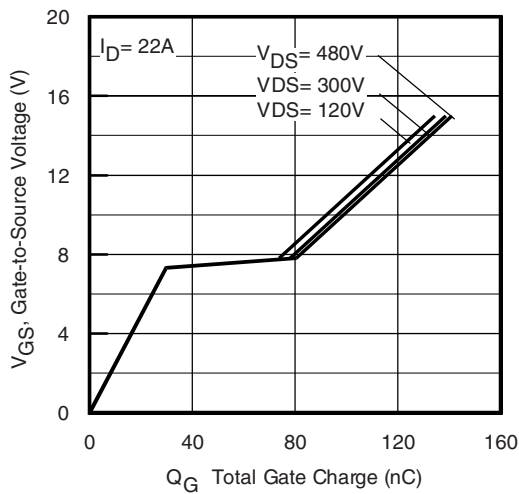


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

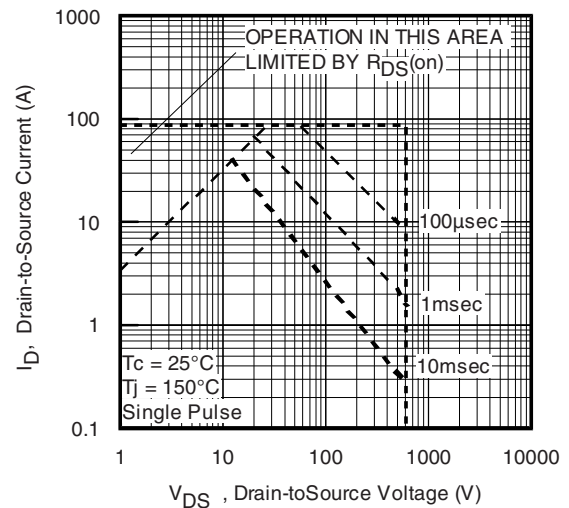


Fig. 8 - Maximum Safe Operating Area

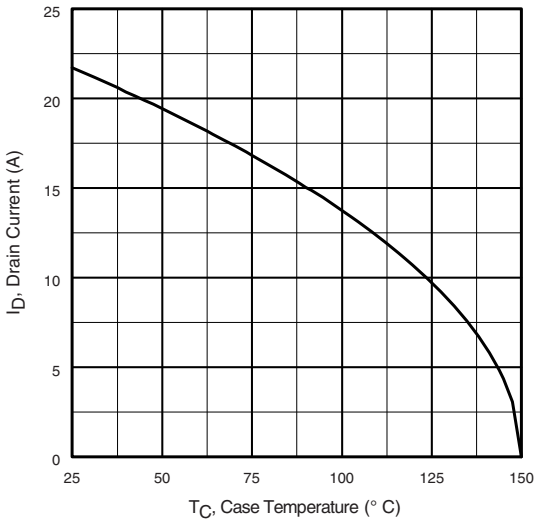


Fig. 9 - Maximum Drain Current vs. Case Temperature

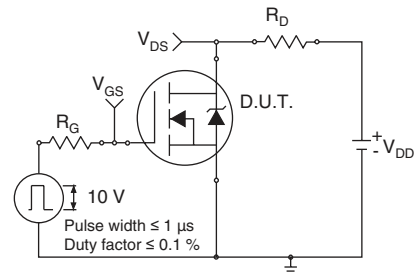


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

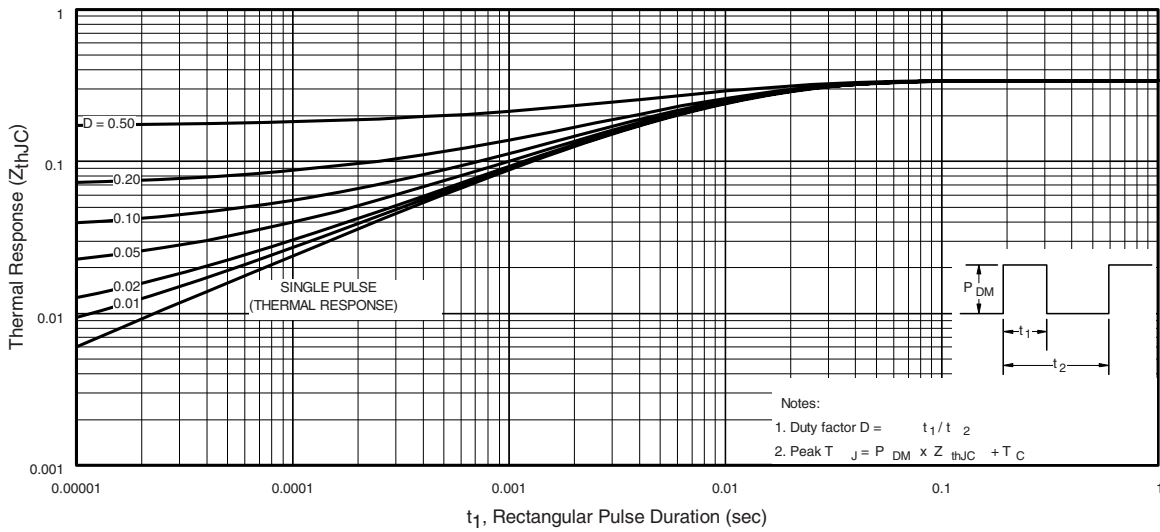


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

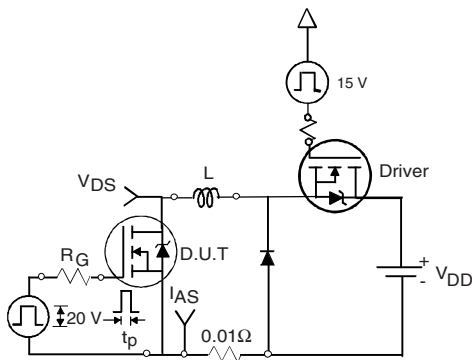


Fig. 12a - Unclamped Inductive Test Circuit

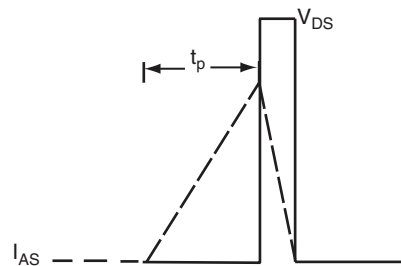


Fig. 12b - Unclamped Inductive Waveforms

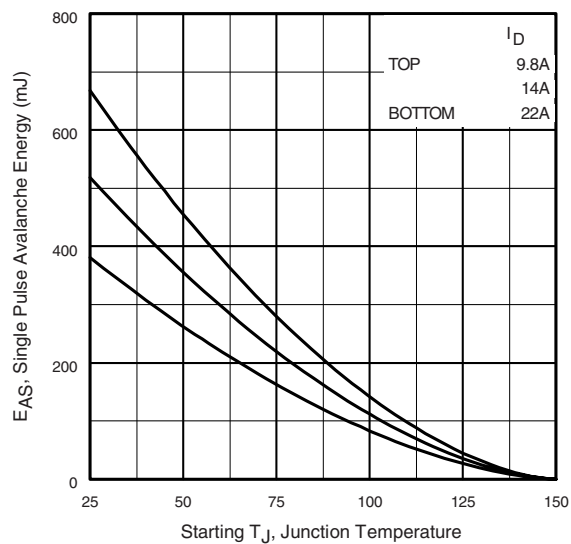


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

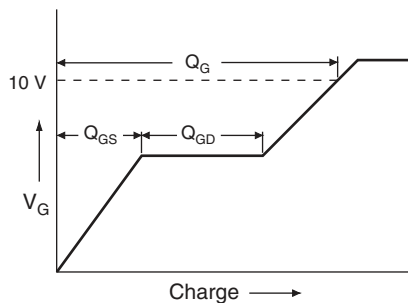


Fig. 13a - Basic Gate Charge Waveform

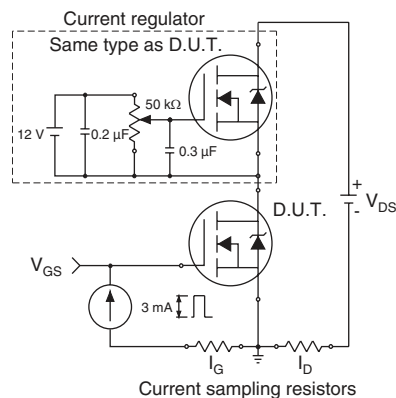
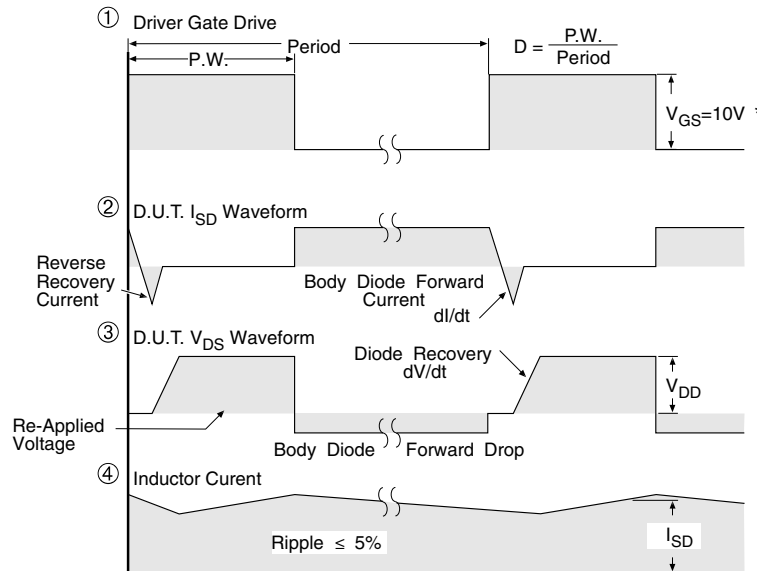
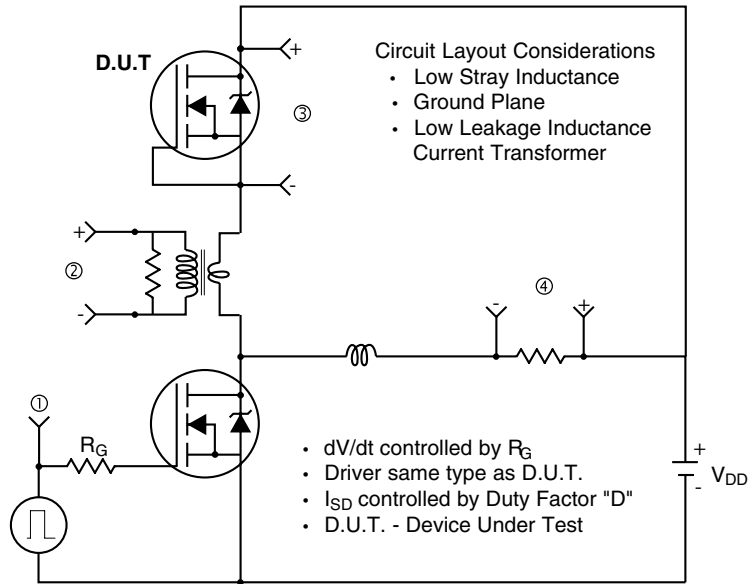


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?91208>.



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.