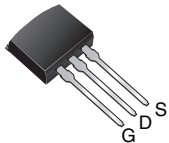


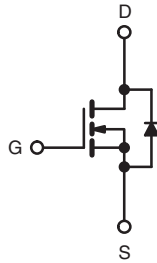
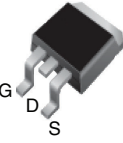
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5$ V	0.20
Q_g (Max.) (nC)	8.4	
Q_{gs} (nC)	3.5	
Q_{gd} (nC)	6.0	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)



N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Advanced Process Technology
- Surface Mount (IRLZ14S, SiHLZ14S)
- Low-Profile Through-Hole (IRLZ14L, SiHLZ14L)
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve externally low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

The through-hole version (IRLZ44L, SiHLZ44L) is available for low-profile applications.

ORDERING INFORMATION				
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-262)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHLZ14S-GE3	SiHLZ14STR-L-GE3 ^a	SiHLZ14STRR-GE3 ^a	-
Lead (Pb)-free	IRLZ14SPbF	-	IRLZ14STRRPbF ^a	-
	SiHLZ14S-E3	-	SiHLZ14STR-E3	-
SnPb	IRLZ14S	-	IRLZ14TRR ^a	IRLZ14L
	SiHLZ14S	-	SiHLZ14STR ^a	SiHLZ14L

Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage ^e	V_{DS}		60	V
Gate-Source Voltage	V_{GS}		± 10	
Continuous Drain Current	V_{GS} at 5 V	$T_C = 25$ °C	10	A
		$T_C = 100$ °C	7.2	
Pulsed Drain Current ^{a, e}	I_{DM}		40	
Linear Derating Factor			0.29	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}		68	mJ
Maximum Power Dissipation	$T_C = 25$ °C		43	W
	$T_A = 25$ °C		3.7	
Peak Diode Recovery dV/dt ^{c, e}	dV/dt		4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	

Notes


- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 790$ μ H, $R_g = 25$ Ω , $I_{AS} = 10$ A (see fig. 12).
 c. $I_{SD} \leq 10$ A, $dI/dt \leq 90$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C.
 d. 1.6 mm from case.
 e. Uses IRLZ14, SiHLZ14 data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.07	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5\text{ V}$	$I_D = 6.0\text{ A}^b$	-	-	0.2	Ω
		$V_{GS} = 4\text{ V}$	$I_D = 5.0\text{ A}^b$	-	-	0.28	
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 6.0\text{ A}$		3.5	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	400	-	μF
Output Capacitance	C_{oss}			-	170	-	
Reverse Transfer Capacitance	C_{rss}			-	42	-	
Total Gate Charge	Q_g	$V_{GS} = 5\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b	-	-	8.4	nC
Gate-Source Charge	Q_{gs}			-	-	3.5	
Gate-Drain Charge	Q_{gd}			-	-	6.0	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 10\text{ A}, R_g = 12\text{ }\Omega, R_D = 2.8\text{ }\Omega$, see fig. 10 ^b		-	9.3	-	ns
Rise Time	t_r			-	110	-	
Turn-Off Delay Time	$t_{d(off)}$			-	17	-	
Fall Time	t_f			-	26	-	
Internal Source Inductance	L_S	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	10	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	40	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 10\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	93	130	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	340	650	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

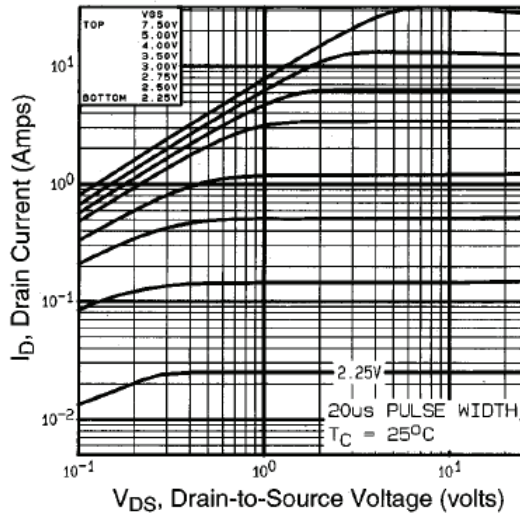


Fig. 1 - Typical Output Characteristics

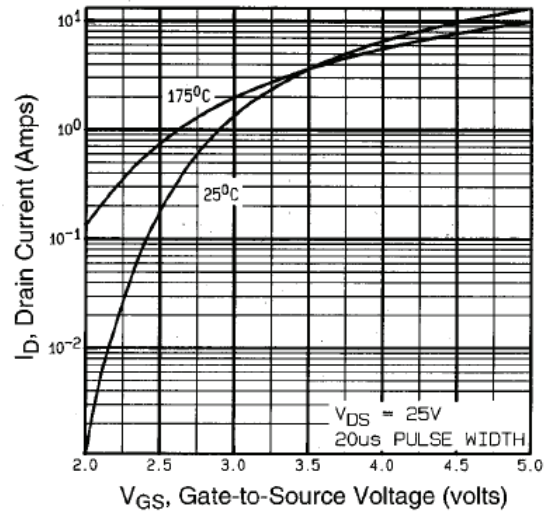


Fig. 3 - Typical Transfer Characteristics

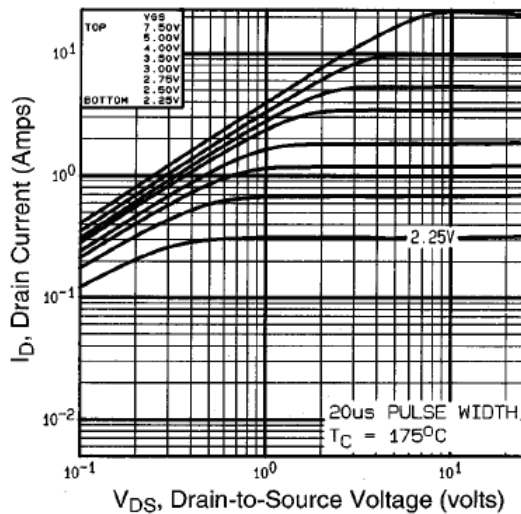


Fig. 2 - Typical Output Characteristics

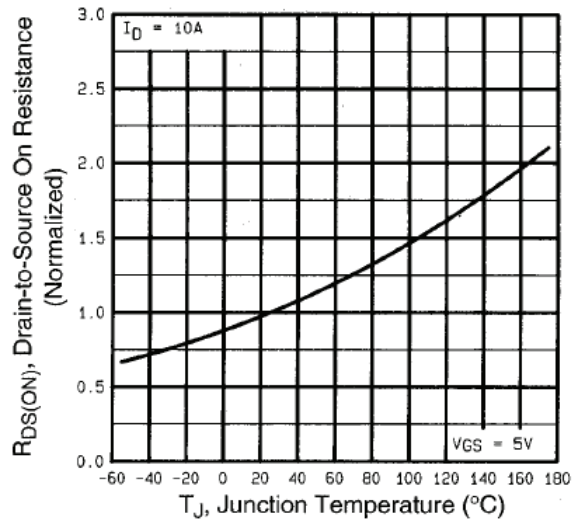


Fig. 4 - Normalized On-Resistance vs. Temperature

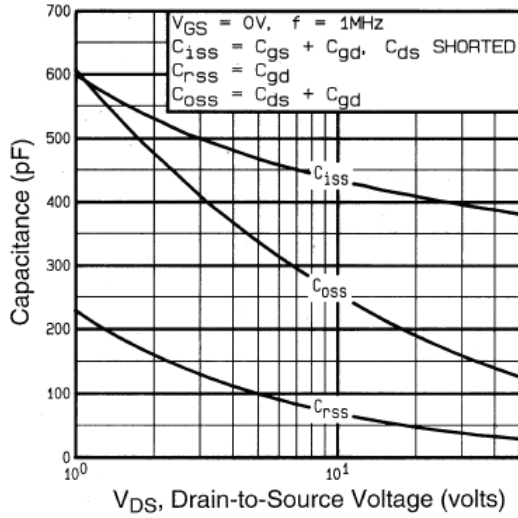


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

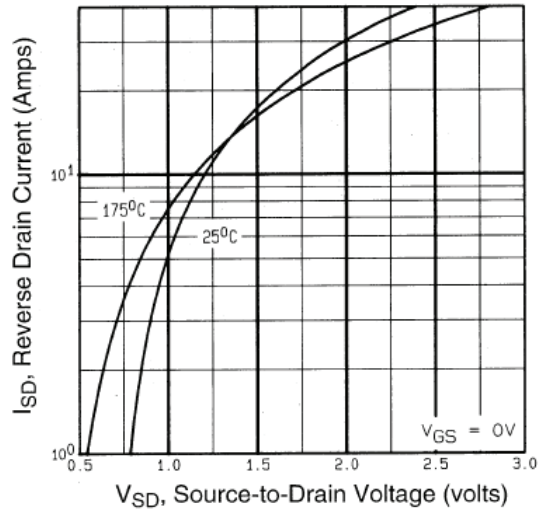


Fig. 7 - Typical Source-Drain Diode Forward Voltage

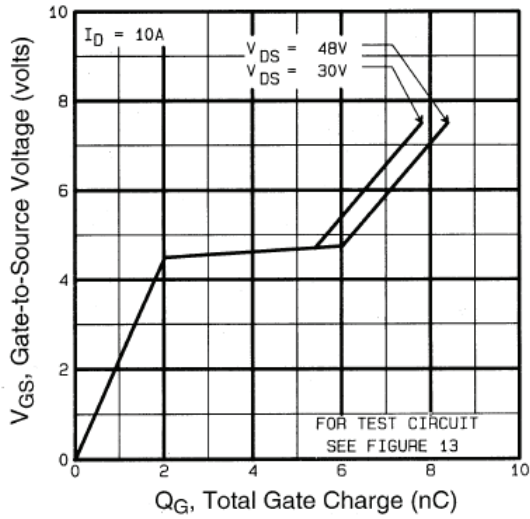


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

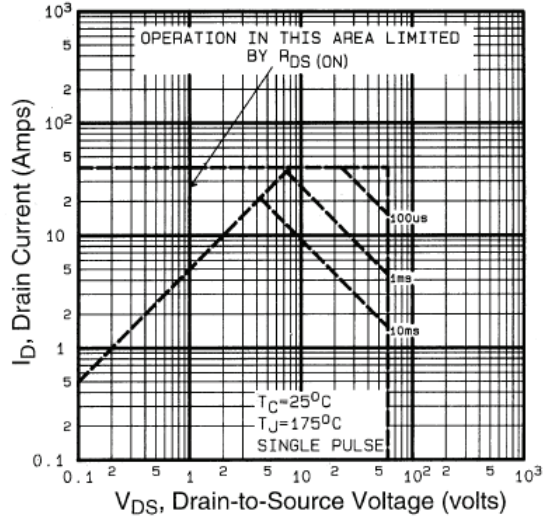


Fig. 8 - Maximum Safe Operating Area

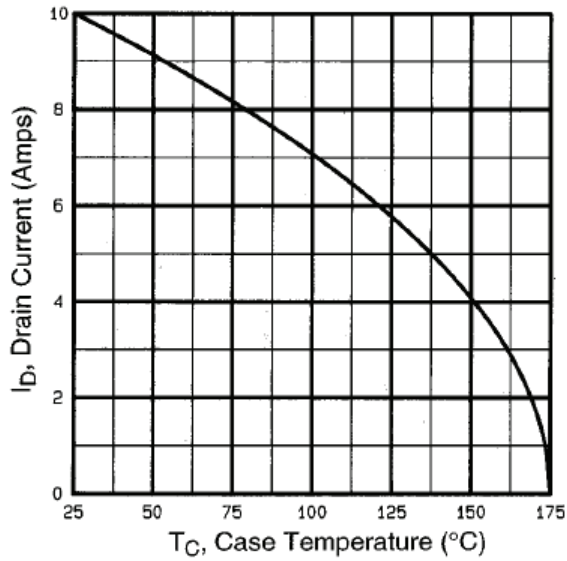


Fig. 9 - Maximum Drain Current vs. Case Temperature

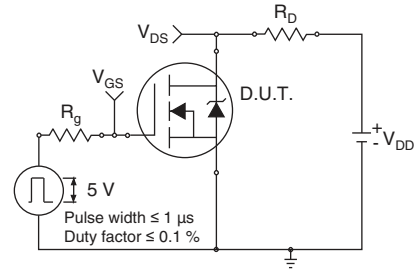


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

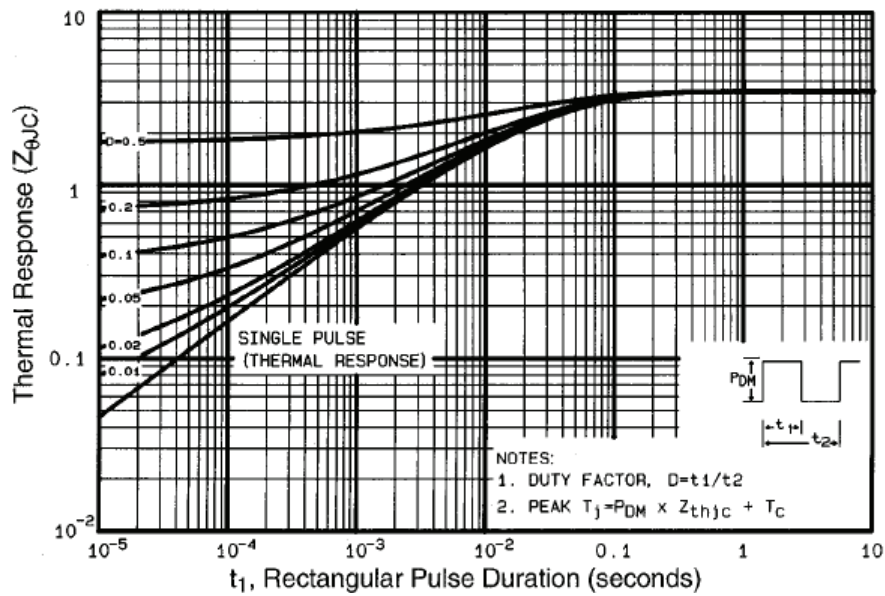


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

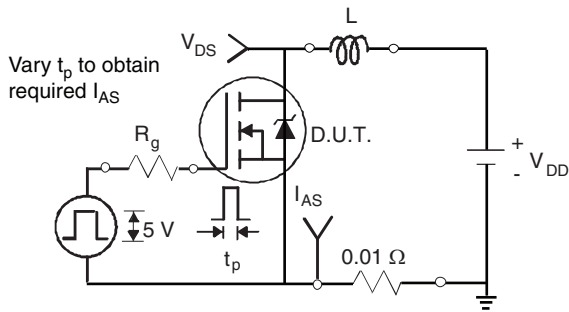


Fig. 12a - Unclamped Inductive Test Circuit

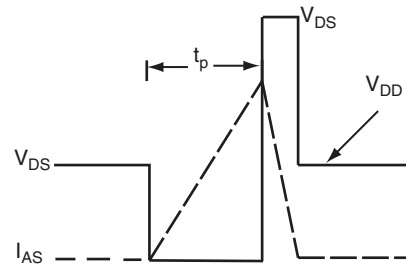


Fig. 12b - Unclamped Inductive Waveforms

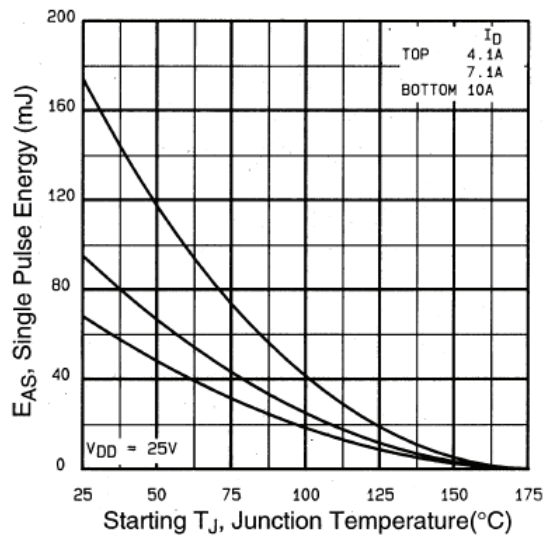


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

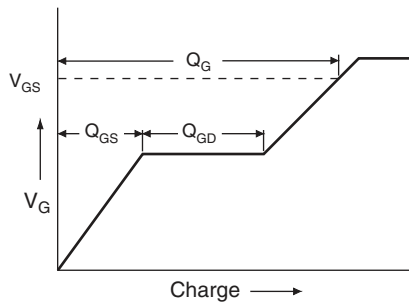


Fig. 13a - Basic Gate Charge Waveform

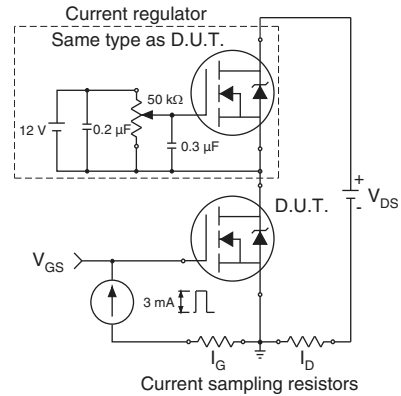
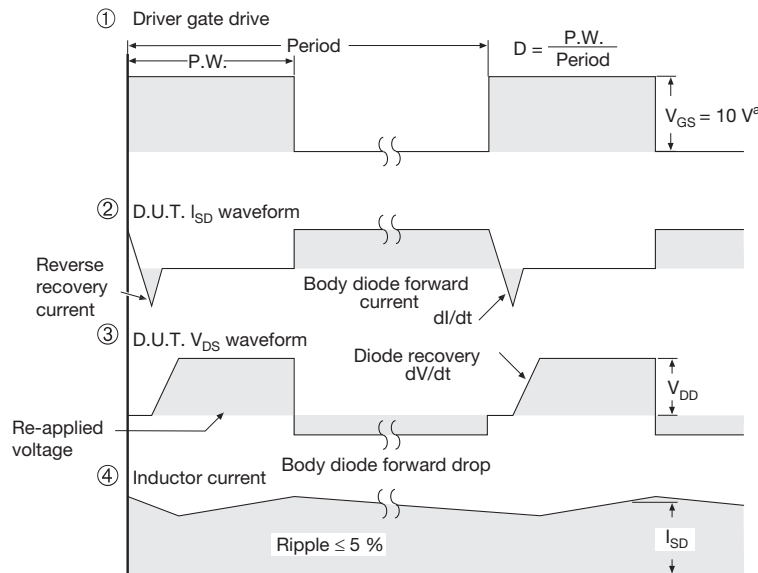


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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