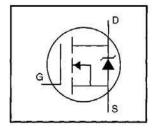
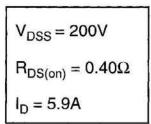
# International Rectifier

# IRFI630GPbF

#### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ®
- Sink to Lead Creepage Dist.= 4.8mm
- Dynamic dv/dt Rating
- Low Thermal Resistance
- Lead-Free

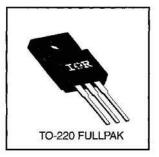




#### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



#### **Absolute Maximum Ratings**

	Parameter	Max.	Units	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	°C Continuous Drain Current, V <sub>GS</sub> @ 10 V 5.9			
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, VGS @ 10 V	3.7	Α	
I <sub>DM</sub>	Pulsed Drain Current ①	24		
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	35	W	
	Linear Derating Factor	0.28	W/°C	
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V	
Eas	Single Pulse Avalanche Energy ②	230	mJ	
IAR	Avalanche Current ①	5.9	A	
EAR	Repetitive Avalanche Energy ①	3.5	mJ	
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns	
TJ TSTG	Operating Junction and Storage Temperature Range	-55 to +150	°C	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)		
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)		

#### **Thermal Resistance**

	Parameter	Min.	Тур.	Max.	Units	
Reuc	Junction-to-Case		_	3.6	°C/W	
ReJA	Junction-to-Ambient		_	65		

11/14/03

Document Number: 91148 www.vishay.com

# IRFI630GPbF

### Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200	-8	_	٧	V <sub>GS</sub> =0V, I <sub>D</sub> = 250μA	
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	-	0.24	_	V/°C	Reference to 25°C, ID= 1mA	
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		_	0.40	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A ④	
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0		4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250μA	
g <sub>fs</sub>	Forward Transconductance	3.2	-	_	S	V <sub>DS</sub> =50V, I <sub>D</sub> =3.5A ④	
	Dunin to Source Lookson Surrent	_	-	25		V <sub>DS</sub> =200V, V <sub>GS</sub> =0V	
IDSS	Drain-to-Source Leakage Current		_	250	μА	V <sub>DS</sub> =160V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C	
lane.	Gate-to-Source Forward Leakage		_	100	nA	V <sub>GS</sub> =20V	
lgss	Gate-to-Source Reverse Leakage	_	-	-100	IIA	V <sub>GS</sub> =-20V	
$Q_g$	Total Gate Charge	_	_	43		I <sub>D</sub> =5.9A	
Q <sub>gs</sub>	Gate-to-Source Charge	-	_	7.0	nC	V <sub>DS</sub> =160V	
Qgd	Gate-to-Drain ("Miller") Charge		_	23		V <sub>GS</sub> =10V See Fig. 6 and 13 @	
t <sub>d(on)</sub>	Turn-On Delay Time	_	9.4			V <sub>DD</sub> =100V	
tr	Rise Time		28	_	ns	I <sub>D</sub> =5.9A	
t <sub>d(off)</sub>	Turn-Off Delay Time	-	39		110	R <sub>G</sub> =12Ω	
tf	Fall Time		20	_		R <sub>D</sub> =16Ω See Figure 10 ®	
Lo	Internal Drain Inductance	-	4.5	_	nН	Between lead, 6 mm (0.25in.)	
Ls	Internal Source Inductance	-	7.5	_	1111	from package and center of die contact	
Ciss	Input Capacitance		800			V <sub>GS</sub> =0V	
Coss	Output Capacitance		240		pF	V <sub>DS</sub> = 25V	
Crss	Reverse Transfer Capacitance	-	76	-		f=1.0MHz See Figure 5	
C	Drain to Sink Capacitance		12		pF	f=1.0MHz	

#### Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Test Conditions	
Is	Continuous Source Current (Body Diode)	-	_	5.9	A	MOSFET symbol showing the	
Ism	Pulsed Source Current (Body Diode) ①		_	24	^	integral reverse p-n junction diode.	
V <sub>SD</sub>	Diode Forward Voltage	_		2.0	٧	T <sub>J</sub> =25°C, I <sub>S</sub> =5.9A, V <sub>GS</sub> =0V @	
trr	Reverse Recovery Time		170	340	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =5.9A di/dt=100A/μs ④	
Qrr	Reverse Recovery Charge		1.1	2.2	μC		
ton	Forward Turn-On Time	Intrinsi	Intrinsic turn-on time is neglegible (turn-on is dominated by Ls+Lp)				

#### Notes:

- Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ③ IsD≤5.9A, di/dt≤120A/ $\mu$ s, VDD≤V(BR)DSs, TJ≤150°C
- ⑤ t=60s, f=60Hz

- ②  $V_{DD}$ =50V, starting  $T_J$ =25°C, L=9.9mH  $R_G$ =25 $\Omega$ , IAS=5.9A (See Figure 12)
- ④ Pulse width ≤ 300 μs; duty cycle ≤2%.

Document Number: 91148 www.vishay.com

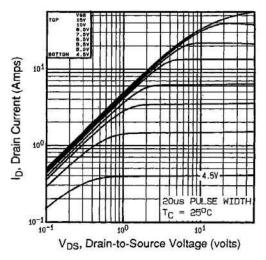


Fig 1. Typical Output Characteristics, T<sub>C</sub>=25°C

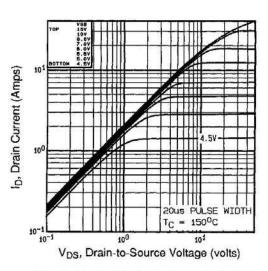


Fig 2. Typical Output Characteristics, T<sub>C</sub>=150°C

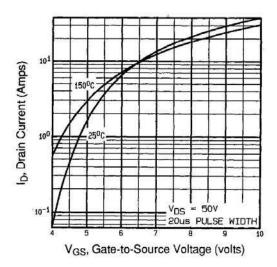


Fig 3. Typical Transfer Characteristics

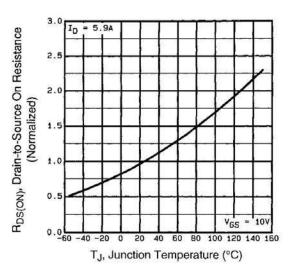


Fig 4. Normalized On-Resistance Vs. Temperature

Document Number: 91148

www.vishay.com

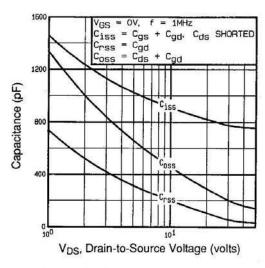


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

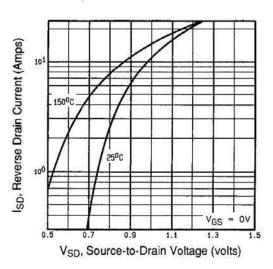


Fig 7. Typical Source-Drain Diode Forward Voltage

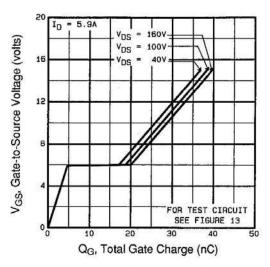


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

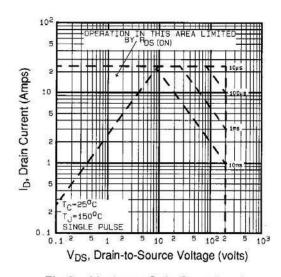


Fig 8. Maximum Safe Operating Area

Document Number: 91148

www.vishay.com

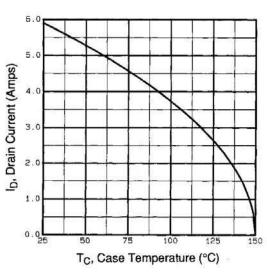


Fig 9. Maximum Drain Current Vs. Case Temperature

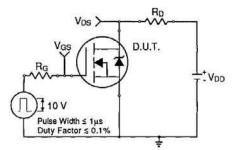


Fig 10a. Switching Time Test Circuit

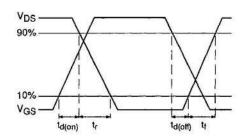


Fig 10b. Switching Time Waveforms

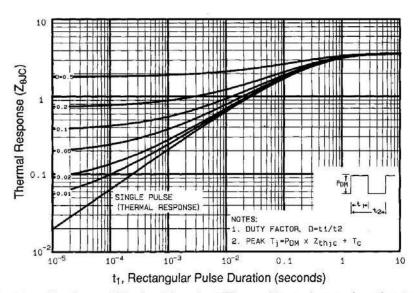


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Document Number: 91148

www.vishay.com

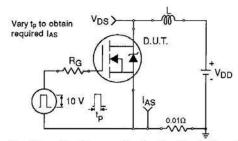


Fig 12a. Unclamped Inductive Test Circuit

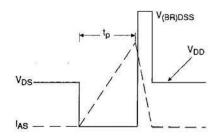


Fig 12b. Unclamped Inductive Waveforms

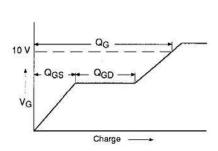


Fig 13a. Basic Gate Charge Waveform

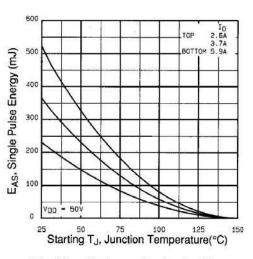


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

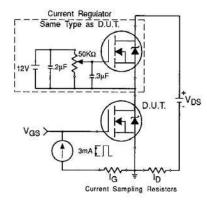


Fig 13b. Gate Charge Test Circuit

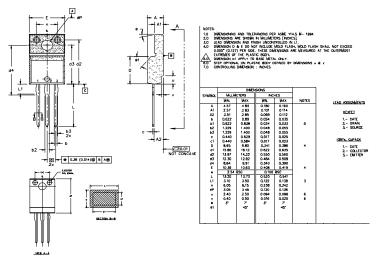
Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit - See page 1505

Appendix B: Package Outline Mechanical Drawing - See page 1510

Document Number: 91148

## TO-220 Full-Pak Package Outline

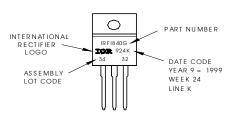
Dimensions are shown in millimeters (inches)



## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

310) 252-7903 11/03

Document Number: 91148 www.vishay.com



Vishay

## **Notice**

The products described herein were acquired by Vishay Intertechnology, Inc., as part of its acquisition of International Rectifier's Power Control Systems (PCS) business, which closed in April 2007. Specifications of the products displayed herein are pending review by Vishay and are subject to the terms and conditions shown below.

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.

International Rectifier<sup>®</sup>, IR<sup>®</sup>, the IR logo, HEXFET<sup>®</sup>, HEXSense<sup>®</sup>, HEXDIP<sup>®</sup>, DOL<sup>®</sup>, INTERO<sup>®</sup>, and POWIRTRAIN<sup>®</sup> are registered trademarks of International Rectifier Corporation in the U.S. and other countries. All other product names noted herein may be trademarks of their respective owners.

Document Number: 99901 www.vishay.com
Revision: 12-Mar-07 1