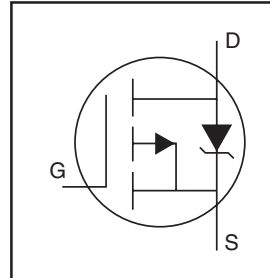


IRFI9610GPbF

HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation=2.5KVRMS ⑤
- Sink to Lead Creepage Dist.=4.8mm
- P-Channel
- Dynamic dv/dt Rating
- Low thermal Resistance
- Lead-Free

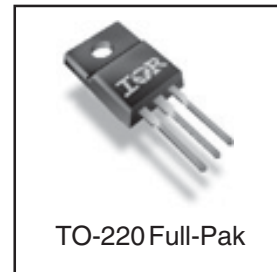


$V_{DSS} = -200V$
$R_{DS(on)} = 3.0\Omega$
$I_D = -2.0A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-2.0	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-1.3	
I_{DM}	Pulsed Drain Current ①	-8.0	
$P_D @ T_C = 25^\circ C$	Power Dissipation	27	W
	Linear Derating Factor	0.22	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	100	mJ
I_{AR}	Avalanche Current③	-2.0	A
E_{AR}	Repetitive Avalanche Energy④	2.7	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	-11	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

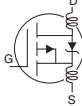
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	4.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient	---	65	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.22	—	V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V _{GS} = -10V, I _D = -1.2A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	0.7	—	—	S	V _{DS} = -50V, I _D = -1.2A
I _{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	V _{DS} = -200V, V _{GS} = 0V
		—	—	-500		V _{DS} = -160V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	13	nC	I _D = -2.0A
Q _{gs}	Gate-to-Source Charge	—	—	3.2		V _{DS} = -160V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	7.3		V _{GS} = -10V, See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	12	—	ns	V _{DD} = -100V
t _r	Rise Time	—	17	—		I _D = -2.0A
t _{d(off)}	Turn-Off Delay Time	—	19	—		R _G = 24Ω
t _f	Fall Time	—	15	—		V _{GS} = -10V, See Fig. 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	180	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	66	—		V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	12	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-8.0		
V _{SD}	Diode Forward Voltage	—	—	-5.8	V	T _J = 25°C, I _S = -2.0A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	130	200	ns	T _J = 25°C, I _F = -2.0A
Q _{rr}	Reverse Recovery Charge	—	700	1050	nC	di/dt = -100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 51mH
R_G = 25Ω, I_{AS} = -2.0A. (See Figure 12)
- ③ I_{SD} ≤ -2.0A, di/dt ≤ -250A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ t = 60s, f = 60Hz.

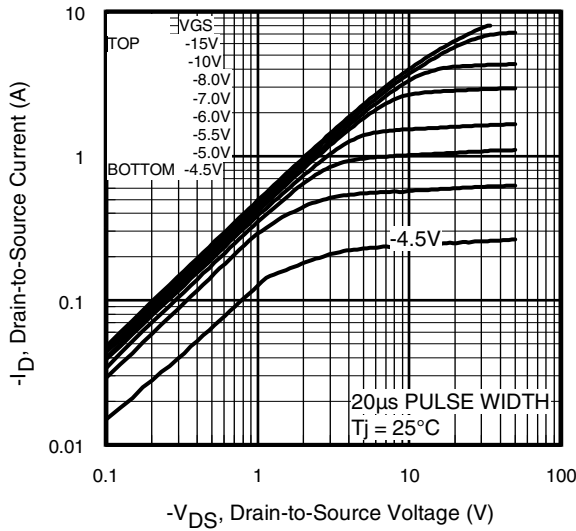


Fig 1. Typical Output Characteristics, $T_J = 25^\circ\text{C}$

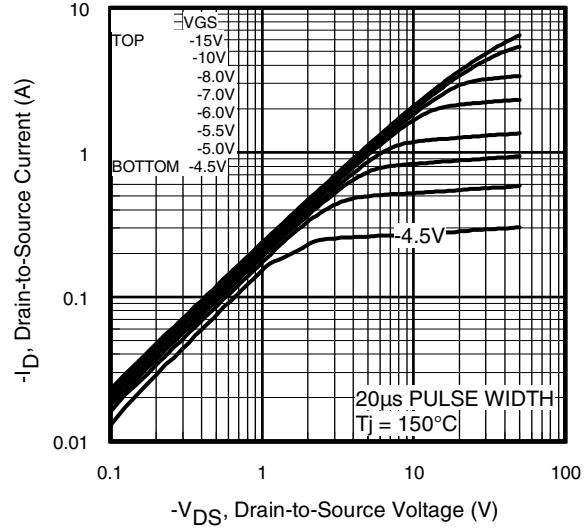


Fig 2. Typical Output Characteristics, $T_J = 150^\circ\text{C}$

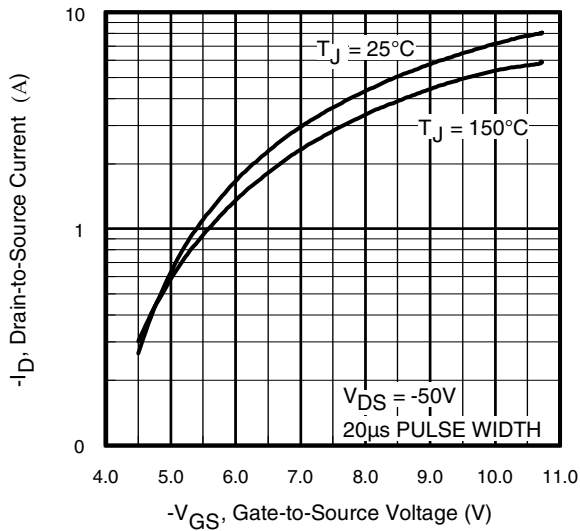


Fig 3. Typical Transfer Characteristics

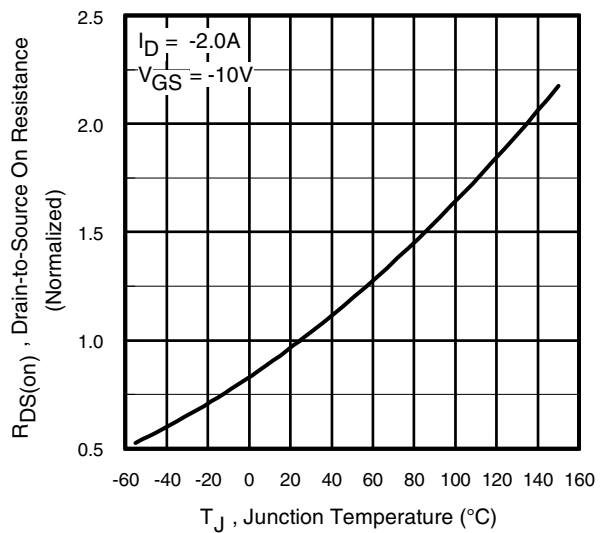


Fig 4. Normalized On-Resistance Vs. Temperature

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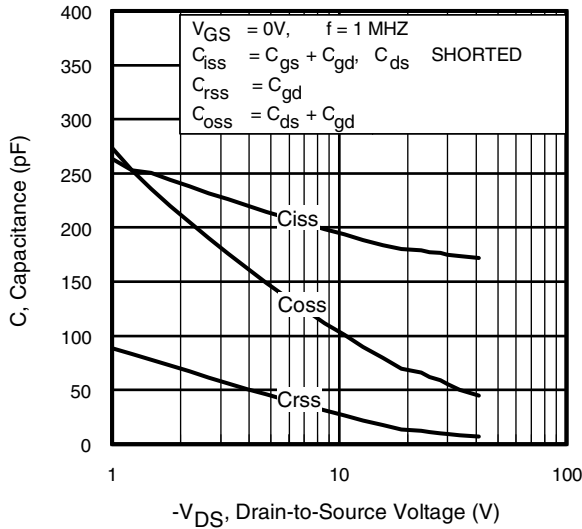


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

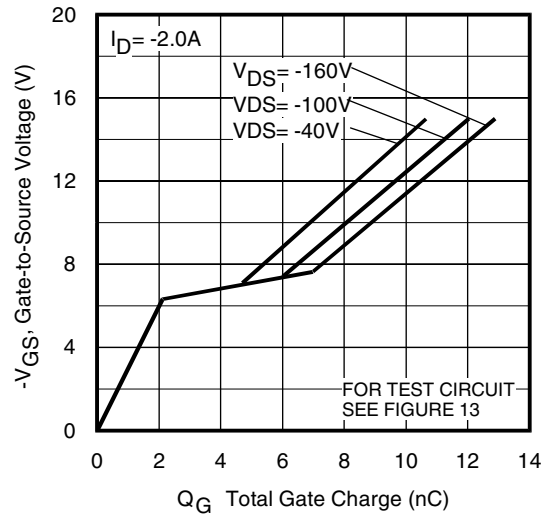


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

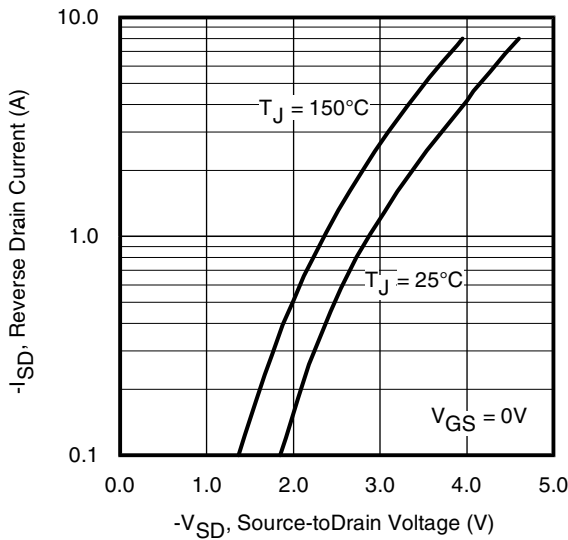


Fig 7. Typical Source-Drain Diode Forward Voltage

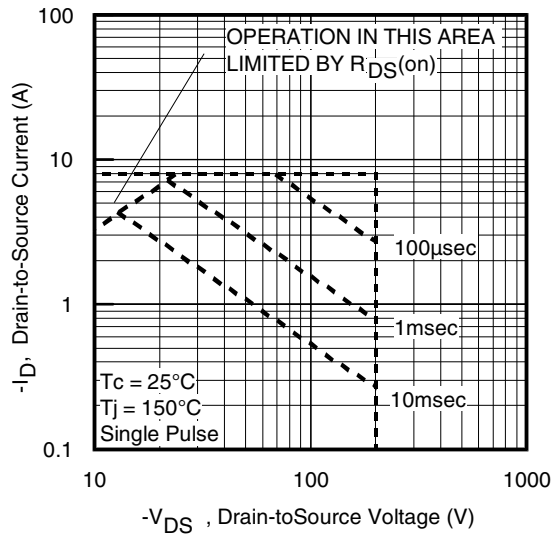


Fig 8. Maximum Safe Operating Area

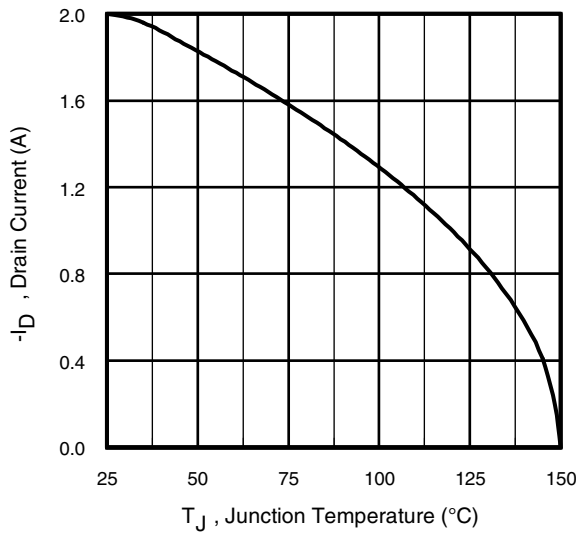


Fig 9. Maximum Drain Current Vs. Case Temperature

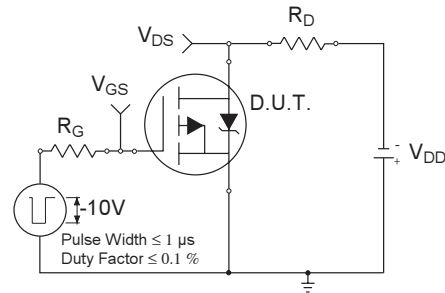


Fig 10a. Switching Time Test Circuit

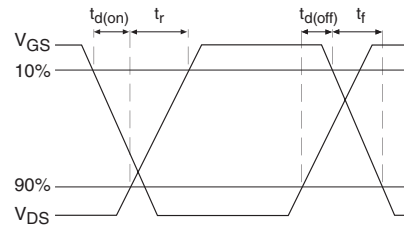


Fig 10b. Switching Time Waveforms

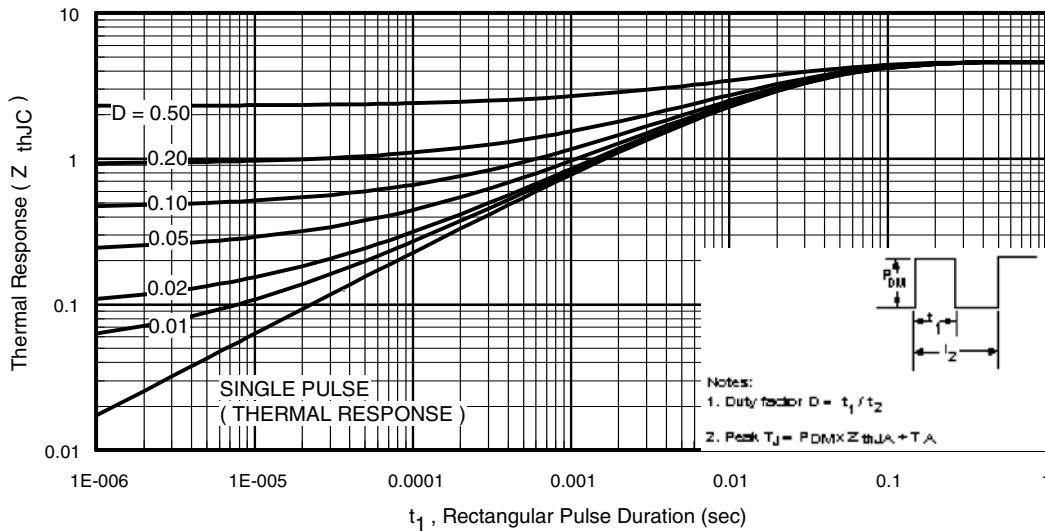


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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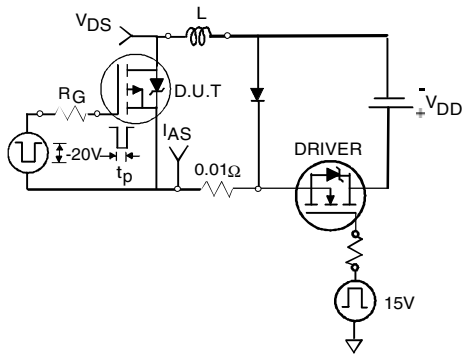


Fig 12a. Unclamped Inductive Test Circuit

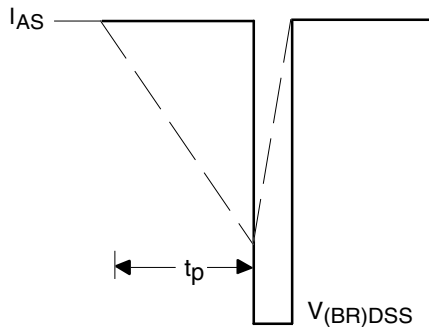


Fig 12b. Unclamped Inductive Waveforms

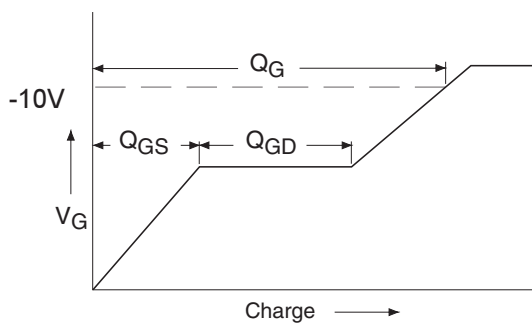


Fig 13a. Basic Gate Charge Waveform

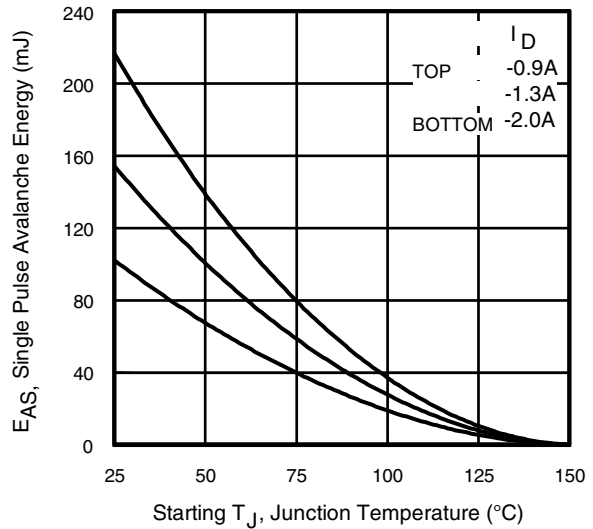


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

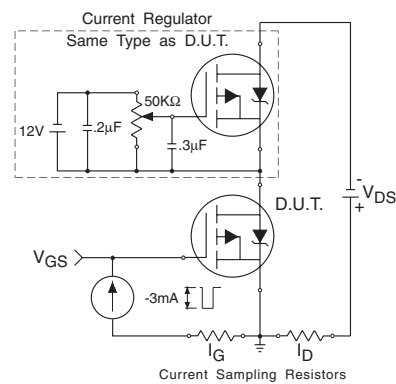
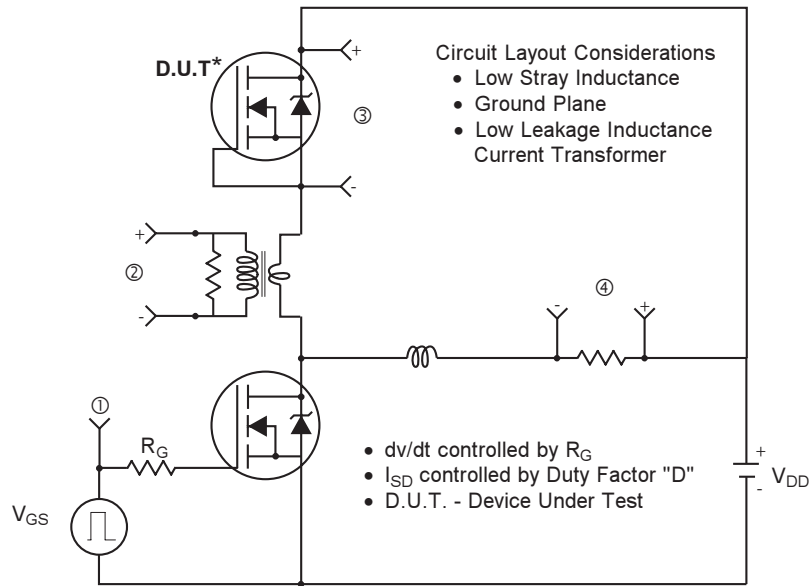
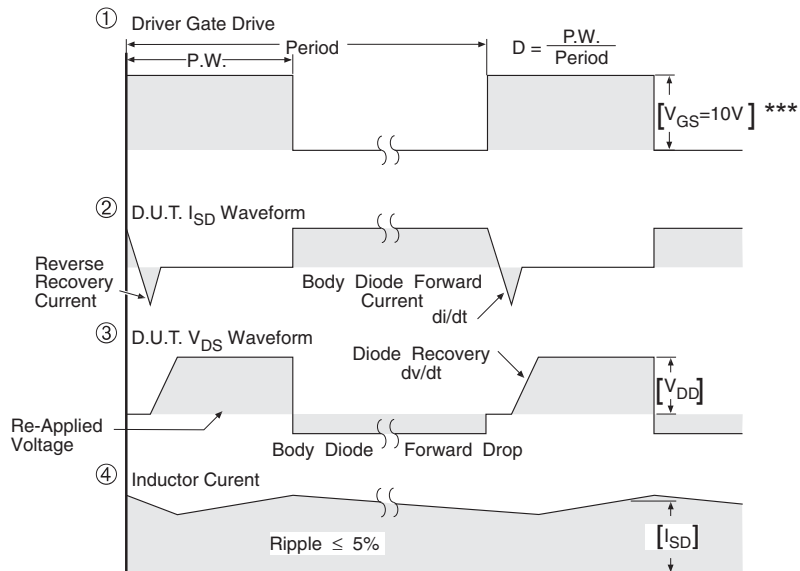


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

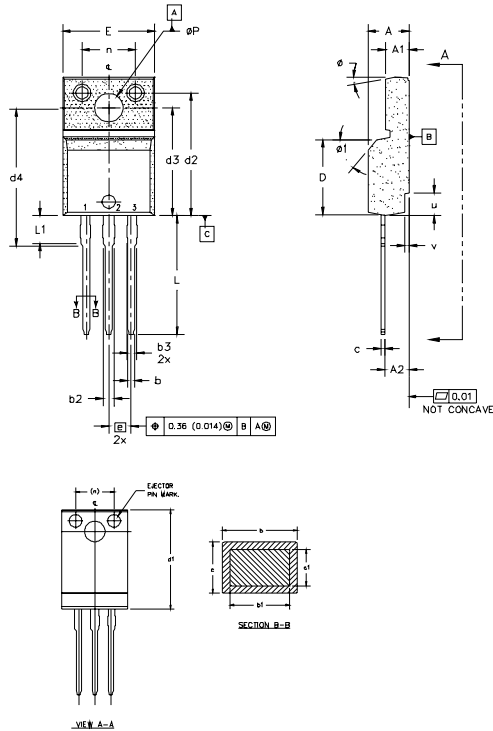
Fig 14. For P-Channel HEXFETS

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TO-220 Full-Pak Package Outline

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Dimensions are shown in millimeters (inches)



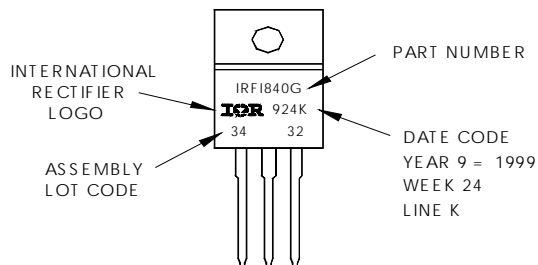
NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M-1994.
2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMITIES OF THE PLASTIC BODY.
5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.
6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	MILLIMETERS		INCHES			
A	4.57	4.83	0.180	0.190		HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE
A1	2.57	2.83	0.101	0.114		
A2	2.51	2.85	0.099	0.112		
b	0.622	0.89	0.024	0.035	5	
b1	0.622	0.838	0.024	0.033		
b2	1.229	1.400	0.048	0.056		
b3	1.229	1.400	0.048	0.056	4	
c	0.440	0.629	0.017	0.025		
c1	0.440	0.584	0.017	0.023		
D	8.65	9.80	0.341	0.386	4	IGBTs, COIPACK 1.- GATE 2.- COLLECTOR 3.- EMITTER
d1	15.80	16.12	0.622	0.636		
d2	13.97	14.22	0.550	0.560		
d3	12.30	12.92	0.484	0.509	4	
d4	8.64	9.91	0.340	0.390		
E	10.36	10.63	0.408	0.419		
e	2.54 BSC		0.100 BSC			
L	13.20	13.73	0.520	0.541	3	
L1	3.10	3.50	0.122	0.138		
n	6.05	6.15	0.238	0.242		
dP	3.05	3.45	0.120	0.136	6	
u	2.40	2.50	0.094	0.098		
v	0.40	0.50	0.016	0.020		
ø	3"	7"	3"	7"	6	
ø1	45°	45°	45°	45°		

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24 1999
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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TAC Fax: (310) 252-7903
07/04

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