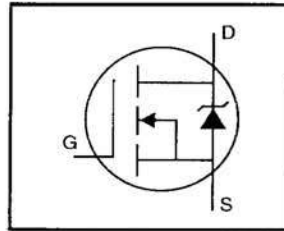


IRL640PbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- RDS(on) Specified at VGS=4V & 5V
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead-Free

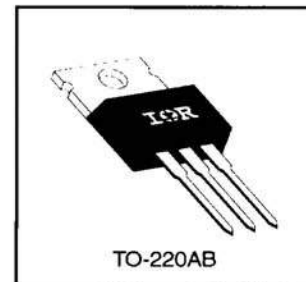


$V_{DSS} = 200V$
 $R_{DS(on)} = 0.18\Omega$
 $I_D = 17A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	17	A
$I_D @ T_C = 100^\circ C$	11	
I_{DM}	68	
$P_D @ T_C = 25^\circ C$	125	W
	1.0	W/°C
V_{GS}	±10	V
E_{AS}	580	mJ
I_{AR}	10	A
E_{AR}	13	mJ
dv/dt	5.0	V/ns
T_J T_{STG}	-55 to +150	°C
	300 (1.6mm from case)	
	10 lbf•in (1.1 N•m)	


Thermal Resistance

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	1.0	°C/W
$R_{\theta CS}$	—	0.50	—	
$R_{\theta JA}$	—	—	62	


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International
IR Rectifier

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.27	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D=1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.18	Ω	$V_{GS}=5.0V, I_D=10A$ ④
		—	—	0.27		$V_{GS}=4.0V, I_D=8.5A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
g_{fs}	Forward Transconductance	16	—	—	S	$V_{DS}=50V, I_D=10A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=200V, V_{GS}=0V$
		—	—	250		$V_{DS}=160V, V_{GS}=0V, T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10V$
Q_g	Total Gate Charge	—	—	66	nC	$I_D=17A$
Q_{gs}	Gate-to-Source Charge	—	—	9.0		$V_{DS}=160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	38		$V_{GS}=5.0V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	$V_{DD}=100V$
t_r	Rise Time	—	83	—		$I_D=17A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G=4.6\Omega$
t_f	Fall Time	—	52	—		$R_D=5.7\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1800	—	pF	$V_{GS}=0V$
C_{oss}	Output Capacitance	—	400	—		$V_{DS}=25V$
C_{rss}	Reverse Transfer Capacitance	—	120	—		$f=1.0MHz$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	68		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}, I_S=17A, V_{GS}=0V$ ④
t_{rr}	Reverse Recovery Time	—	310	470	ns	$T_J=25^\circ\text{C}, I_F=17A$
Q_{rr}	Reverse Recovery Charge	—	3.2	4.8	μC	$di/dt=100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DD}=50V$, starting $T_J=25^\circ\text{C}$, $L=3.0mH$, $R_G=25\Omega$, $I_{AS}=17A$ (See Figure 12)
- ③ $I_{SD}\leq 17A$, $di/dt\leq 150A/\mu s$, $V_{DD}\leq V_{(BR)DSS}$, $T_J\leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

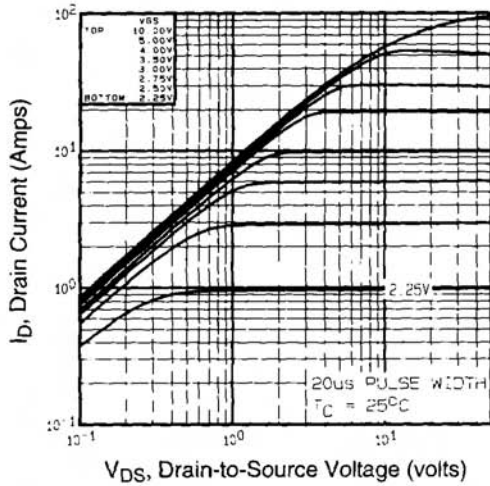


Fig 1. Typical Output Characteristics,
 $T_C=25^\circ\text{C}$

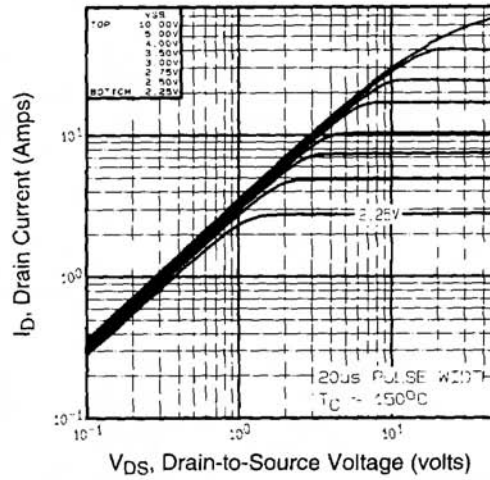


Fig 2. Typical Output Characteristics,
 $T_C=150^\circ\text{C}$

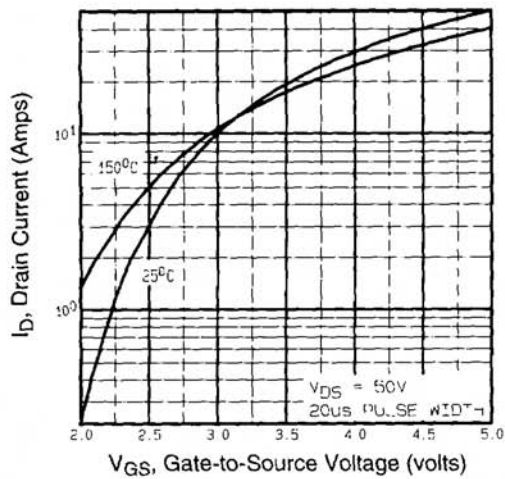


Fig 3. Typical Transfer Characteristics

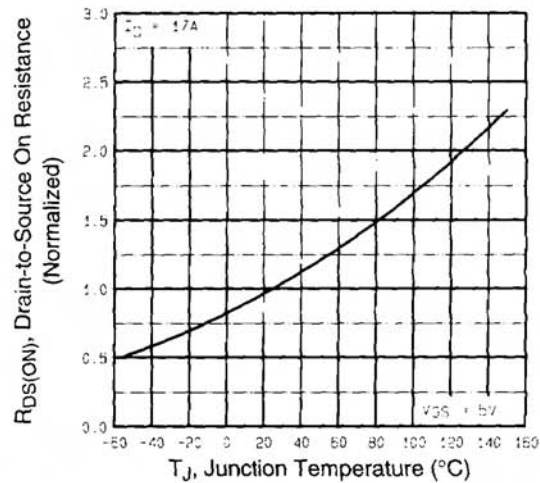


Fig 4. Normalized On-Resistance
 Vs. Temperature

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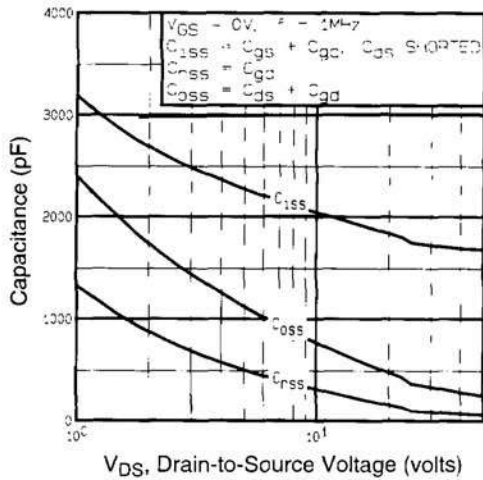


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

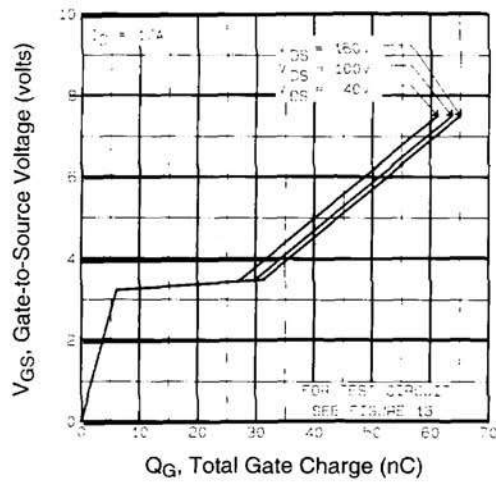


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

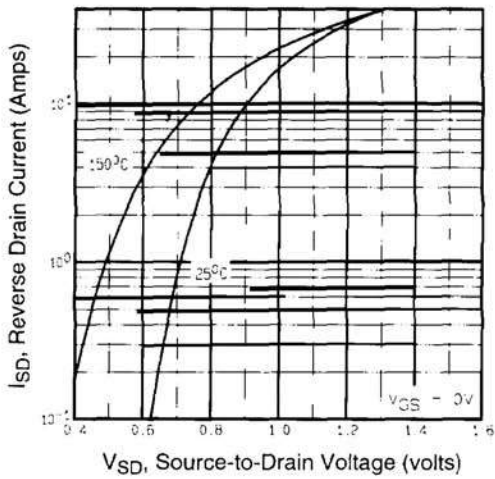


Fig 7. Typical Source-Drain Diode Forward Voltage

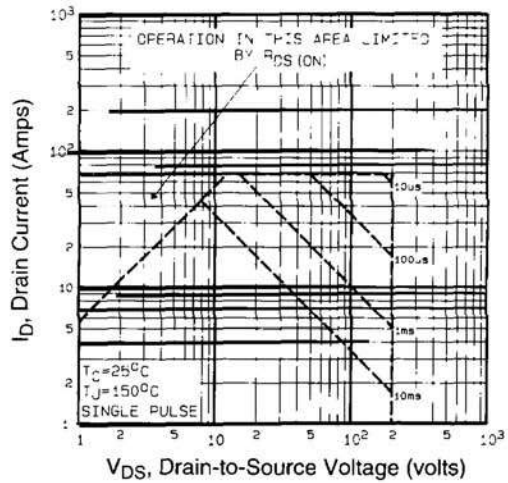


Fig 8. Maximum Safe Operating Area

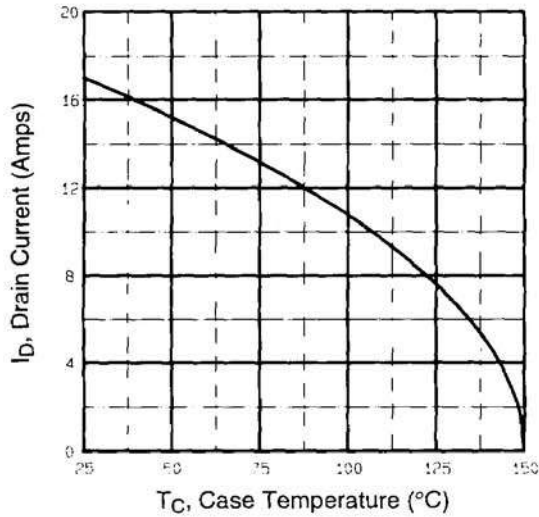


Fig 9. Maximum Drain Current Vs. Case Temperature

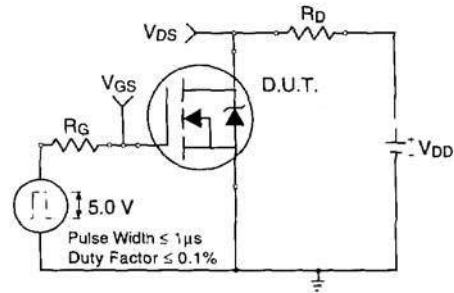


Fig 10a. Switching Time Test Circuit

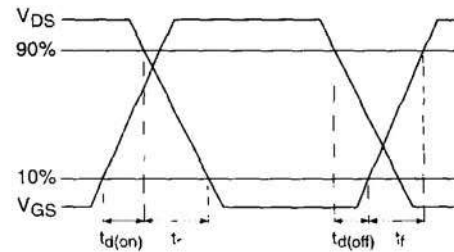


Fig 10b. Switching Time Waveforms

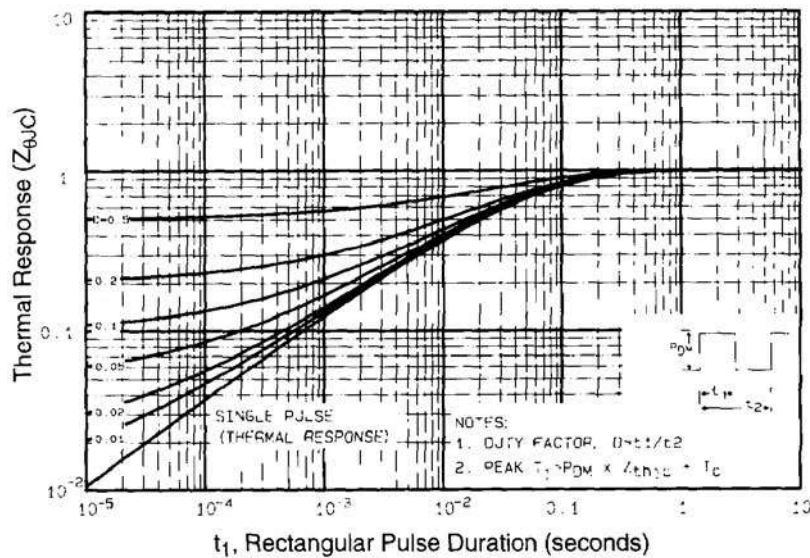


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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IR Rectifier

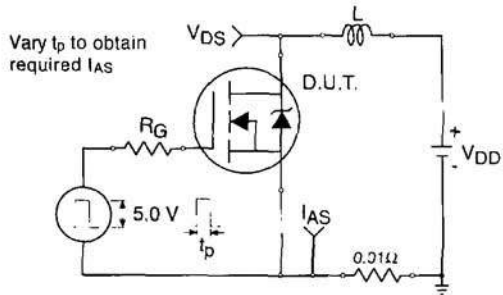


Fig 12a. Unclamped Inductive Test Circuit

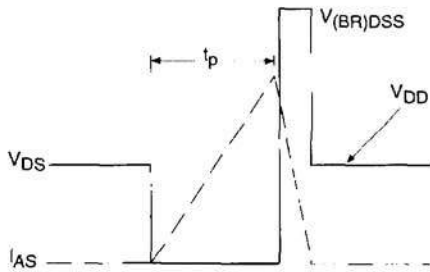


Fig 12b. Unclamped Inductive Waveforms

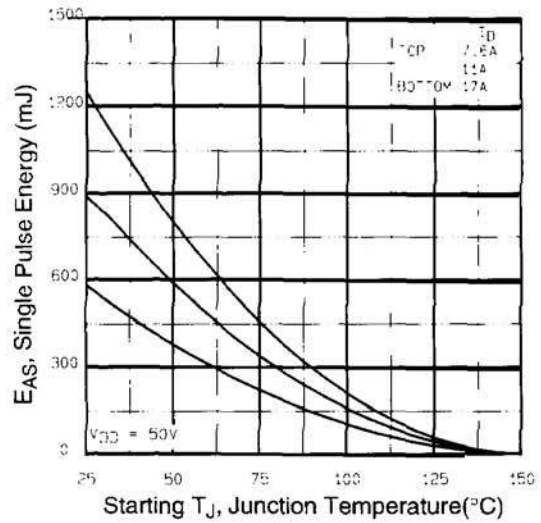


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

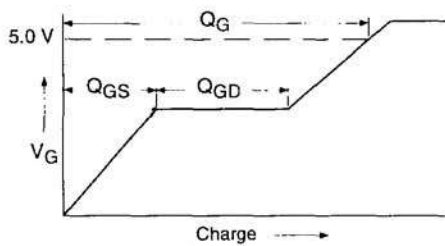


Fig 13a. Basic Gate Charge Waveform

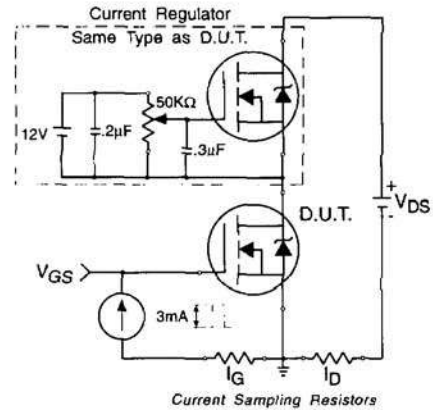


Fig 13b. Gate Charge Test Circuit

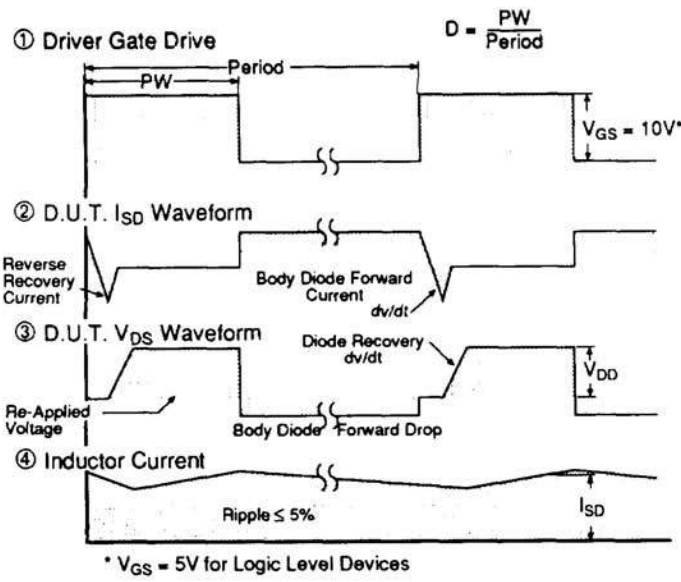
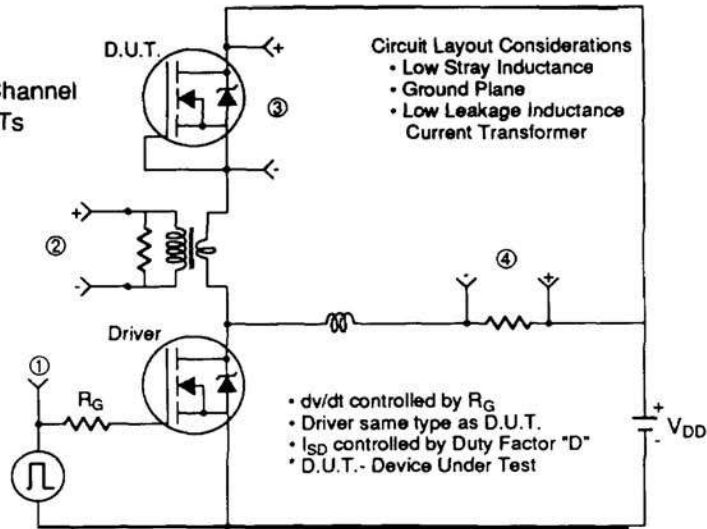
Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

Appendix B: Package Outline Mechanical Drawing

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs

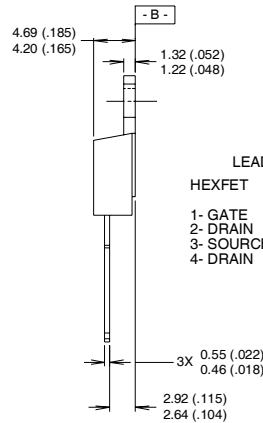
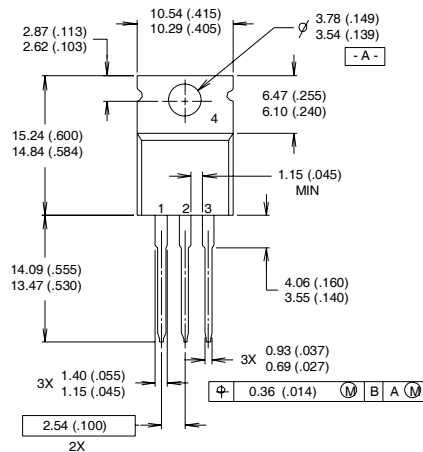


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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



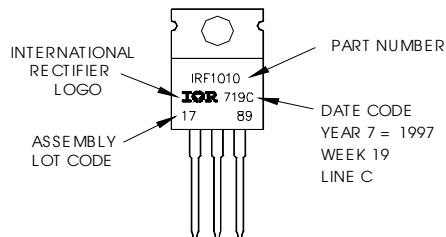
LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH
 - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
 - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 TAC Fax: (310) 252-7903
 01/04

Document Number: 91305

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