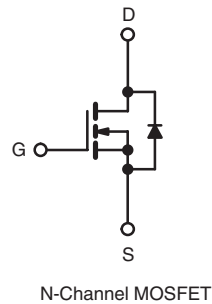
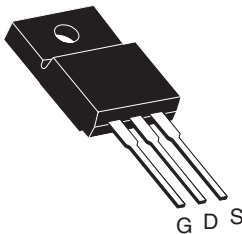


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	400	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.55
$Q_g$ (Max.) (nC)	39	
$Q_{gs}$ (nC)	10	
$Q_{gd}$ (nC)	19	
Configuration	Single	

**TO-220 FULLPAK**

**FEATURES**

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V  $V_{GS}$  Rating
- Isolated Package
- High Voltage Isolation = 2.5 kV<sub>RMS</sub> (t = 60 s, f = 60 Hz)
- Sink to Lead Creepage Distance = 4.8 mm
- Repetitive Avalanche Rated
- Lead (Pb)-free Available


 Available  
**RoHS\***  
 COMPLIANT

**DESCRIPTION**

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Power MOSFETs technology, the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability that are characteristic of Power MOSFETs offer the designer a new standard in power transistors for switching applications. The TO-220 Fullpak eliminates the need for additional insulating hardware. The moulding compound used provides a high isolation capability and low thermal resistance between the tab and external heatsink.

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI740GLCPbF
	SiHFI740GLC-E3
SnPb	IRFI740GLC
	SiHFI740GLC

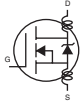
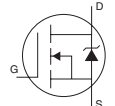
ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	400	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	5.7	A
		$T_C = 100$ °C	3.6	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	23		
Linear Derating Factor		0.32	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	310	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	5.7	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	4.0	mJ	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	40	W
Peak Diode Recovery dV/dt <sup>c</sup>	$dV/dt$	4.0	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C, L = 16 mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 5.7$  A (see fig. 12).
- $I_{SD} \leq 10$  A,  $dI/dt \leq 120$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.1	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		400	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.76	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 3.4\text{ A}^b$	-	-	0.55	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 6.0\text{ A}^b$		3.0	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	1100	-	pF
Output Capacitance	$C_{oss}$			-	190	-	
Reverse Transfer Capacitance	$C_{rss}$			-	18	-	
Drain to Sink Capacitance	$C$	$f = 1.0\text{ MHz}$		-	12	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}, V_{DS} = 320\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	39	nC
Gate-Source Charge	$Q_{gs}$			-	-	10	
Gate-Drain Charge	$Q_{gd}$			-	-	19	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200\text{ V}, I_D = 10\text{ A}, R_G = 9.1\text{ }\Omega, R_D = 20\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	11	-	ns
Rise Time	$t_r$			-	31	-	
Turn-Off Delay Time	$t_{d(off)}$			-	25	-	
Fall Time	$t_f$			-	20	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	5.7	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	23	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	380	570	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	2.8	4.2	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

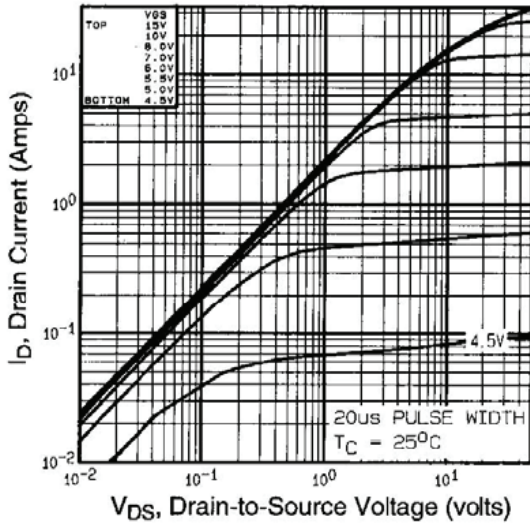


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

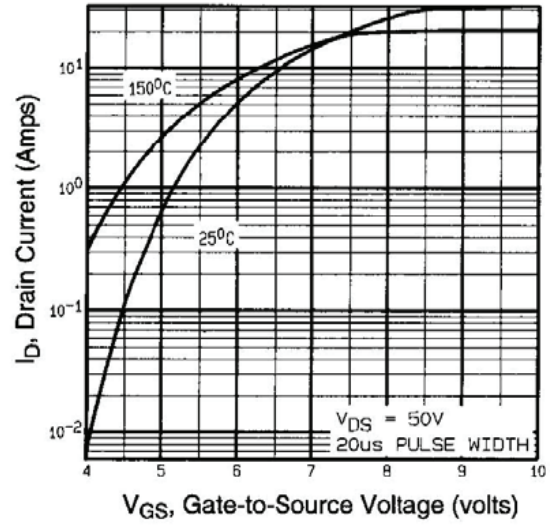


Fig. 3 - Typical Transfer Characteristics

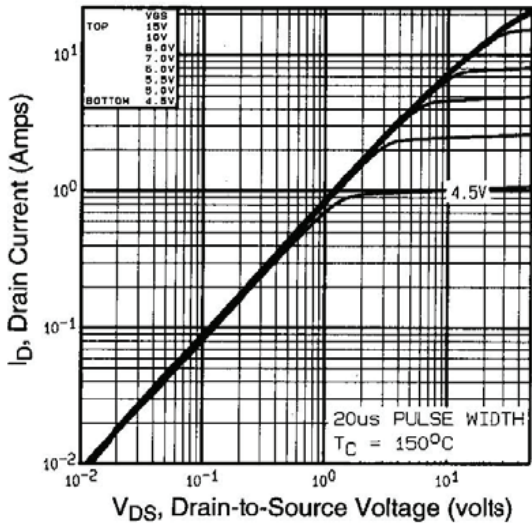


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

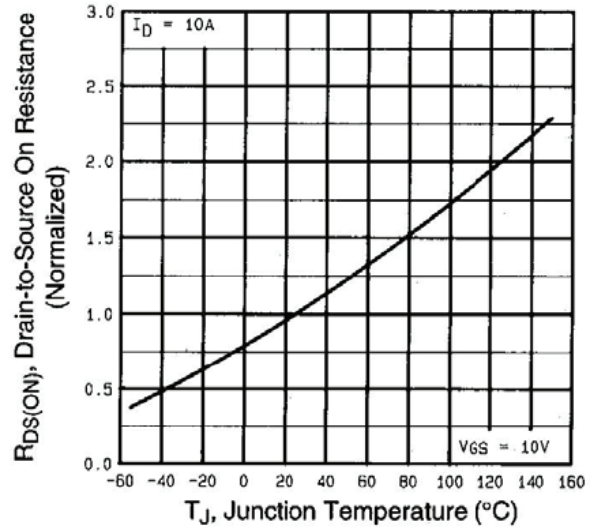


Fig. 4 - Normalized On-Resistance vs. Temperature

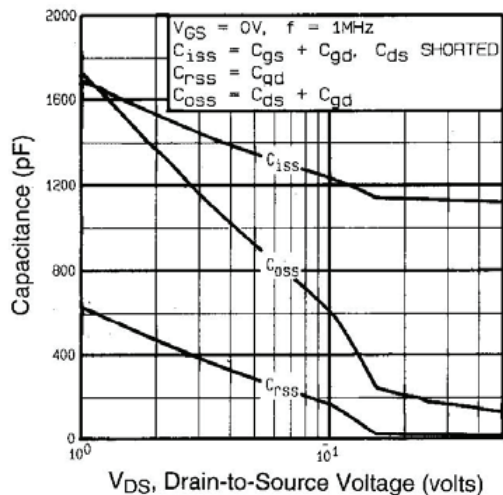


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

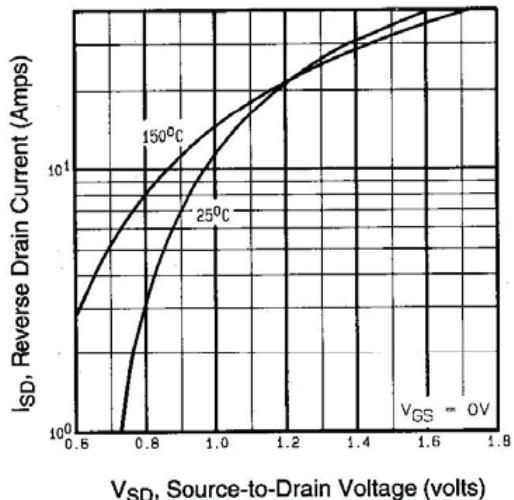


Fig. 7 - Typical Source-Drain Diode Forward Voltage

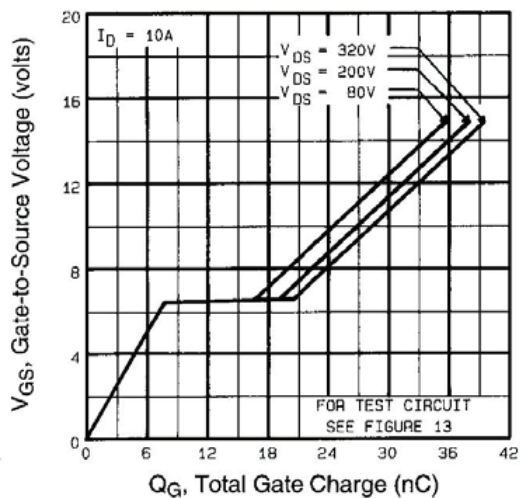


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

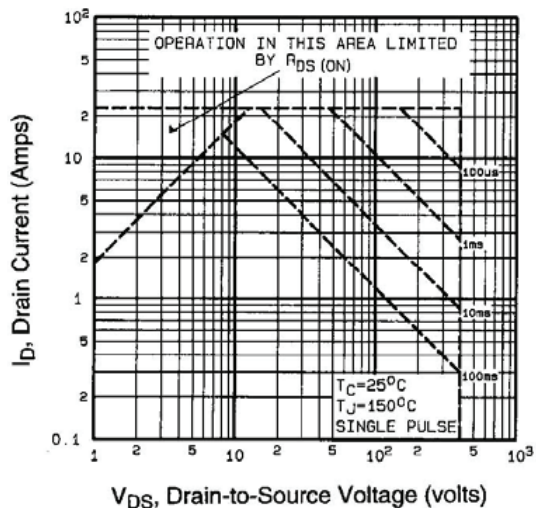


Fig. 8 - Maximum Safe Operating Area

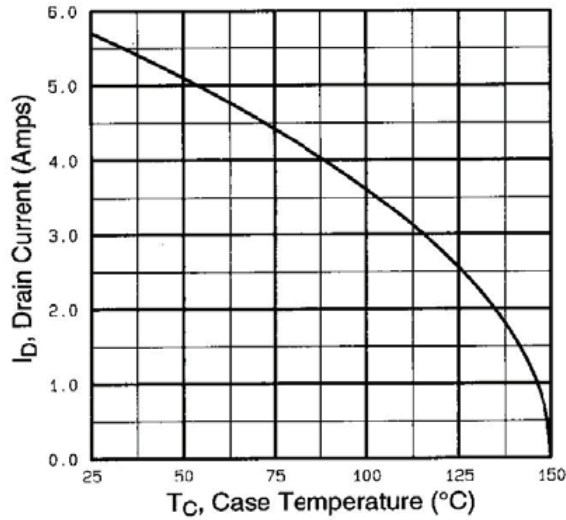


Fig. 9 - Maximum Drain Current vs. Case Temperature

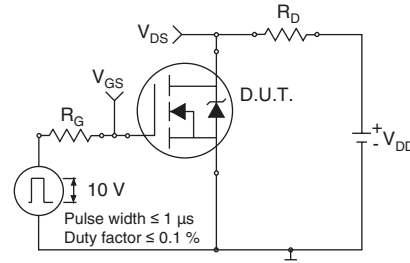


Fig. 10a - Switching Time Test Circuit

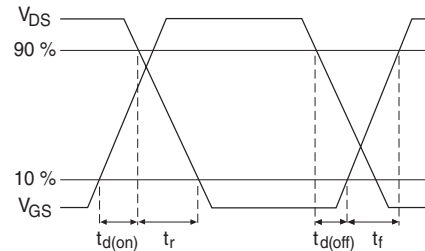


Fig. 10b - Switching Time Waveforms

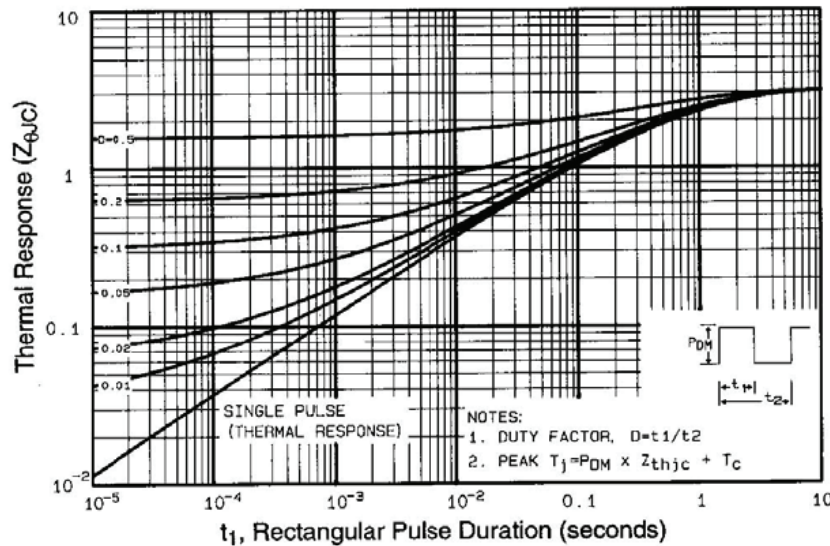


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

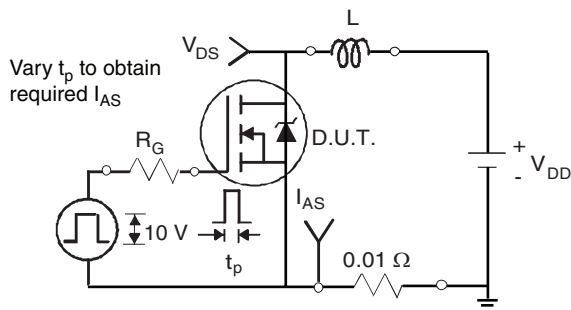


Fig. 12a - Unclamped Inductive Test Circuit

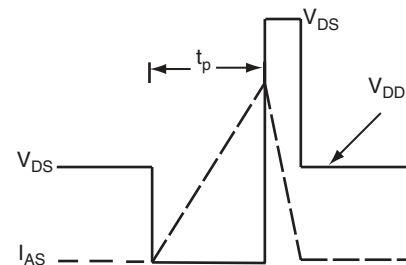


Fig. 12b - Unclamped Inductive Waveforms

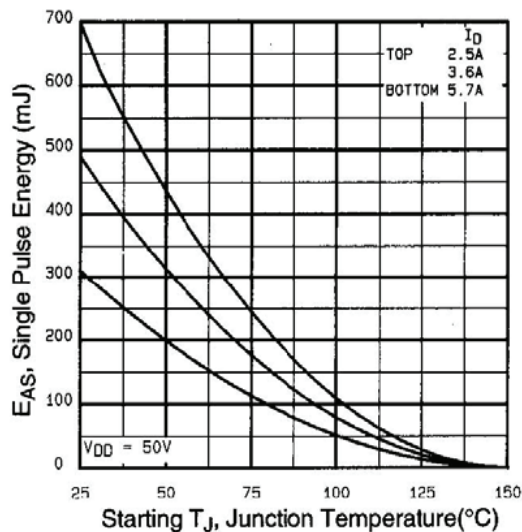


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

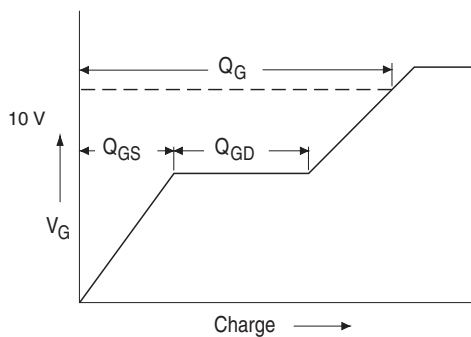


Fig. 13a - Basic Gate Charge Waveform

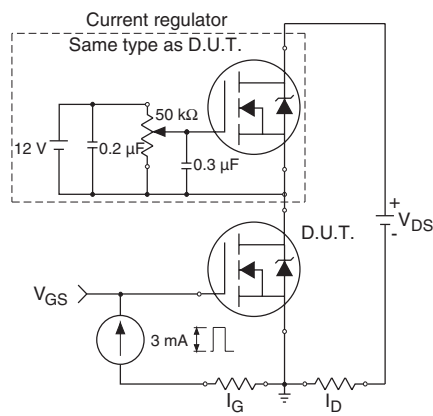
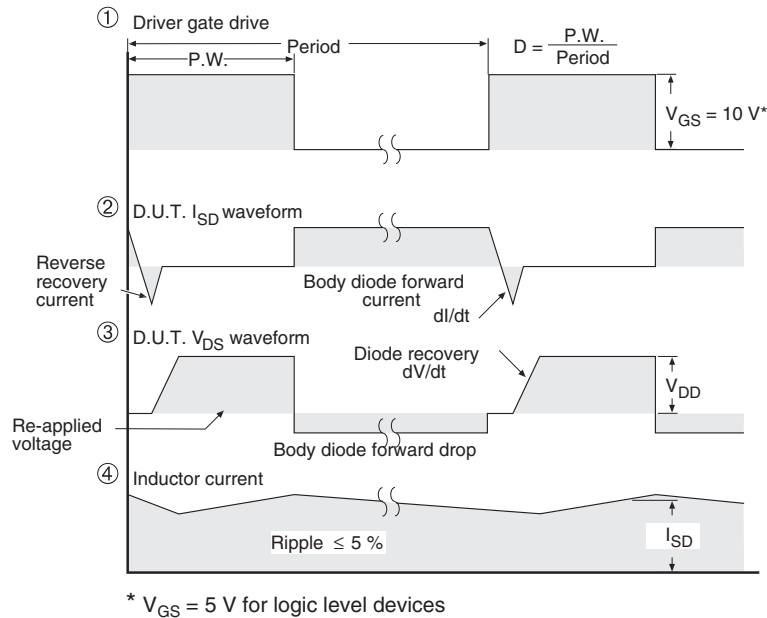
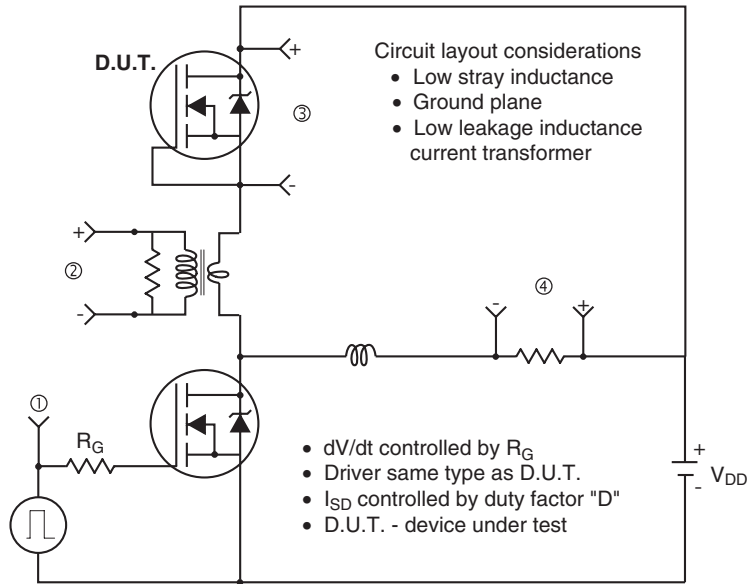


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery $dV/dt$ Test Circuit



**Fig. 14 - For N-Channel**

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