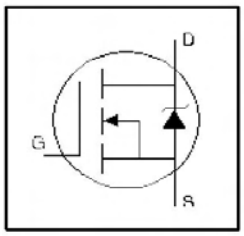
PD- 95756

International
IOR Rectifier

# IRL630PbF

HEXFET® Power MOSFET

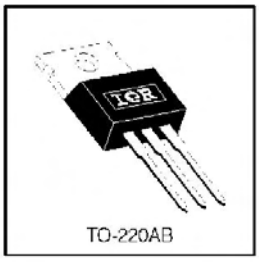



$V_{DSS}$ = 200V

$R_{DS(on)}$ = 0.40Ω

$I_D$ = 9.0A

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(ON)}$ Specified at $V_{GS}$ = 4V & 5V
- 150°C Operating Temperature
- Fast Switching
- Ease of paralleling
- Lead-Free



TO-220AB

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 5.0V | 9.0 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 5.0V | 5.7 | |
| $I_{DM}$ | Pulsed Drain Current ① | 36 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 74 | W |
| | Linear Derating Factor | 0.59 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ±10 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy ② | 250 | mJ |
| $I_{AR}$ | Avalanche Current ① | 9.0 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 7.4 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.0 | V/ns |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw. | 10 lbf•in (1.1N•m) | |

## Thermal Resistance

| | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | —— | 1.7 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | —— | 0.50 | —— | |
| $R_{\theta JA}$ | Junction-to-Ambient | —— | —— | 62 | |

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 200 | — | — | V | $V_{GS}$ = 0V, ID = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.27 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(ON)}$ | Static Drain-to-Source On-Resistance | — | — | 0.40 | Ω | $V_{GS}$ = 5.0V, $I_D$ = 5.4A ④ |
| | | — | — | 0.50 | | $V_{GS}$ = 4.0V, $I_D$ = 4.5A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 2.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $g_{fs}$ | Forward Transconductance | 4.8 | — | — | S | $V_{DS}$ = 50V, $I_D$ = 5.4A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 25 | µA | $V_{DS}$ = 200V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 160V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 10V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -10V |
| $Q_g$ | Total Gate Charge | — | — | 40 | nC | $I_D$ = 9.0A |
| $Q_{gs}$ | Gate-to-Source Charge | — | — | 5.5 | | $V_{DS}$ = 160V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | — | 24 | | $V_{GS}$ = 10V, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 8.0 | — | ns | $V_{DD}$ = 100V |
| $t_r$ | Rise Time | — | 57 | — | | $I_D$ = 9.0A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 38 | — | | $R_G$ = 6.0Ω |
| $t_f$ | Fall Time | — | 33 | — | | $R_D$ = 11Ω, See Fig. 10 ④ |
| $L_D$ | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | — | 7.5 | — | | |
| $C_{iss}$ | Input Capacitance | — | 1100 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 220 | — | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 70 | — | | $f$ = 1.0MHz, See Fig. 5 |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 9.0 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 36 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 2.0 | V | $T_J$ = 25°C, $I_S$ = 9.0A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | — | 230 | 350 | ns | $T_J$ = 25°C, $I_F$ = 9.0A |
| $Q_{rr}$ | Reverse Recovery Charge | — | 1.7 | 2.6 | µC | di/dt = 100A/µs ④ |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$+$L_D$) | | | | |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

② $V_{DD}$ = 25V, starting $T_J$ = 25°C, L = 4.6mH $R_G$ = 25Ω, $I_{AS}$ = 9.0A. (See Figure 12)

③ $I_{SD}$ ≤ 9.0A, di/dt ≤ 120A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 150°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

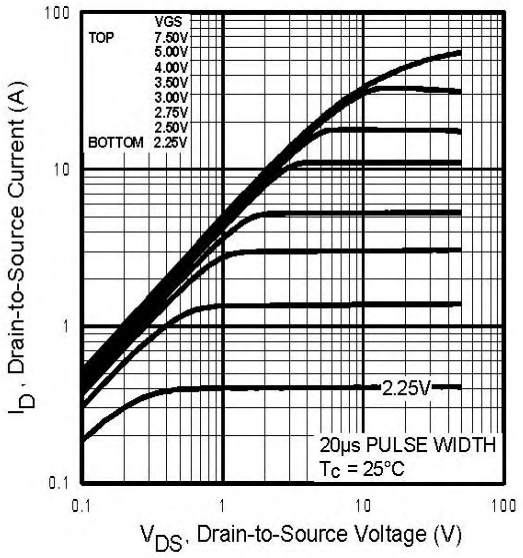



**Fig 1.** Typical Output Characteristics, $T_C = 25°C$

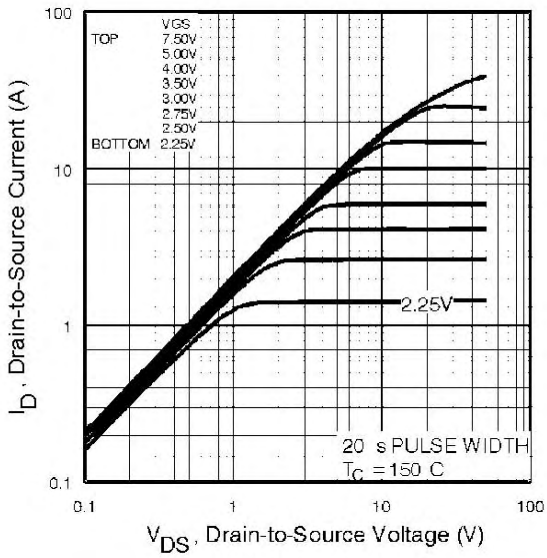



**Fig 2.** Typical Output Characteristics, $T_C = 150°C$

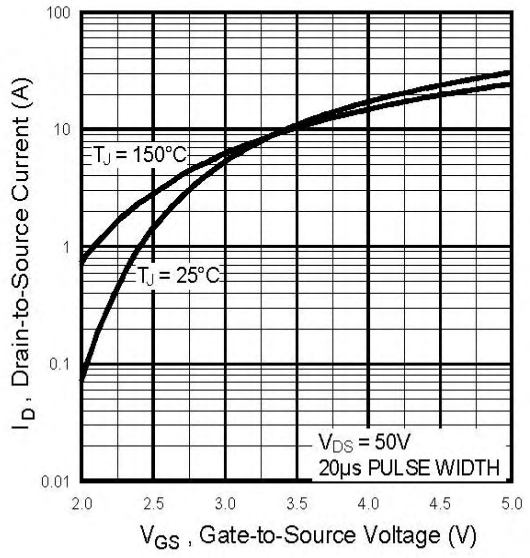



**Fig 3.** Typical Transfer Characteristics

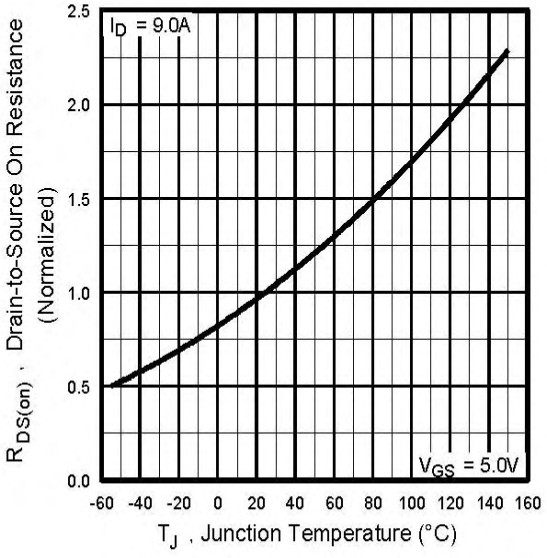



**Fig 4.** Normalized On-Resistance Vs. Temperature

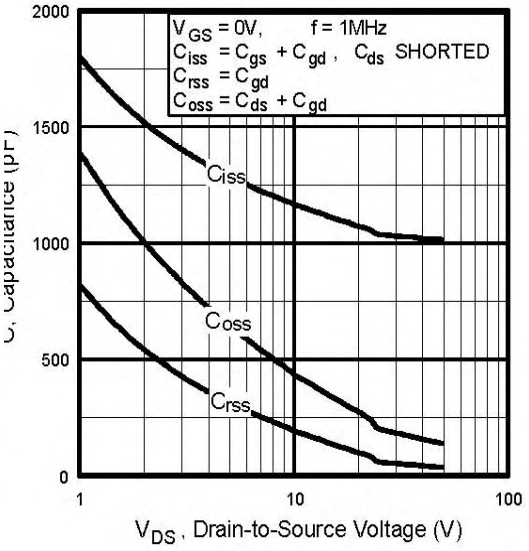



**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

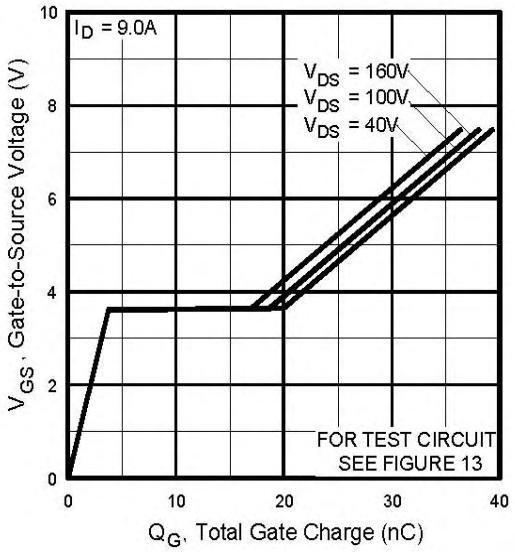



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

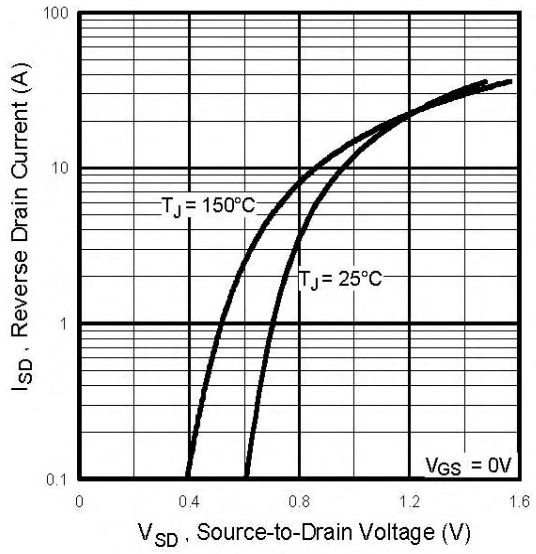



**Fig 7.** Typical Source-Drain Diode Forward Voltage

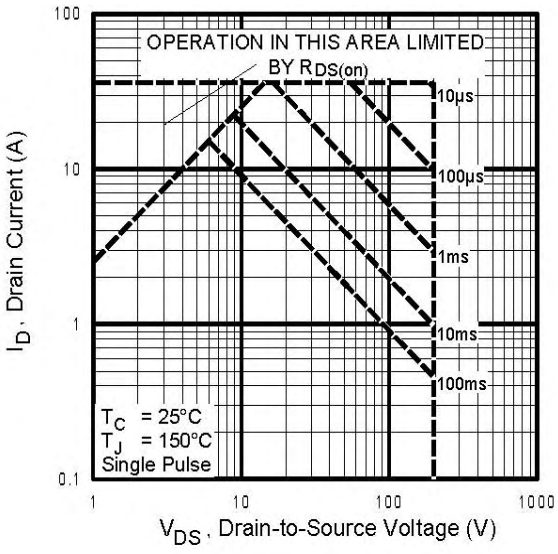



**Fig 8.** Maximum Safe Operating Area

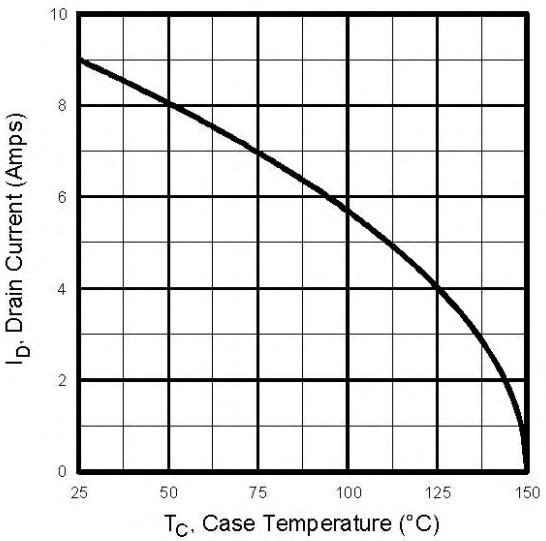



**Fig 9.** Maximum Drain Current Vs. Case Temperature

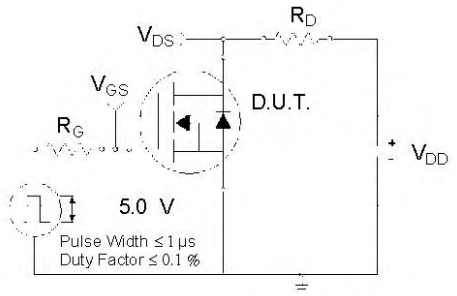



**Fig 10a.** Switching Time Test Circuit

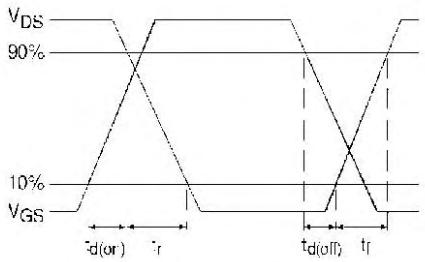



**Fig 10b.** Switching Time Waveforms

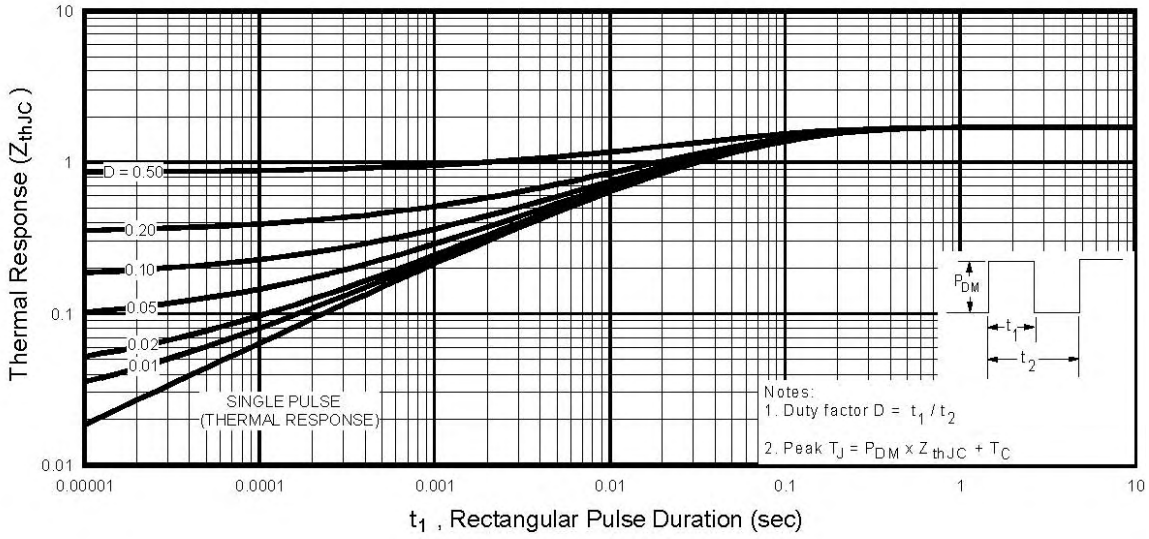



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

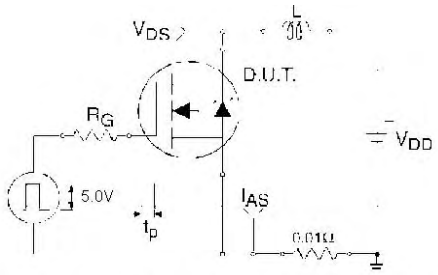



**Fig 12a.** Unclamped Inductive Test Circuit

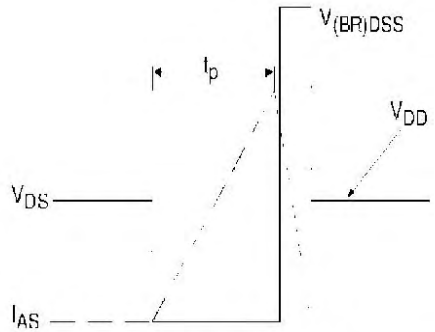



**Fig 12b.** Unclamped Inductive Waveforms

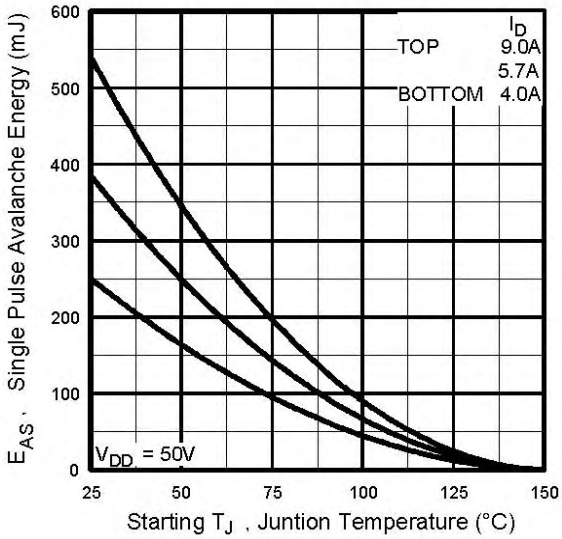



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

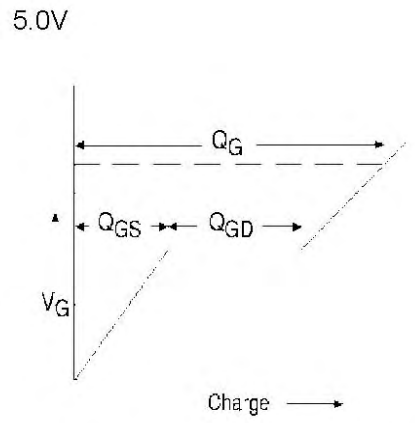



**Fig 13a.** Basic Gate Charge Waveform

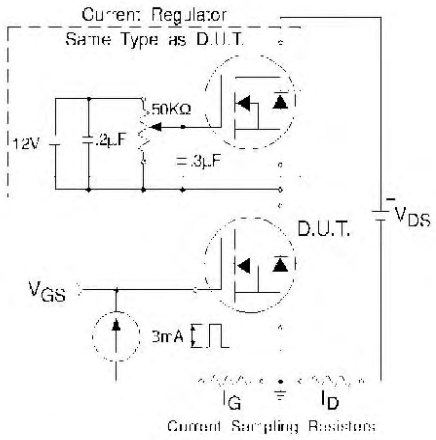
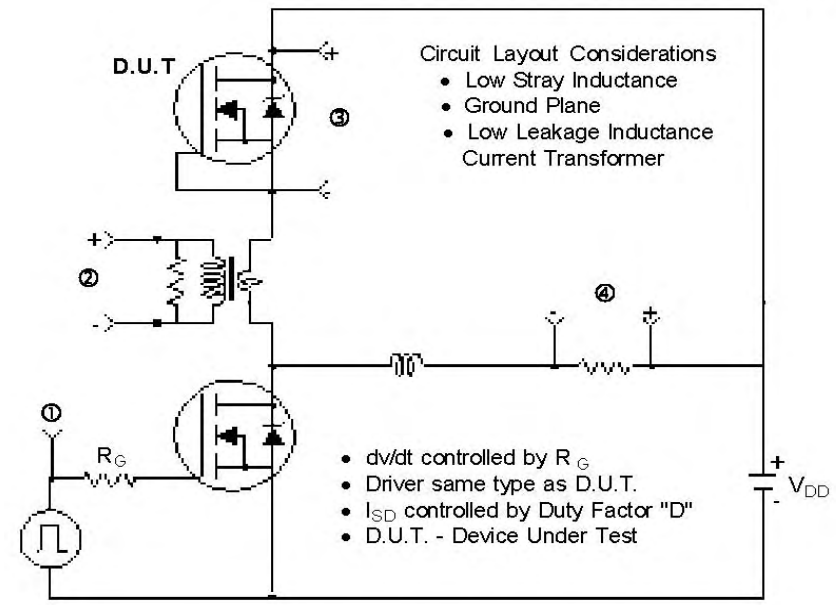
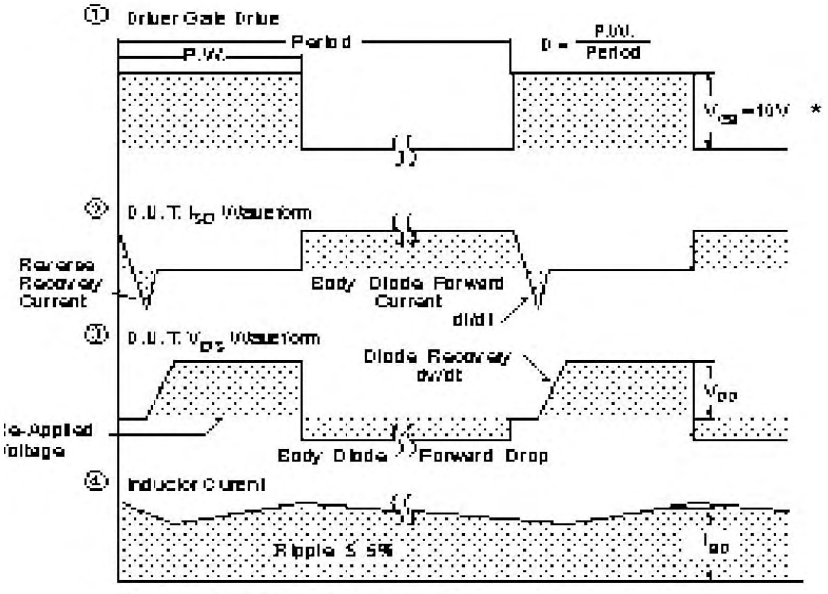



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



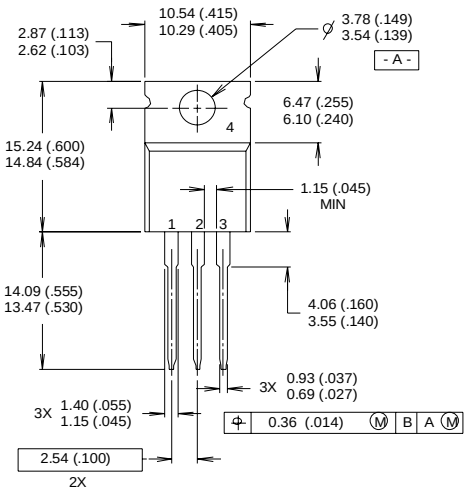



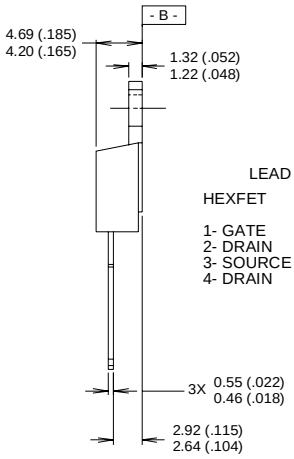

* VGS = 5V for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)




LEAD ASSIGNMENTS

| HEXFET | IGBTs, CoPACK |
|---|---|
| 1- GATE | 1- GATE |
| 2- DRAIN | 2- COLLECTOR |
| 3- SOURCE | 3- EMITTER |
| 4- DRAIN | 4- COLLECTOR |

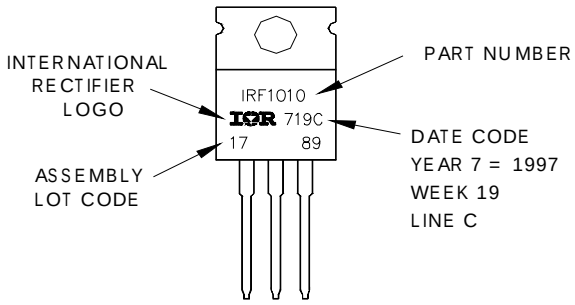
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

**Note:** "P" in assembly line position indicates "Lead-Free"




Data and specifications subject to change without notice.

International
IOR Rectifier

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08/04

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