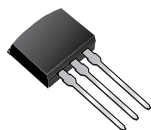
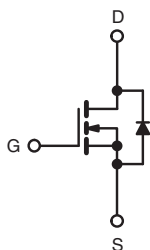
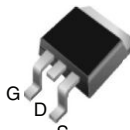


## Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	2.2
$Q_g$ (Max.) (nC)	23	
$Q_{gs}$ (nC)	5.4	
$Q_{gd}$ (nC)	11	
Configuration	Single	

**I<sup>2</sup>PAK (TO-262)**

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  Specified
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFBC30AS-GE3	SiHFBC30ASTRL-GE3 <sup>a</sup>	SiHFBC30ASTRR-GE3 <sup>a</sup>	SiHFBC30AL-GE3
Lead (Pb)-free	IRFBC30ASPbF	IRFBC30ASTRLPbF <sup>a</sup>	IRFBC30ASTRRPbF <sup>a</sup>	IRFBC30ALPbF
	SiHFBC30AS-E3	SiHFBC30ASTL-E3 <sup>a</sup>	SiHFBC30ASTR-E3 <sup>a</sup>	SiHFBC30AL-E3
SnPb	IRFBC30AS	IRFBC30ASTRL <sup>a</sup>	IRFBC30ASTRR <sup>a</sup>	IRFBC30AL
	SiHFBC30AS	SiHFBC30ASTL <sup>a</sup>	SiHFBC30ASTR <sup>a</sup>	SiHFBC30AL

#### Note

a. See device orientation.

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current <sup>a, e</sup>	$I_{DM}$	14	
Linear Derating Factor		0.69	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	290	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$	3.6	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	7.4	mJ
Maximum Power Dissipation	$P_D$	74	W
Peak Diode Recovery $dV/dt$ <sup>c, e</sup>	$dV/dt$	7.0	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 46\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 3.6\text{ A}$  (see fig. 12).
- $I_{SD} \leq 3.6\text{ A}$ ,  $dI/dt \leq 170\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- Uses IRFBC30A/SiHFBC30A data and test conditions.

\* Pb containing terminations are not RoHS compliant, exemptions may apply


**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.7	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>d</sup>		-	0.67	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	-	25	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 2.2 A <sup>b</sup>	-	-	2.2	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 2.2 A		2.1	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	510	-	pF
Output Capacitance	C <sub>oss</sub>			-	70	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	3.5	-	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	730	-	pF
			V <sub>DS</sub> = 480 V, f = 1.0 MHz	-	19	-	
Effective Output Capacitance	C <sub>oss eff.</sub>		V <sub>DS</sub> = 0 V to 480 V <sup>c</sup>	-	31	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.6 A, V <sub>DS</sub> = 480 V, see fig. 6 and 13 <sup>b</sup>	-	-	23	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	5.4	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	11	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 3.6 A, R <sub>g</sub> = 12 Ω, R <sub>D</sub> = 82 Ω, see fig. 10 <sup>b, d</sup>		-	9.8	-	ns
Rise Time	t <sub>r</sub>			-	13	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	19	-	
Fall Time	t <sub>f</sub>			-	12	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	3.6	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	14	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 3.6 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.6	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.6 A, dI/dt = 100 A/μs <sup>b</sup> ,		-	400	600	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	1.1	1.7	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .  
c.  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .  
d. Uses IRFBC30A/SiHFBC30A data and test conditions.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

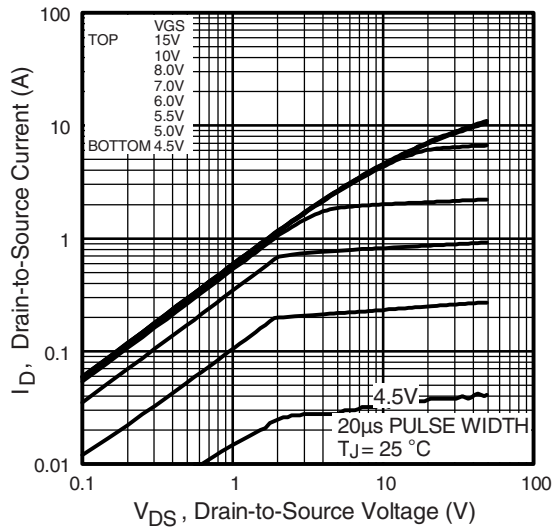


Fig. 1 - Typical Output Characteristics

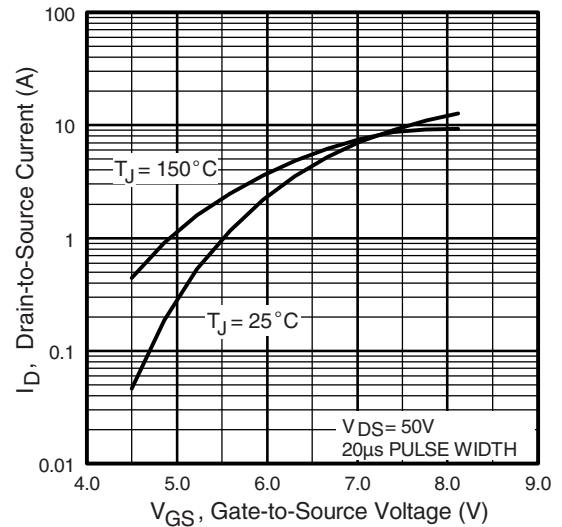


Fig. 3 - Typical Transfer Characteristics

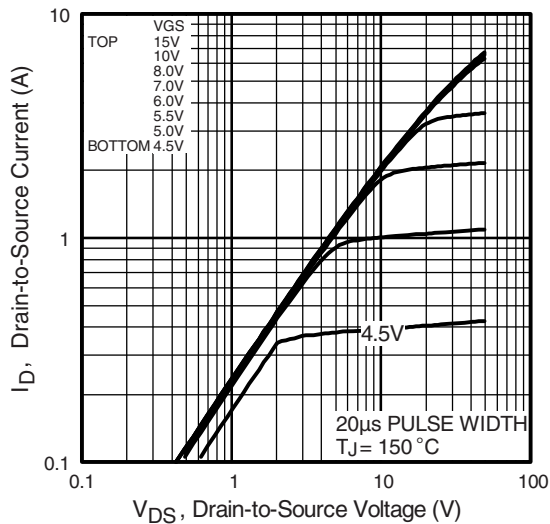


Fig. 2 - Typical Output Characteristics

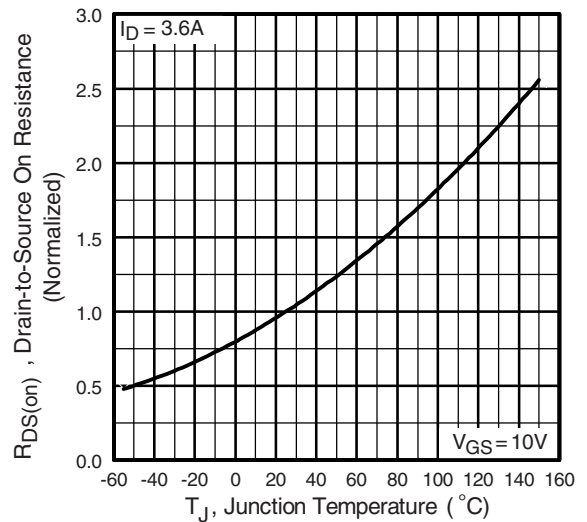


Fig. 4 - Normalized On-Resistance vs. Temperature

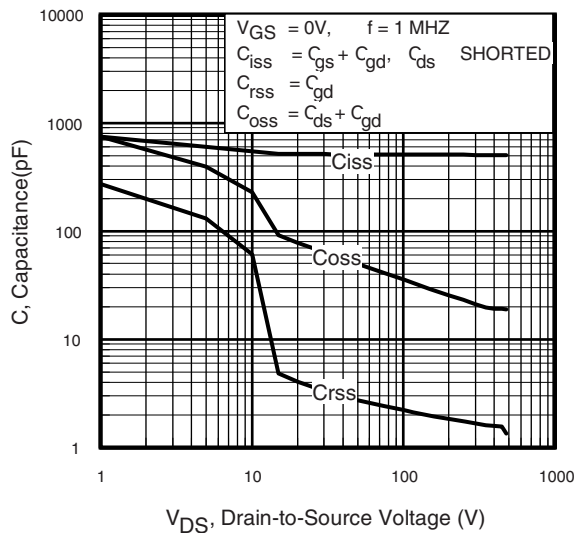


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

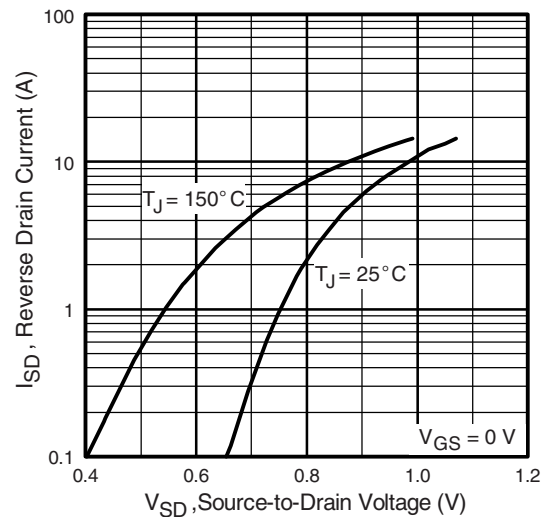


Fig. 7 - Typical Source-Drain Diode Forward Voltage

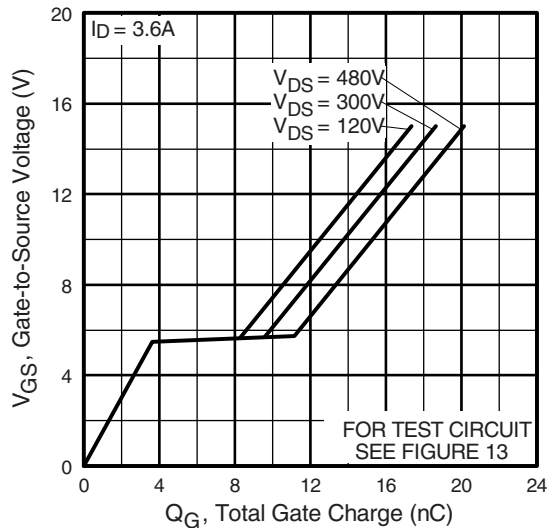


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

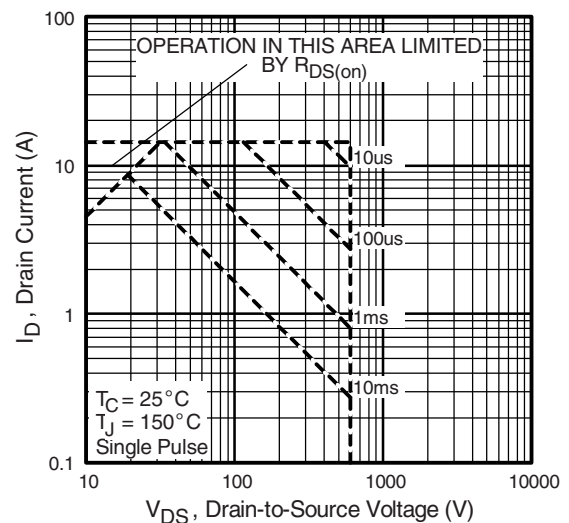


Fig. 8 - Maximum Safe Operating Area

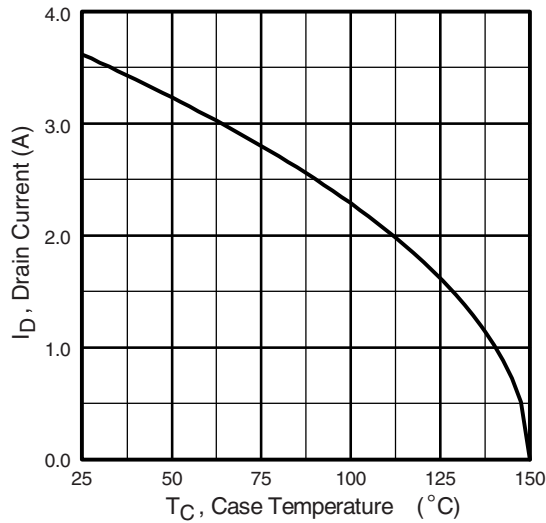


Fig. 9 - Maximum Drain Current vs. Case Temperature

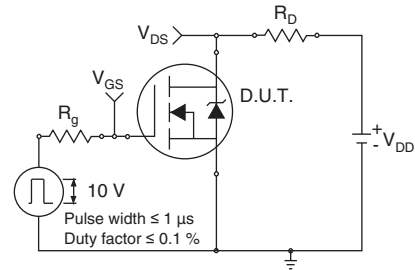


Fig. 10a - Switching Time Test Circuit

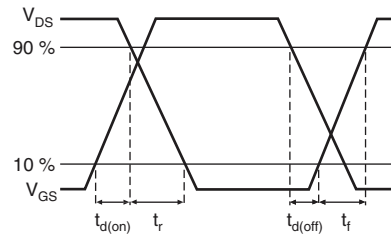


Fig. 10b - Switching Time Waveforms

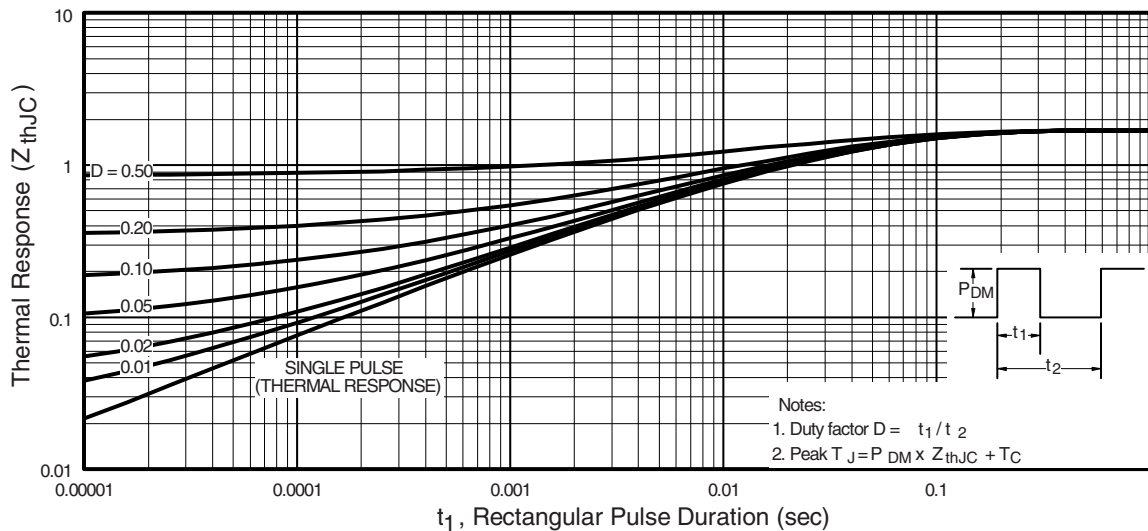


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

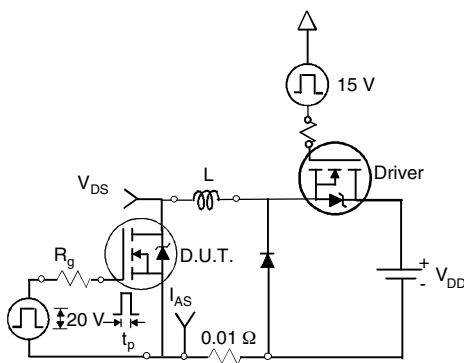


Fig. 12a - Unclamped Inductive Test Circuit

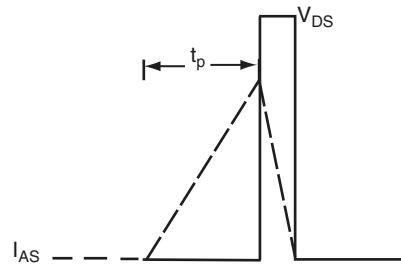


Fig. 12b - Unclamped Inductive Waveforms

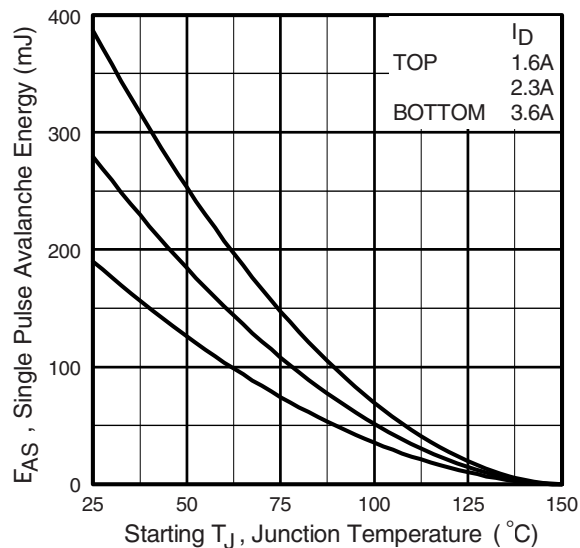


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

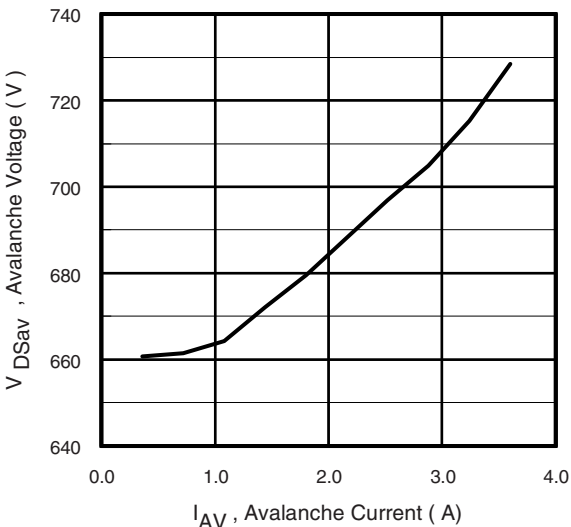


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

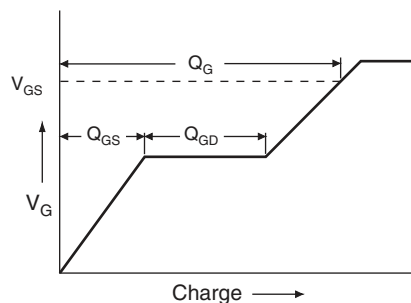


Fig. 13a - Basic Gate Charge Waveform

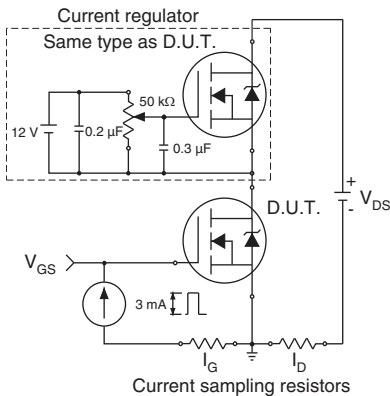
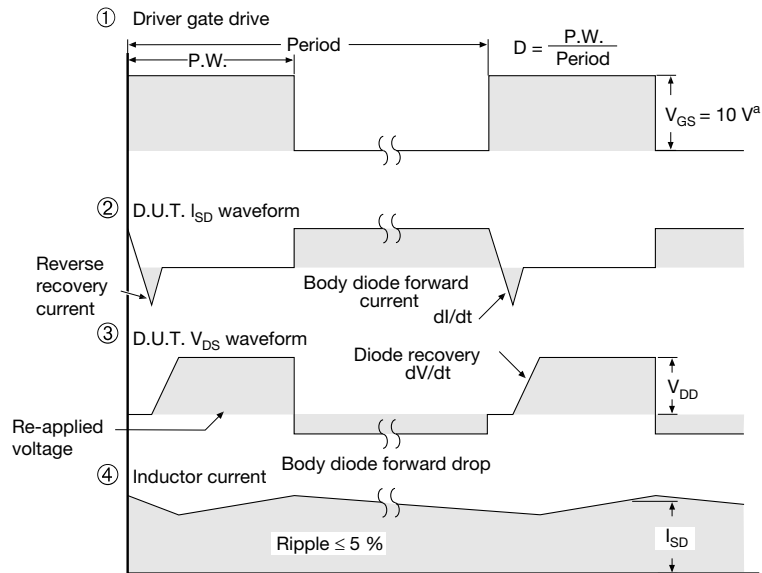
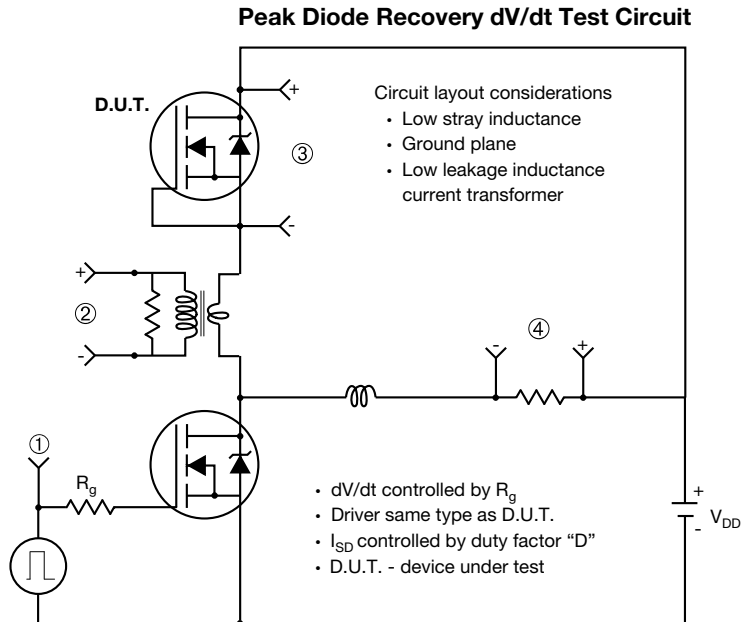


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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