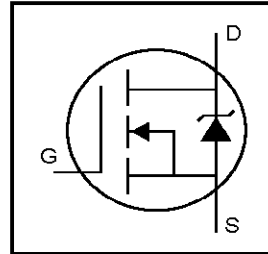


IRFBC40S/LPbF

HEXFET® Power MOSFET

- Surface Mount (IRFBC40S)
- Low-profile through-hole (IRFBC40L)
- Available in Tape & Reel (IRFBC40S)
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

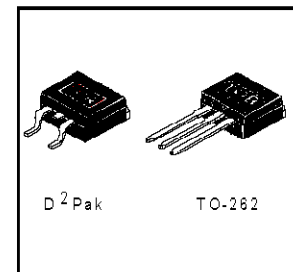


$V_{DSS} = 600V$
$R_{DS(on)} = 1.2\Omega$
$I_D = 6.2A$

Description

Third generation HEXFETs from international Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRFBC40L) is available for low-profile applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ Ⓞ	6.2	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ Ⓞ	3.9	
I_{DM}	Pulsed Drain Current ① ⑤	25	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ② ⑤	570	mJ
I_{AR}	Avalanche Current ①	6.2	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③ ⑤	3.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	600	---	---	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	---	0.70	---	V/°C	Reference to 25°C, I _D = 1mA ^⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance	---	---	1.2	Ω	V _{GS} = 10V, I _D = 3.7A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	---	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	4.7	---	---	S	V _{DS} = 100V, I _D = 3.7A ^⑤
I _{DSS}	Drain-to-Source Leakage Current	---	---	100	μA	V _{DS} = 600V, V _{GS} = 0V
		---	---	500		V _{DS} = 480V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	---	---	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	---	---	-100		V _{GS} = -20V
Q _g	Total Gate Charge	---	---	60	nC	I _D = 6.2A
Q _{gs}	Gate-to-Source Charge	---	---	8.3		V _{DS} = 3600V
Q _{gd}	Gate-to-Drain ("Miller") Charge	---	---	30		V _{GS} = 10V, See Fig. 6 and 13 ^{④⑤}
t _{d(on)}	Turn-On Delay Time	---	13	---	ns	V _{DD} = 300V
t _r	Rise Time	---	18	---		I _D = 6.2A
t _{d(off)}	Turn-Off Delay Time	---	55	---		R _G = 9.1Ω
t _f	Fall Time	---	20	---		R _D = 47Ω, See Fig. 10 ^{④⑤}
L _S	Internal Source Inductance	---	7.5	---	nH	Between lead, and center of die contact
C _{iss}	Input Capacitance	---	1300	---	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	---	160	---		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	---	30	---		f = 1.0MHz, See Fig. 5 ^⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	---	---	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ^①	---	---	25		
V _{SD}	Diode Forward Voltage	---	---	1.5	V	T _J = 25°C, I _S = 6.2A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	---	450	940	ns	T _J = 25°C, I _F = 6.2A
Q _{rr}	Reverse Recovery Charge	---	3.8	7.9	μC	di/dt = 100A/μs ^{④⑤}
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = 50V, starting T_J = 25°C, L = 27mH, R_G = 25Ω, I_{AS} = 6.2A. (See Figure 11)
- ③ I_{SD} ≤ 6.2A, di/dt ≤ 80A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRFBC40 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

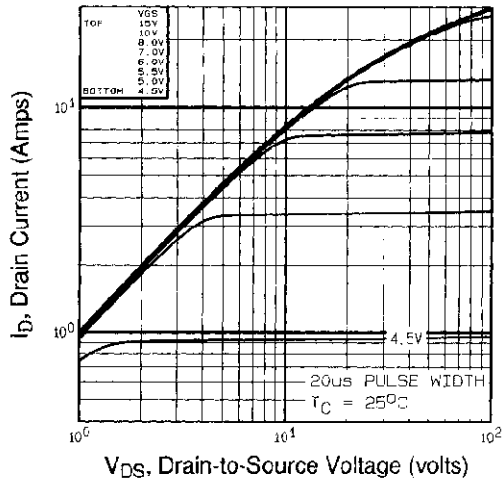


Fig 1. Typical Output Characteristics,

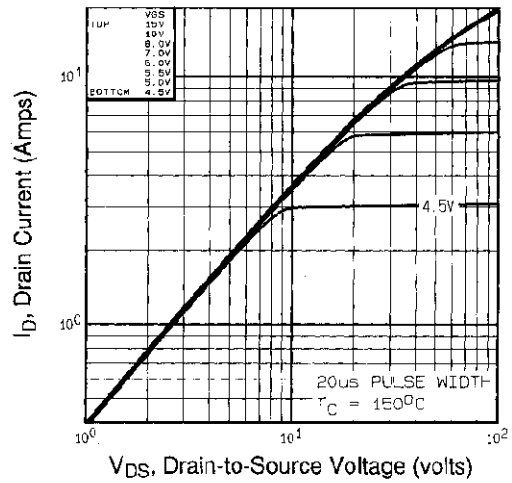


Fig 2. Typical Output Characteristics,

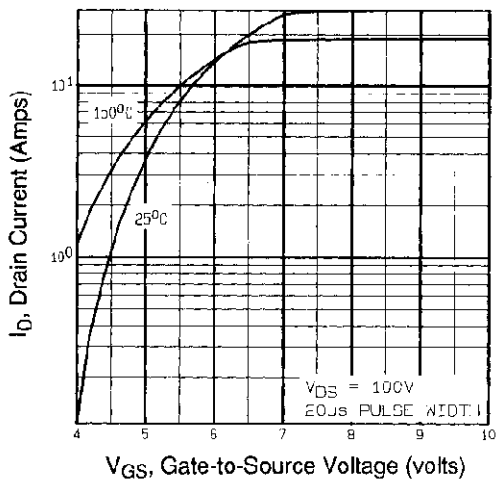


Fig 3. Typical Transfer Characteristics

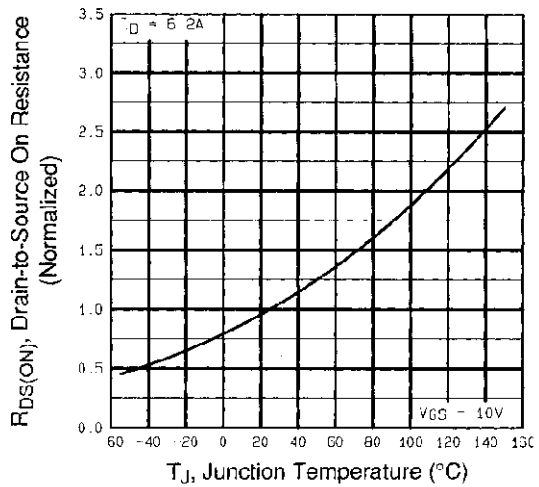


Fig 4. Normalized On-Resistance Vs. Temperature

IRFBC40S/LPbF

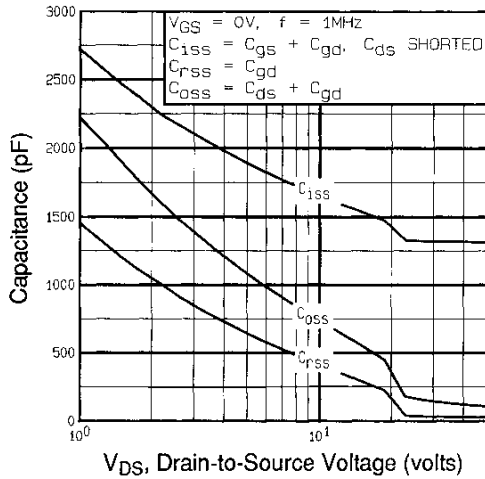


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

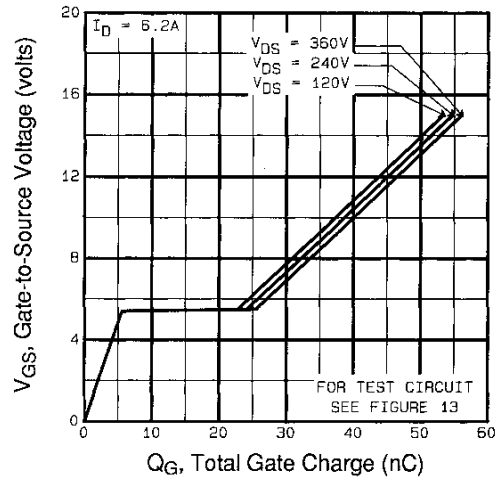


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

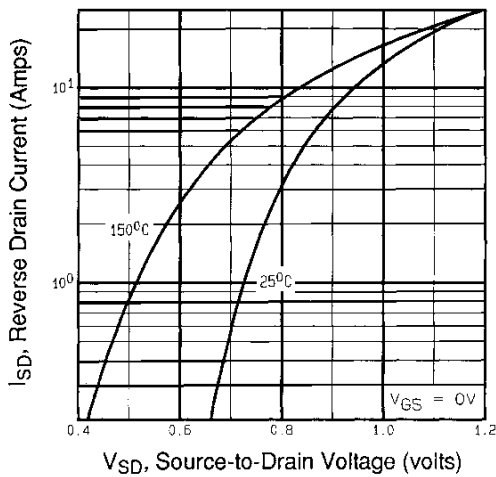


Fig 7. Typical Source-Drain Diode Forward Voltage

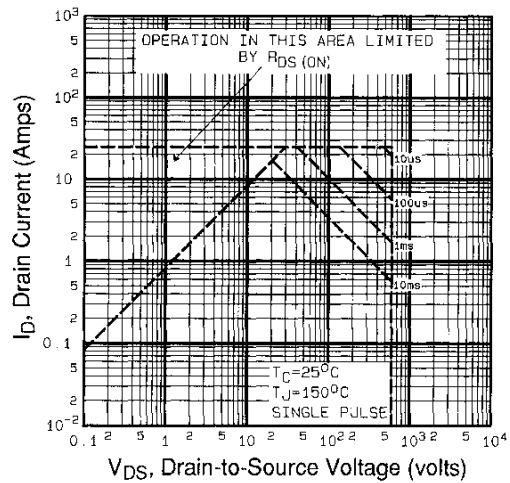


Fig 8. Maximum Safe Operating Area

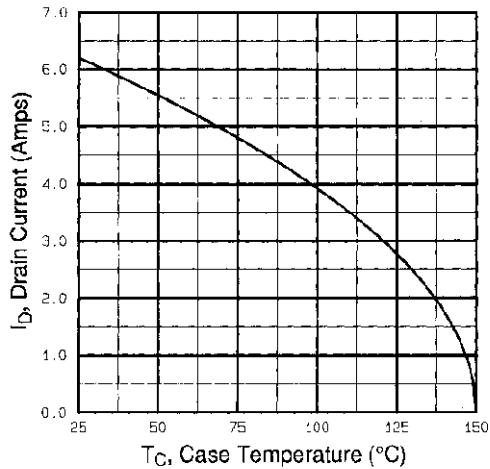


Fig 9. Maximum Drain Current Vs. Case Temperature

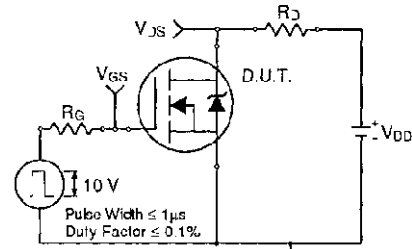


Fig 10a. Switching Time Test Circuit

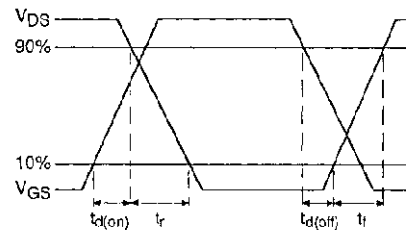


Fig 10b. Switching Time Waveforms

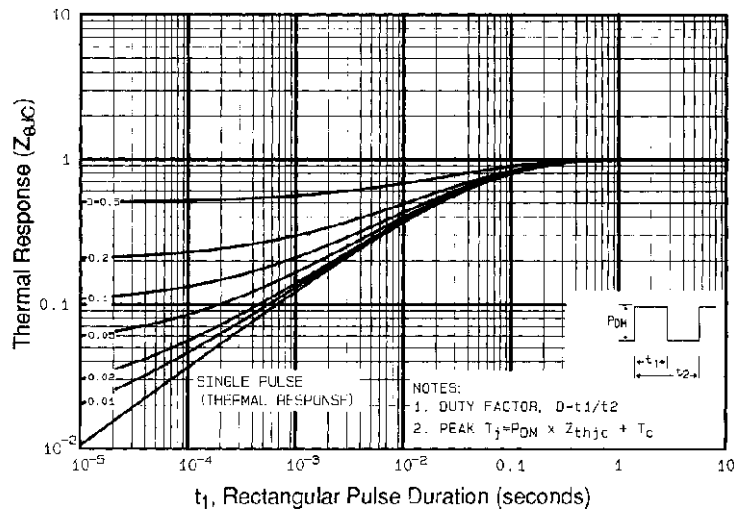


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFBC40S/LPbF

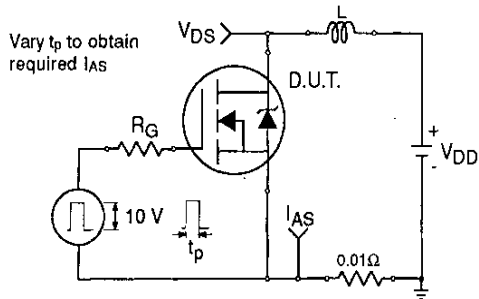


Fig 12a. Unclamped Inductive Test Circuit

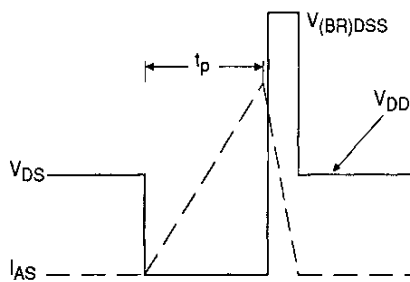


Fig 12b. Unclamped Inductive Waveforms

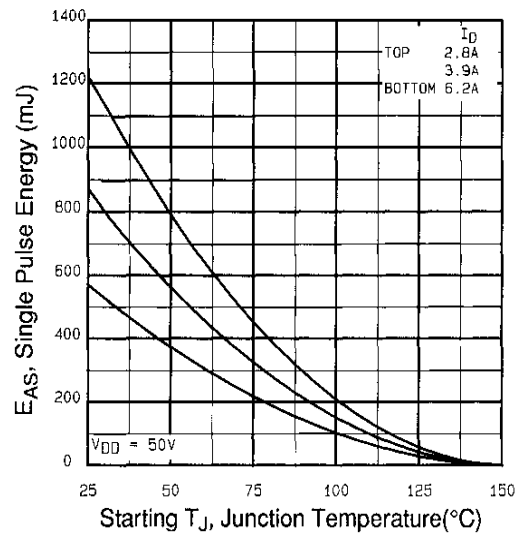


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

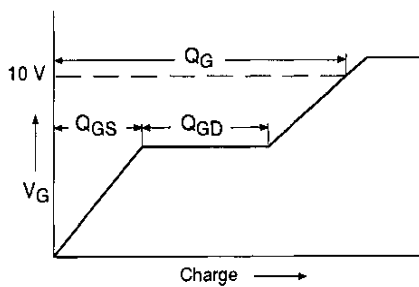


Fig 13a. Basic Gate Charge Waveform

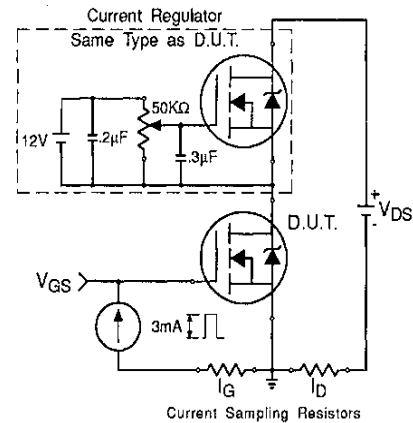


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

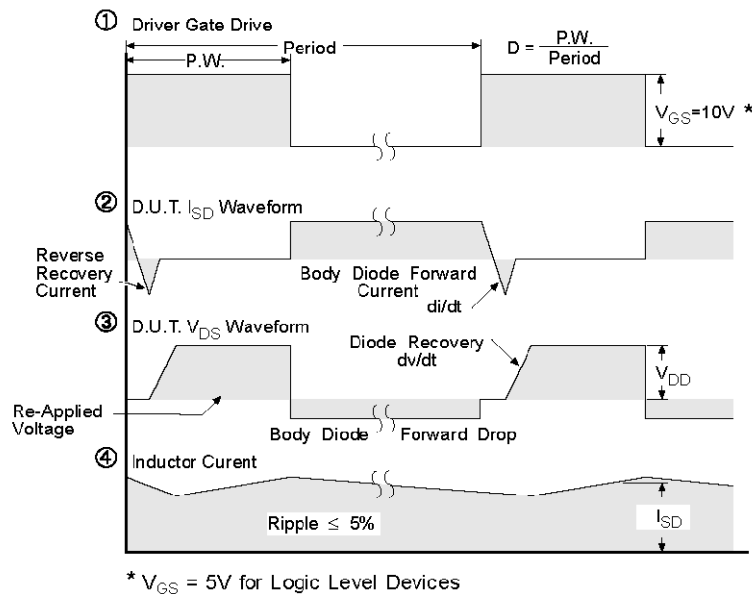
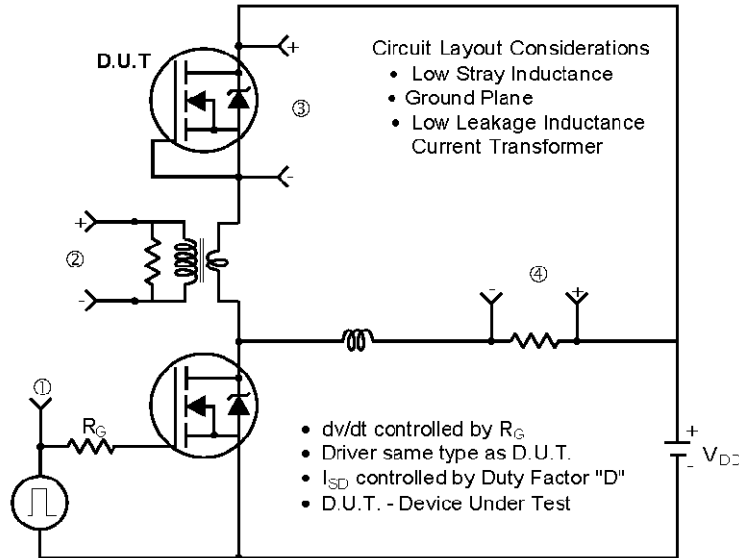
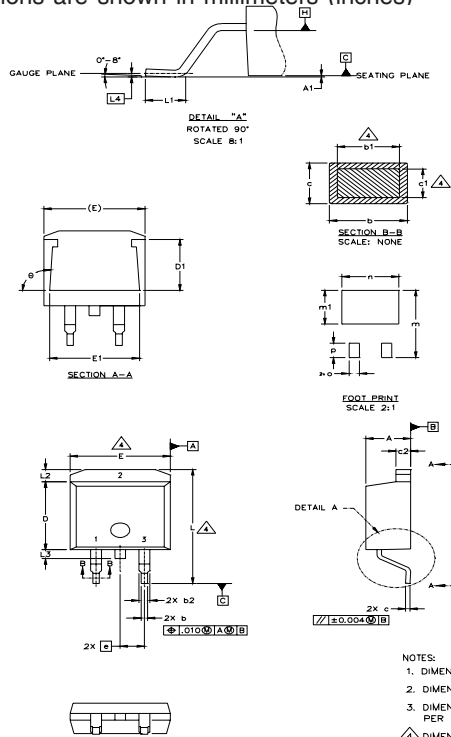


Fig 14.For N-Channel HEXFETS

IRFBC40S/LPbF

D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	3
D	8.51	9.65	.335	.380	
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs_CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

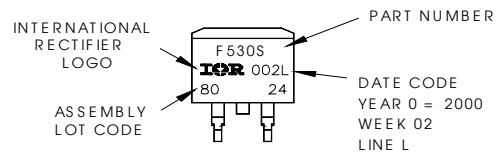
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

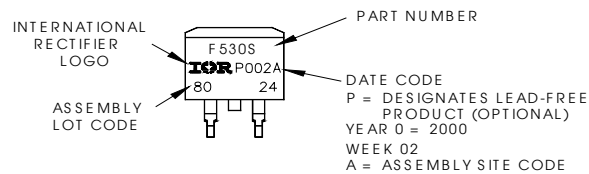
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

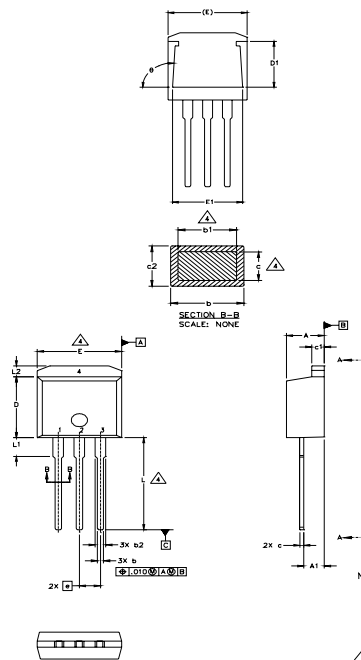
Note: "P" in assembly line
position indicates "Lead-Free"



OR



TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

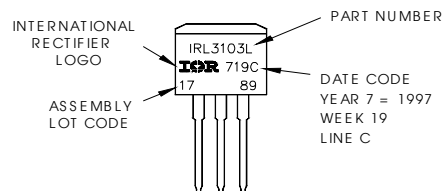
HEXFET	IGBT
1. - GATE	1 - GATE
2. - DRAIN	2 - COLLECTOR
3. - SOURCE	3 - EMITTER
4. - DRAIN	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
 3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

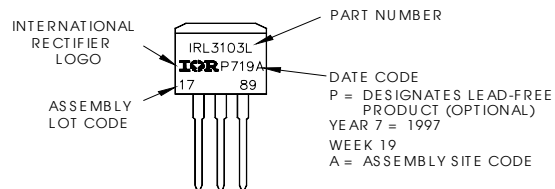
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



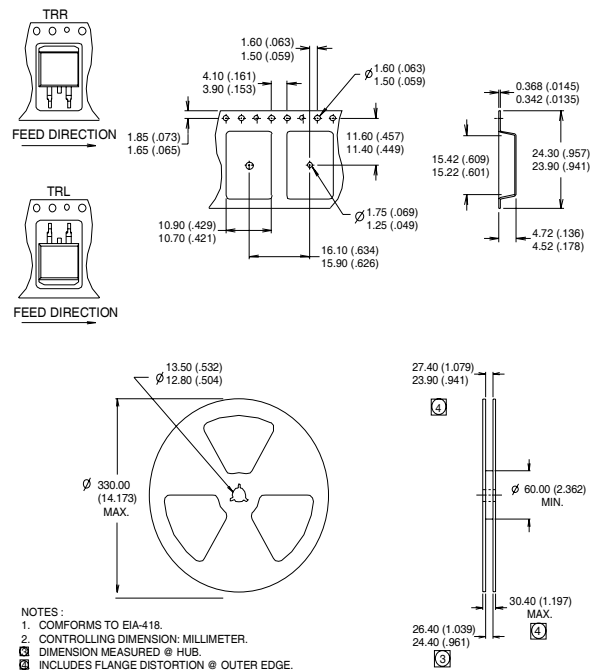
OR



IRFBC40S/LPbF

International
IOR Rectifier

D²Pak Tape & Reel Information



Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

07/04

Document Number: 91116

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